

Features

- Synchronizes to standard telecom or Ethernet backplane clocks and provides jitter filtered output clocks for SONET/SDH, PDH and Ethernet network interface cards
- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks
- Meets the SONET/SDH jitter generation requirements up to OC-192/STM-64
- Two independent DPLLs provides timing for the transmit path (backplane to line rate) and the receive path (recovered line rate to backplane)
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Selectable loop bandwidth of 14 Hz, 28 Hz, 890 Hz, 3.5 Hz, 1.7 Hz, or 0.1 Hz
- Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs

Ordering Information

ZL30146GGG	64 Pin CABGA	Trays
ZL30146GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Programmable output synthesizer to generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz (e.g., T1/E1, DS3/E3)
- Generates several styles of output frame pulse with selectable pulse width, polarity, and frequency
- Configurable input to output delay and output to output phase alignment
- Configurable through a serial interface (SPI or I²C)
- DPLLs can be configured to provide synchronous or asynchronous clock outputs

Applications

- ITU-T G.8262 Line Cards which support 1 GbE and 10 GbE interfaces
- SONET/SDH line cards up to OC-192/STM-64

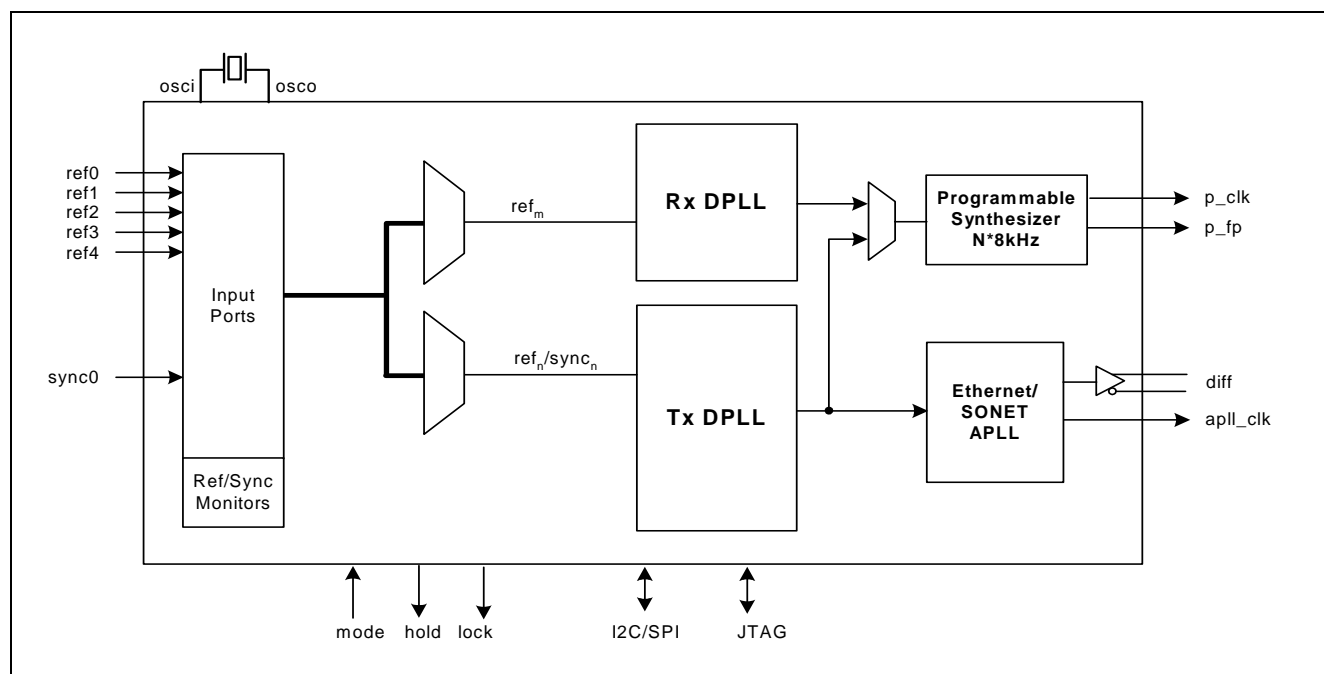


Figure 1 - Functional Block Diagram

1.0 Functional Description

The ZL30146 OC-192/STM-64 PDH/SONET/SDH/Synchronous Ethernet Network Interface Synchronizer is a highly integrated device that provides timing for both PDH/SONET/SDH and Ethernet network interface cards. A functional block diagram is shown in Figure 1.

This device is ideally suited for designs that require both a transmit timing path (backplane to PHY) and a receive timing path (PHY to backplane). Each path is controlled with separate DPLLs (Tx DPLL, Rx DPLL) which are both independently configurable through the serial interface (SPI or I²C). A typical application of the ZL30146 is shown in Figure 2. In this application, the ZL30146 translates the 19.44 MHz clock from the telecom rate backplane (system timing bus), translates the frequency to 622.08 MHz or 156.25 MHz for the PHY Tx clock, and filters the jitter to ensure compliance with the related standards. On the receive path, the Rx DPLL and the programmable synthesizer translate the line recovered clock (8 kHz or 25 MHz) from the PHY to the 19.44 MHz telecom backplane (line recovered timing) for the central timing cards. The ZL30146 allows easy integration of Ethernet line rates with today's telecom backplanes.

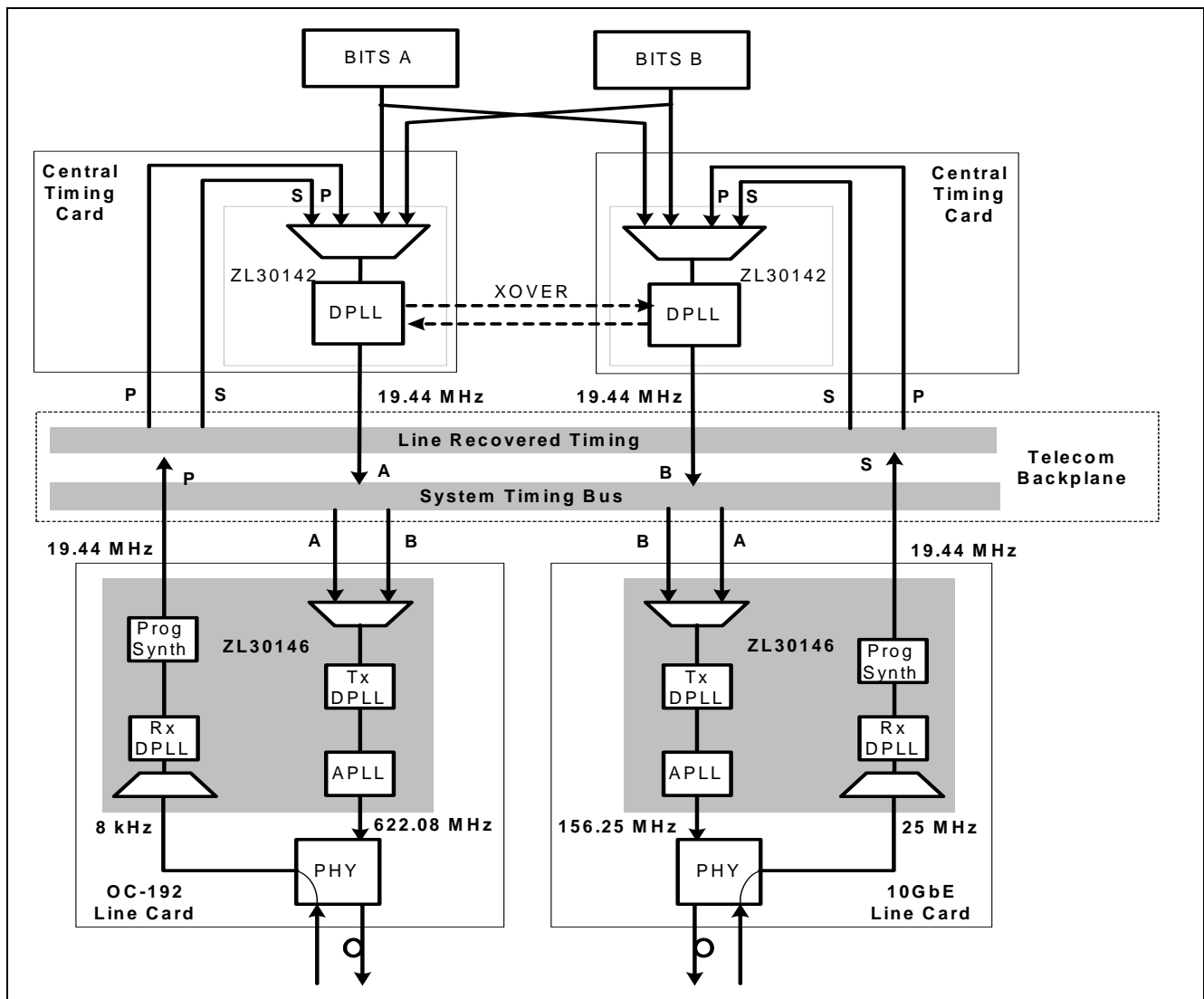
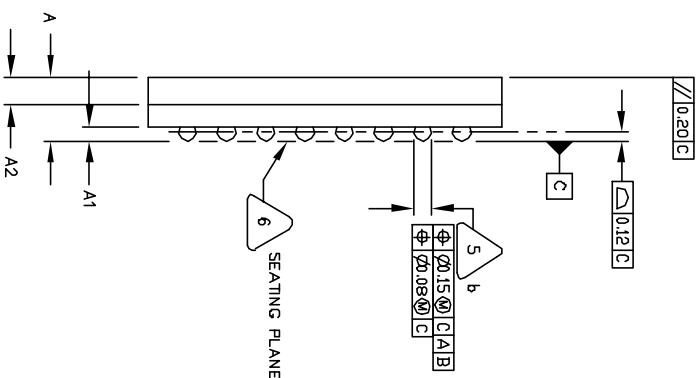
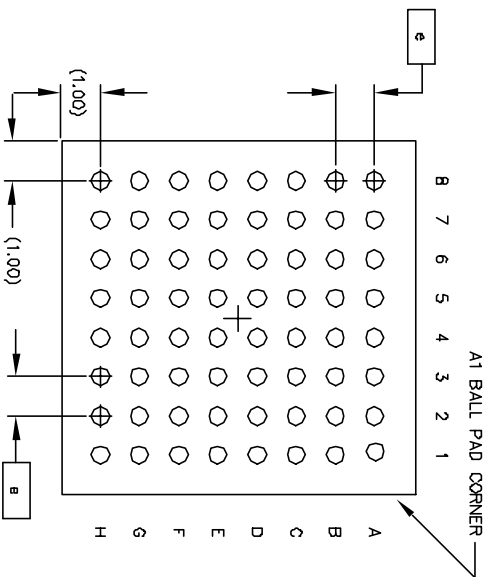
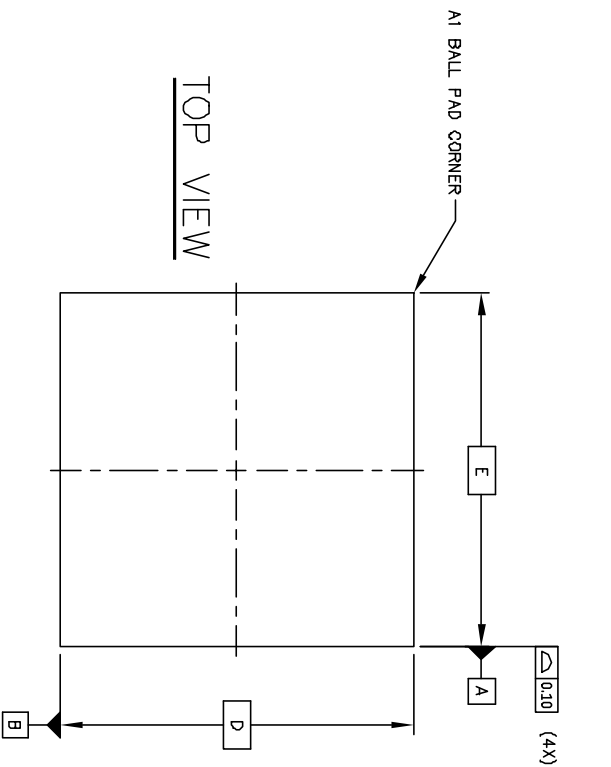


Figure 2 - Typical Application of the ZL30146



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 Typ.		
D	9.00 REF.		
E	9.00 Ref.		
e	1.0 Ref		
n	64		

SIDE VIEW



PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.



DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

BOTTOM VIEW

64 SOLDER BALLS

1. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.
2. Not to Scale.
3. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
4. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

© Zarlink Semiconductor 2005 All rights reserved.			
ISSUE	1		
ACN	CDCA		
DATE	15Apr105		
APPRD.			



Previous package codes		Package Code	GC
N/A		Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA	
		111039	



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I2C components conveys a license under the Philips I2C Patent rights to use these components in an I2C System, provided that the system conforms to the I2C Standard Specification as defined by Philips.

Zarlink, ZL, the Zarlink Semiconductor logo and the Legerity logo and combinations thereof, VoiceEdge, VoicePort, SLAC, ISLIC, ISLAC and VoicePath are trademarks of Zarlink Semiconductor Inc.

TECHNICAL DOCUMENTATION - NOT FOR RESALE

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microsemi:](#)

[ZL30146GGG2](#)