

TC74HC592AP, TC74HC592AF

8-Bit Binary Counter with Input Register

The TC74HC592A is high speed CMOS 8-BIT REGISTER COUNTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable (CCKEN) is held "L" level. If Counter clear (CCLR) is held "L", the internal counter is cleared asynchronously to clock.

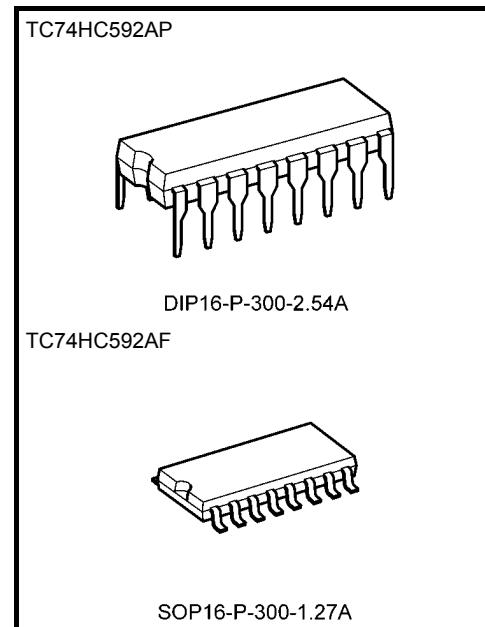
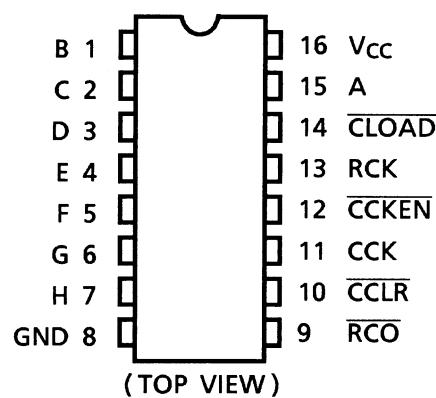
Input A to H are loaded to register at positive edge of Register Clock (RCK), and the register outputs are loaded to Counter when Counter Load (CLOAD) is held "L" level.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{max} = 35$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Output drive capability: 10 LSTTL loads for QA to QH
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 4$ mA (min)
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS592

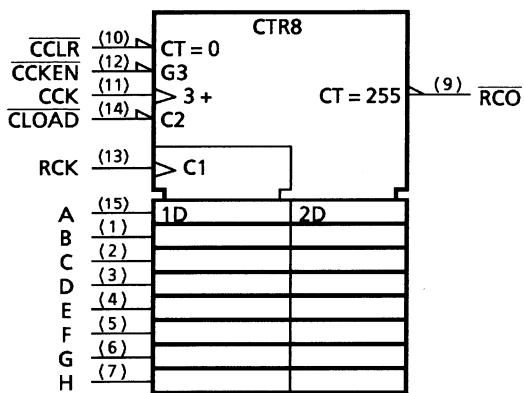
Pin Assignment



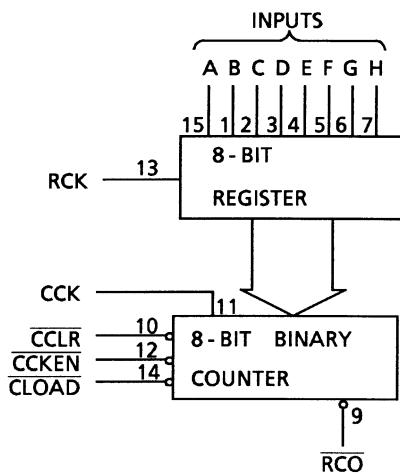
Weight

DIP16-P-300-2.54A:	1.00 g (typ.)
SOP16-P-300-1.27A:	0.18 g (typ.)

IEC Logic Symbol



Block Diagram



Truth Table

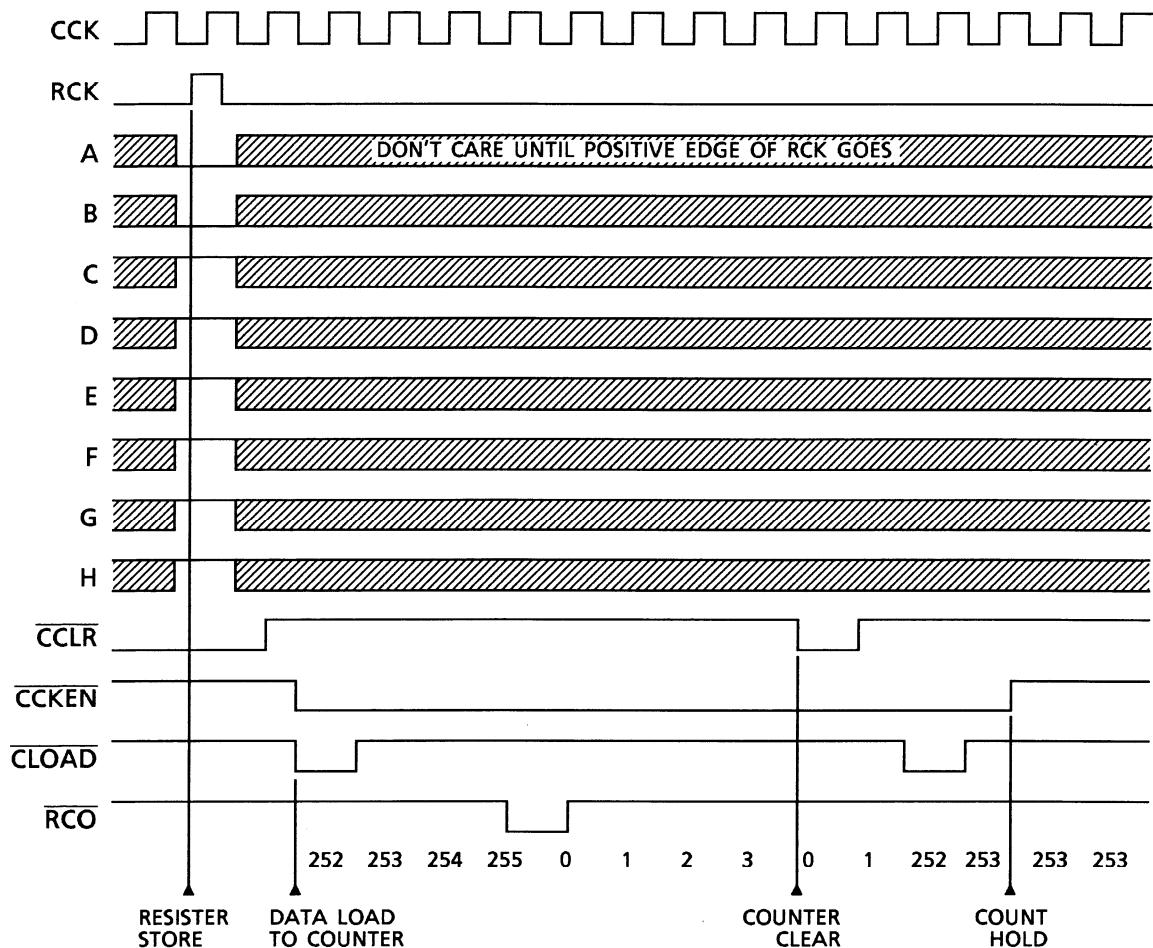
Inputs					Function
RCK	CLOAD	$\overline{\text{CCLR}}$	$\overline{\text{CCKEN}}$	CCK	
X	L	H	X	X	Register data is loaded into counter
X	H	L	X	X	Counter clear
\uparrow	X	X	X	X	The data of A thru H inputs is stored into register
\downarrow	X	X	X	X	Register state is not changed
X	H	H	L	\uparrow	Counter advances the count
X	H	H	L	\downarrow	No count
X	H	H	H	X	No count

X: Don't care

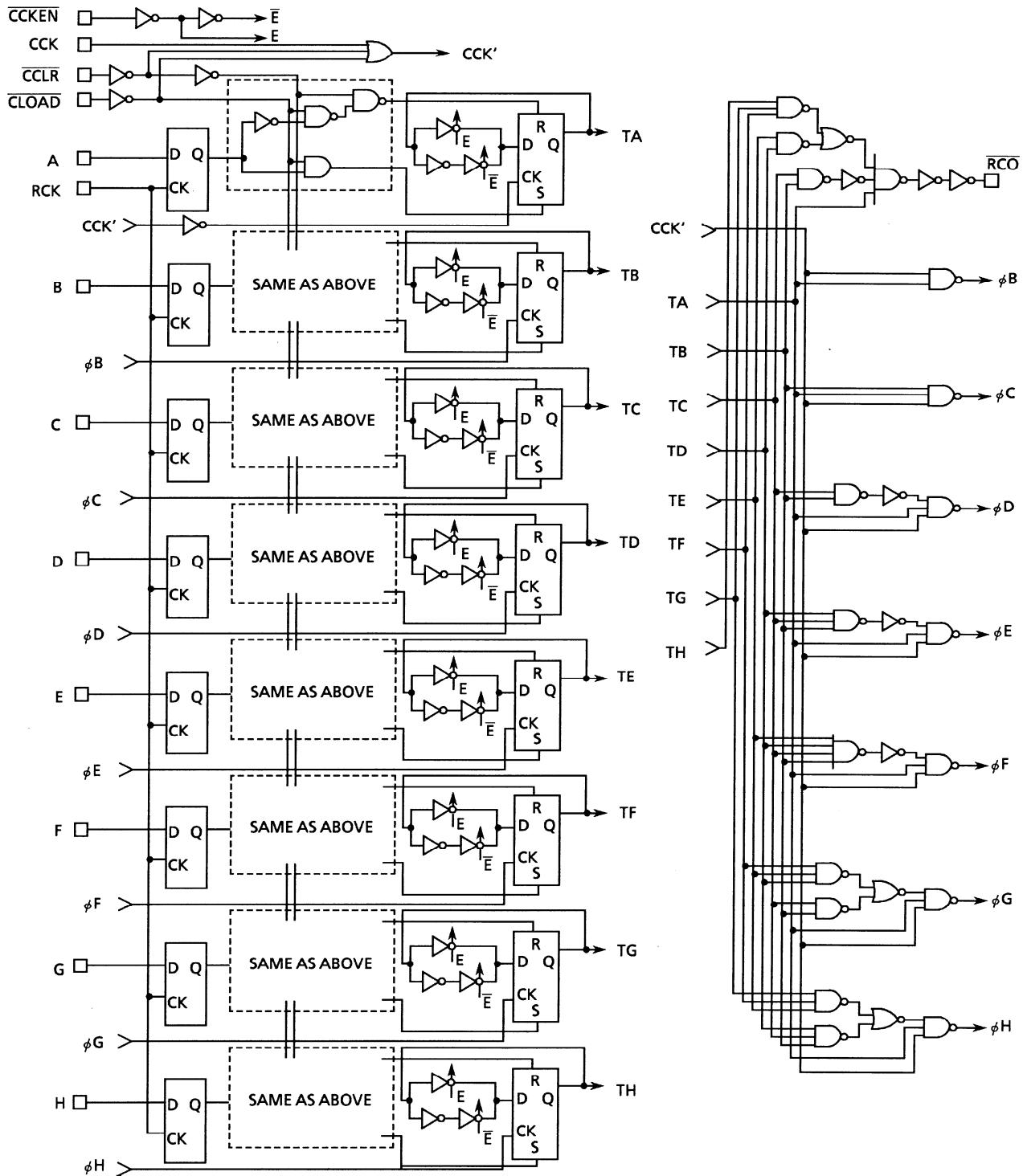
 $\text{RCO} = \text{QA}' \cdot \text{QB}' \cdot \text{QC}' \cdot \text{QD}' \cdot \text{QE}' \cdot \text{QF}' \cdot \text{QG}' \cdot \text{QH}'$

(QA' to QH': internal outputs of the counter)

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to 7	V
DC input voltage	V_{IN}	–0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	–0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2) / 180 (SOP)	mW
Storage temperature	T_{STG}	–65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of $-10 \text{ mW/}^\circ\text{C}$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{OPR}	–40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0 \text{ V}$) 0 to 500 ($V_{CC} = 4.5 \text{ V}$) 0 to 400 ($V_{CC} = 6.0 \text{ V}$)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit		
				V _{CC} (V)	Min	Typ.	Max	Min			
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V	
				4.5	3.15	—	—	3.15	—		
				6.0	4.20	—	—	4.20	—		
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V	
				4.5	—	—	1.35	—	1.35		
				6.0	—	—	1.80	—	1.80		
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 µA	2.0	1.9	2.0	—	1.9	—	V	
				4.5	4.4	4.5	—	4.4	—		
				6.0	5.9	6.0	—	5.9	—		
			I _{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—		
				6.0	5.68	5.80	—	5.63	—		
			I _{OL} = 20 µA	2.0	—	0.0	0.1	—	0.1		
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}		4.5	—	0.0	0.1	—	0.1	V	
				6.0	—	0.0	0.1	—	0.1		
		I _{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33			
			6.0	—	0.18	0.26	—	0.33			
Input leakage current	I _{IN}		V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I _{CC}		V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	µA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Typ.	Limit	
Minimum pulse width (CCK, RCK)	t _W (H) t _W (L)	—	2.0	—	75	95
			4.5	—	15	19
			6.0	—	13	16
Minimum pulse width (<u>CCLR</u>)	t _W (L)	—	2.0	—	100	125
			4.5	—	20	25
			6.0	—	16	21
Minimum pulse width (<u>CLOAD</u>)	t _W (L)	—	2.0	—	175	220
			4.5	—	35	44
			6.0	—	30	37
Minimum set-up time (<u>CCKEN</u> -CCK)	t _s	—	2.0	—	75	95
			4.5	—	15	19
			6.0	—	13	16
Minimum set-up time (RCK- <u>CLOAD</u>)	t _s	—	2.0	—	150	190
			4.5	—	30	38
			6.0	—	26	32
Minimum set-up time (A to H-RCK)	t _s	—	2.0	—	100	125
			4.5	—	20	25
			6.0	—	17	21
Minimum hold time	t _h	—	2.0	—	5	5
			4.5	—	5	5
			6.0	—	5	5
Minimum removal time (<u>CCLR</u>)	t _{rem}	—	2.0	—	75	95
			4.5	—	15	19
			6.0	—	13	16
Minimum removal time (<u>CLOAD</u>)	t _{rem}	—	2.0	—	75	95
			4.5	—	15	19
			6.0	—	13	16
Clock frequency	f	—	2.0	—	4	3.5
			4.5	—	22	18
			6.0	—	26	21

AC Characteristics ($C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	6	12	ns
Propagation delay time (CCK- \overline{RCO})	t_{pLH} t_{pHL}	—	—	25	38	ns
Propagation delay time (RCK- \overline{RCO})	t_{pLH} t_{pHL}	$\overline{CLOAD} = "L"$	—	39	60	ns
Propagation delay time (\overline{CCLR} - \overline{RCO})	t_{pLH}	—	—	24	36	ns
Propagation delay time (\overline{CLOAD} - \overline{RCO})	t_{pLH} t_{pHL}	—	—	35	53	ns
Maximum clock frequency	f_{max}	—	25	35	—	MHz

AC Characteristics ($C_L = 50 \text{ pF}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V _{CC} (V)	Min	Typ.	Max	Min		
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CCK- \overline{RCO})	t_{pLH} t_{pHL}	—	2.0	—	94	220	—	275	ns
			4.5	—	29	44	—	55	
			6.0	—	24	37	—	47	
Propagation delay time (RCK- \overline{RCO})	t_{pLH} t_{pHL}	$\overline{CLOAD} = "L"$	2.0	—	160	340	—	425	ns
			4.5	—	45	68	—	85	
			6.0	—	34	58	—	73	
Propagation delay time (\overline{CCLR} - \overline{RCO})	t_{pLH}	—	2.0	—	89	215	—	270	ns
			4.5	—	28	43	—	54	
			6.0	—	22	37	—	46	
Propagation delay time (\overline{CLOAD} - \overline{RCO})	t_{pLH} t_{pHL}	—	2.0	—	140	300	—	375	ns
			4.5	—	40	60	—	75	
			6.0	—	30	51	—	64	
Maximum clock frequency	f_{max}	—	2.0	4	20	—	3.5	—	MHz
			4.5	22	33	—	18	—	
			6.0	26	49	—	21	—	
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C_{PD} (Note)	—	—	31	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

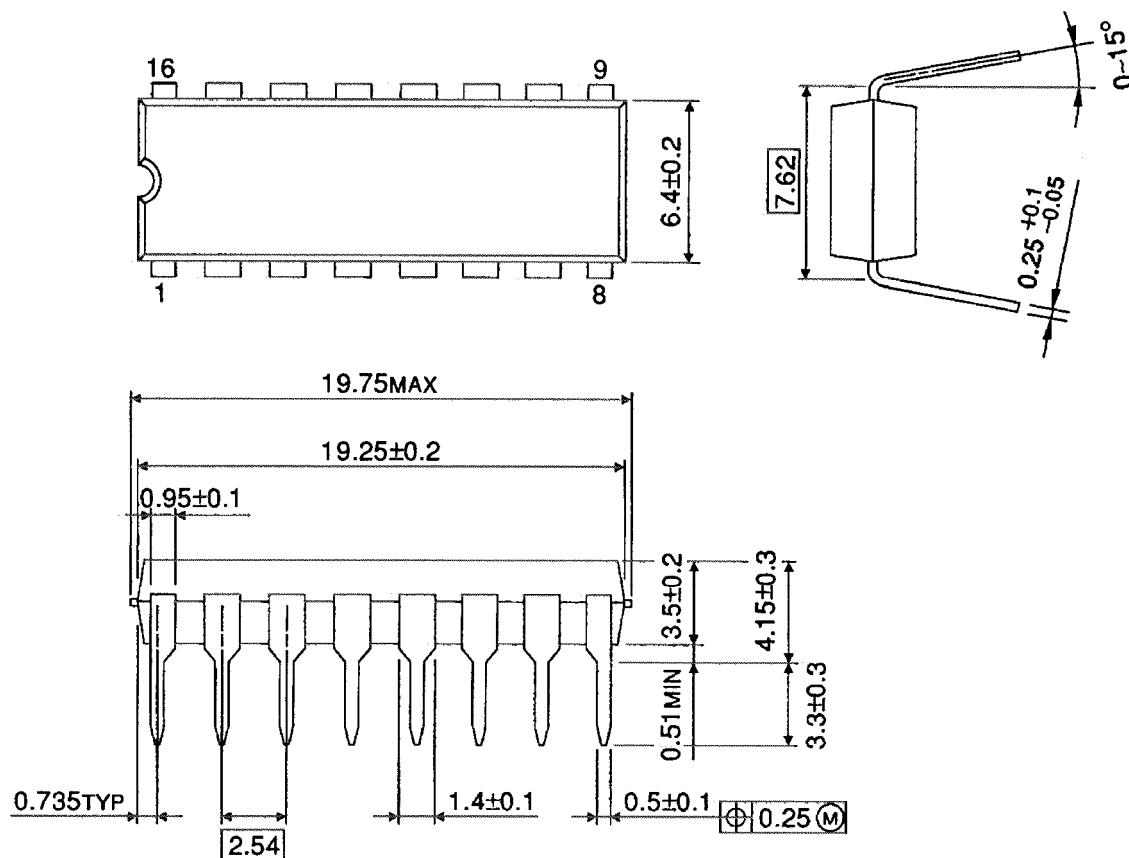
Average operating current can be obtained by the equation:

$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

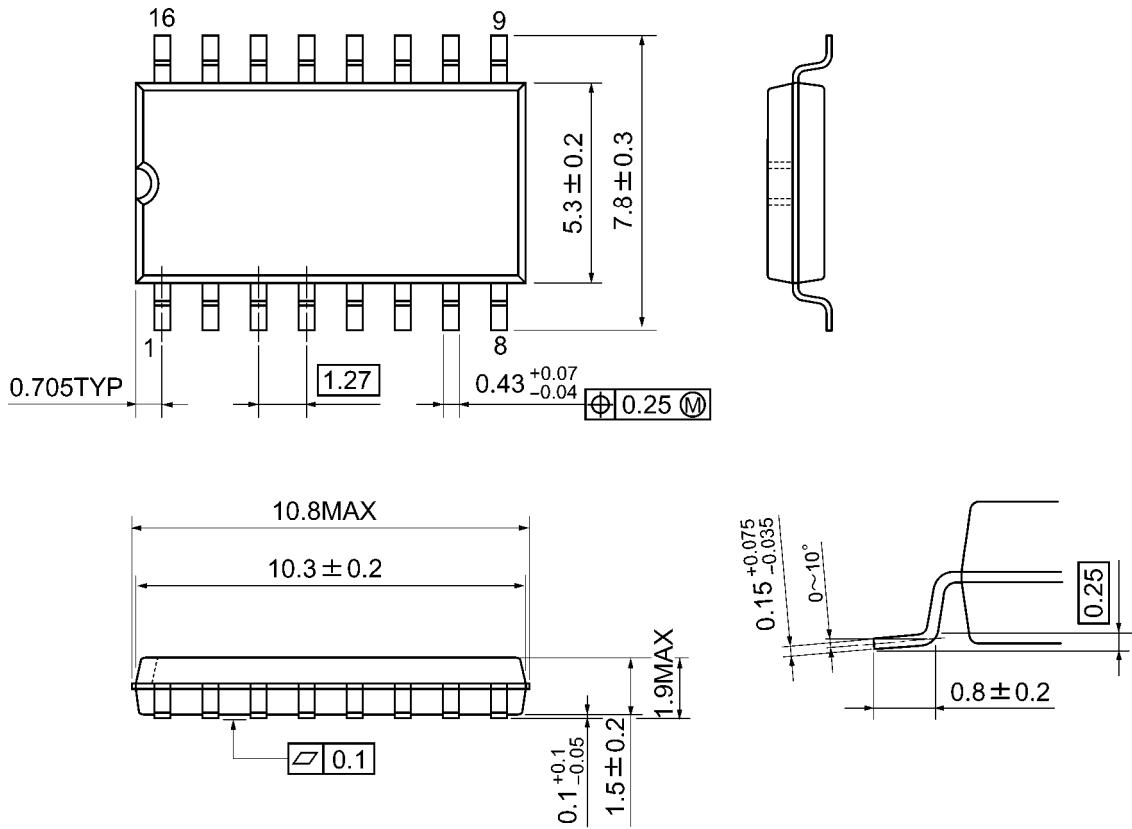


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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