Dual 4-bit binary ripple counter | 74LV393

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Two 4-bit binary counters with individual clocks**
- **Divide-by any binary module up to 28 in one package**
- **Two master resets to clear each 4-bit counter individually**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV393 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT393.

The 74LV393 is a dual 4-bit binary ripple counter with seperate clocks ($1\overline{CP}$, $2\overline{CP}$) and master reset (1MR, 2MR) inputs to each counter.
The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed addres decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.
A HIGH level on the nMR input overides the clock and sets the outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0 nQ to nQ_{n+1} nMR to nQ_n	C_L = 15 pF V_{CC} = 3.3 V	 12 4 11	ns
f_{max}	maximum clock frequency		99	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV393N	14	DIL	plastic	SOT27-1
74LV393D	14	SO	plastic	SOT108-1
74LV393DB	14	SSOP	plastic	SOT337-1
74LV393PW	14	TSSOP	plastic	SOT402-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	$1Q_0$ to $1Q_3$ $2Q_0$ to $2Q_3$	flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

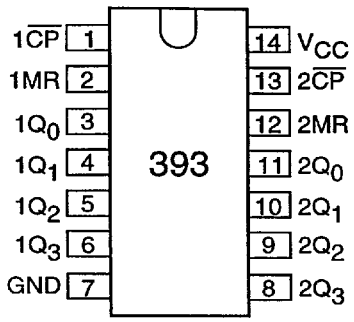

Fig.1 Pin configuration.

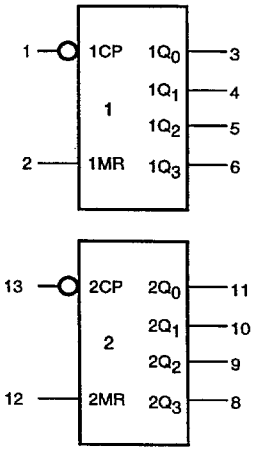

Fig.2 Logic symbol.

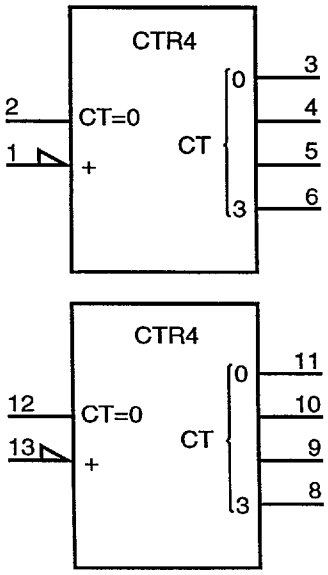

Fig.3 IEC Logic symbol.

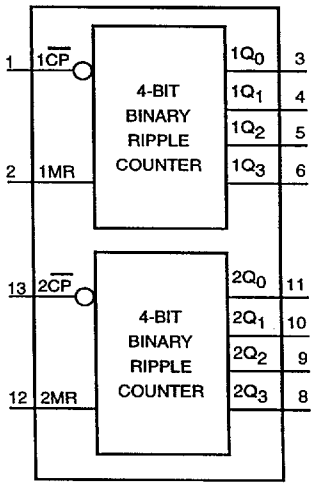

Fig.4 Functional diagram.

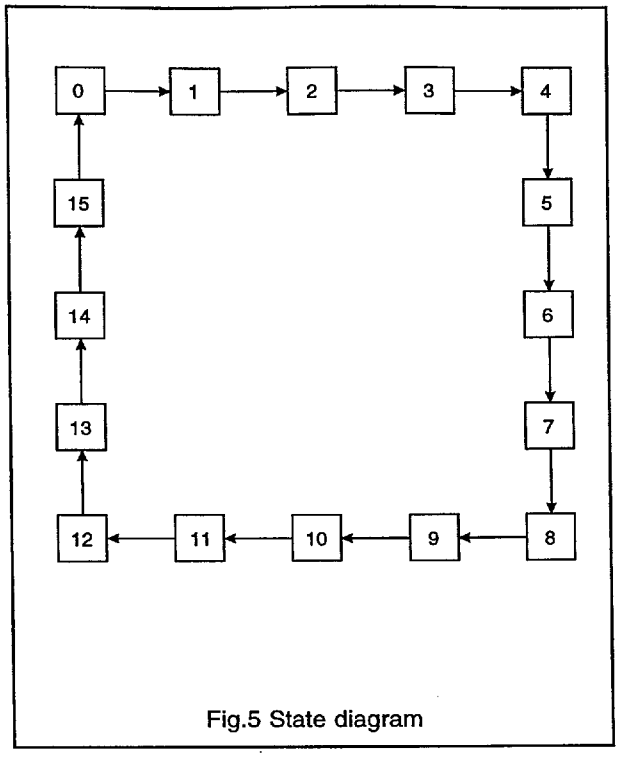

Fig.5 State diagram

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

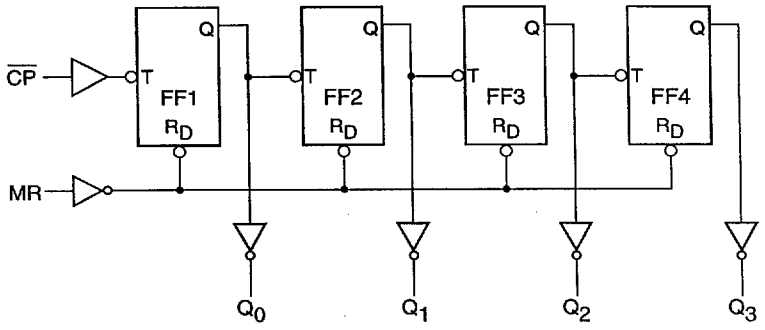

Fig.6 Logic diagram (one counter).

DC CHARACTERISTICS FOR 74LV393

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV393

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0	–	75	–	–	–	ns	1.2	Fig. 7
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay nQ_n to nQ_{n+1}	–	25	–	–	–	ns	1.2	Fig. 7
		–	9	17	–	20		2.0	
		–	6	13	–	15		2.7	
		–	5*	10	–	12		3.0 to 3.6	
t_{PHL}	propagation delay nMR to nQ_n	–	70	–	–	–	ns	1.2	Fig. 8
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig. 7
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width; HIGH	34	12	–	41	–	ns	2.0	Fig. 8
		25	9	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_{rem}	removal time nMR to $n\overline{CP}$	–	5	–	–	–	ns	1.2	Fig. 8
		5	2	–	5	–		2.0	
		5	2	–	5	–		2.7	
		5	1*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	53	–	12	–	MHz	2.0	Fig. 7
		19	72	–	16	–		2.7	
		24	90*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

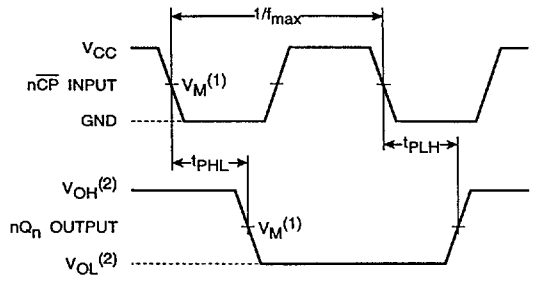

Fig.7 Waveforms showing the clock ($n\overline{CP}$) to output ($1Q_n$, $2Q_n$) propagation delays, the clock pulse width and the maximum clock frequency.

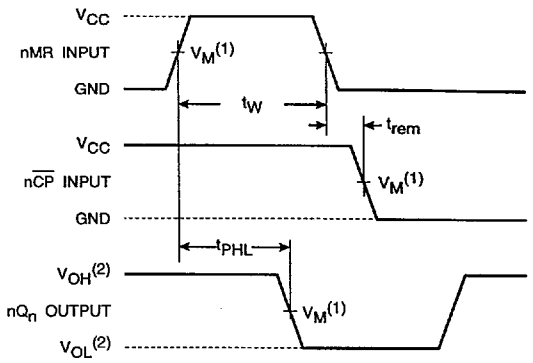

Fig.8 Waveforms showing the master reset (nMR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($n\overline{CP}$) removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.