



# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## General Description

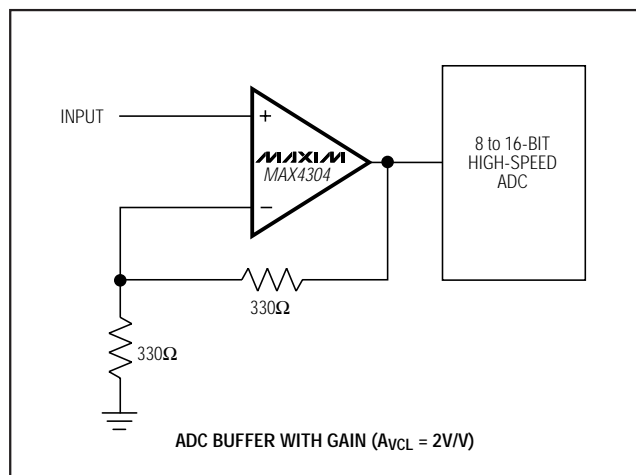
The MAX4104/MAX4105/MAX4304/MAX4305 op amps feature ultra-high speed, low noise, and low distortion in a SOT23 package. The unity-gain-stable MAX4104 requires only 20mA of supply current while delivering 625MHz bandwidth and 400V/ $\mu$ s slew rate. The MAX4304, compensated for gains of +2V/V or greater, delivers a 730MHz bandwidth and a 1000V/ $\mu$ s slew rate. The MAX4105 is compensated for a minimum gain of +5V/V and delivers a 410MHz bandwidth and a 1400V/sec slew rate. The MAX4305 has +10V/V minimum gain compensation and delivers a 340MHz bandwidth and a 1400V/ $\mu$ s slew rate.

Low voltage noise density of 2.1nV/ $\sqrt{\text{Hz}}$  and -88dBc spurious-free dynamic range make these devices ideal for low-noise/low-distortion video and telecommunications applications. These op amps also feature a wide output voltage swing of  $\pm 3.7\text{V}$  and  $\pm 70\text{mA}$  output current-drive capability. For space-critical applications, they are available in a miniature 5-pin SOT23 package.

## Applications

Video ADC Preamplifier  
Pulse/RF Telecom Applications  
Video Buffers and Cable Drivers  
Ultrasound  
Active Filters  
ADC Input Buffers

## Typical Application Circuit



## Features

- ♦ Low 2.1nV/ $\sqrt{\text{Hz}}$  Voltage Noise Density
- ♦ Ultra-High 740MHz -3dB Bandwidth (MAX4304,  $A_{VCL} = 2\text{V/V}$ )
- ♦ 100MHz 0.1dB Gain Flatness (MAX4104/4105)
- ♦ 1400V/ $\mu$ s Slew Rate (MAX4105/4305)
- ♦ -88dBc SFDR (5MHz,  $R_L = 100\Omega$ ) (MAX4104/4304)
- ♦ High Output Current Drive:  $\pm 70\text{mA}$
- ♦ Low Differential Gain/Phase Error: 0.01%/0.01° (MAX4104/4304)
- ♦ Low  $\pm 1\text{mV}$  Input Offset Voltage
- ♦ Available in Space-Saving 5-Pin SOT23 Package

## Selector Guide

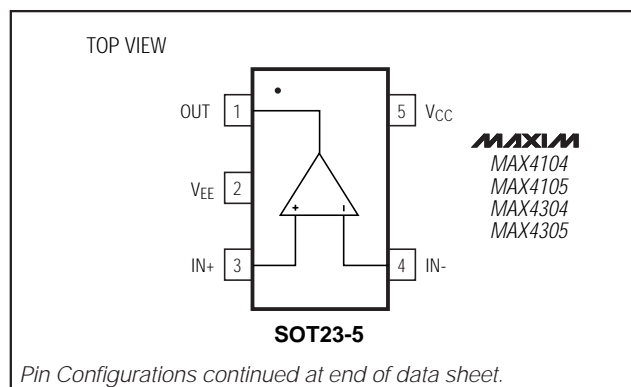
PART	MINIMUM STABLE GAIN (V/V)	BANDWIDTH (MHz)	PIN-PACKAGE
MAX4104	1	625	5-pin SOT23, 8-pin SO
MAX4304	2	740	5-pin SOT23, 8-pin SO
MAX4105	5	410	5-pin SOT23, 8-pin SO
MAX4305	10	340	5-pin SOT23, 8-pin SO

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4104ESA	-40°C to +85°C	8 SO	—
MAX4104EUK-T	-40°C to +85°C	5 SOT23-5	ACCO

Ordering Information continued at end of data sheet.

## Pin Configurations



MAX4104/MAX4105/MAX4304/MAX4305



# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ( $V_{CC}$  to  $V_{EE}$ ) ..... +12V  
 Voltage on Any Pin to Ground ..... ( $V_{EE} - 0.3V$ ) to ( $V_{CC} + 0.3V$ )  
 Short-Circuit Duration ( $V_{OUT}$  to GND) ..... Continuous  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     5-pin SOT23 (derate 7.1mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 571mW  
     8-pin SO (derate 5.9mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 471mW

Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (soldering, 10sec) .....  $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $V_{CM} = 0$ ,  $R_L = 100k\Omega$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V <sub>CC</sub> /V <sub>EE</sub>	Guaranteed by PSRR test		±3.5	±5	±5.5	V
Input Offset Voltage	V <sub>OS</sub>	V <sub>OUT</sub> = 0	MAX4_0_ESA	1		6	mV
			MAX4_0_EUK	1		8	
Input Offset-Voltage Drift	TCV <sub>OS</sub>			2.5			μV/°C
Input Bias Current	I <sub>B</sub>			32		70	μA
Input Offset Current	I <sub>OS</sub>			0.5		5.0	μA
Differential Input Resistance	R <sub>IN</sub>	-0.8V ≤ V <sub>IN</sub> ≤ 0.8V		6			kΩ
Common-Mode Input Resistance	R <sub>IN</sub>	Either input		1.5			MΩ
Input Common-Mode Voltage Range	V <sub>CM</sub>	Guaranteed by CMRR test		-2.8		+4.1	V
Common-Mode Rejection Ratio	CMRR	-2.8V ≤ V <sub>CM</sub> ≤ 4.1V		80	95		dB
Positive Power-Supply Rejection Ratio	PSSR+	V <sub>CC</sub> = 3.5V to 5.5V		75	85		dB
Negative Power-Supply Rejection Ratio	PSRR-	V <sub>EE</sub> = -3.5V to -5.5V		55	65		dB
Quiescent Supply Current	I <sub>S</sub>	V <sub>OUT</sub> = 0		20		27	mA
Open-Loop Gain	A <sub>VOL</sub>	-2.8V ≤ V <sub>OUT</sub> ≤ 2.8V, R <sub>L</sub> = 100Ω		55	65		dB
Output Voltage Swing	V <sub>OUT</sub>	R <sub>L</sub> = 100kΩ		±3.5		-3.7 to +3.8	V
		R <sub>L</sub> = 100Ω		±3.0		-3.5 to +3.4	
Output Current Drive	I <sub>OUT</sub>	R <sub>L</sub> = 30Ω		±53	±70		mA
Short-Circuit Output Current	I <sub>SC</sub>	R <sub>L</sub> = short to ground		80			mA
Open-Loop Output Impedance	Z <sub>OUT</sub>			9			Ω

# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $V_{CM} = 0$ ,  $R_L = 100\Omega$ ;  $A_V = +1V/V$  for MAX4104,  $+2V/V$  for MAX4304,  $+5V/V$  for MAX4105,  $+10V/V$  for MAX4305;  $T_A = +25^\circ C$ ; unless otherwise noted.)

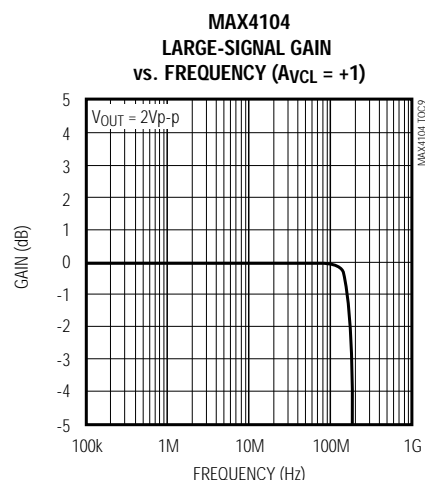
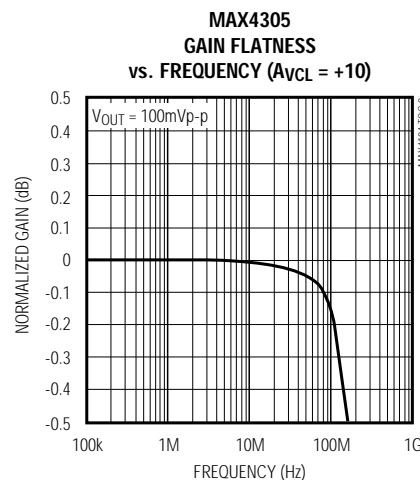
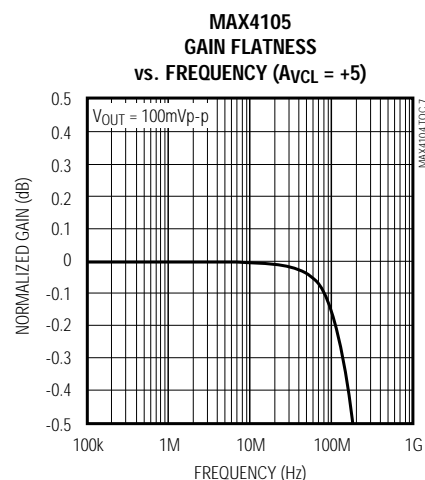
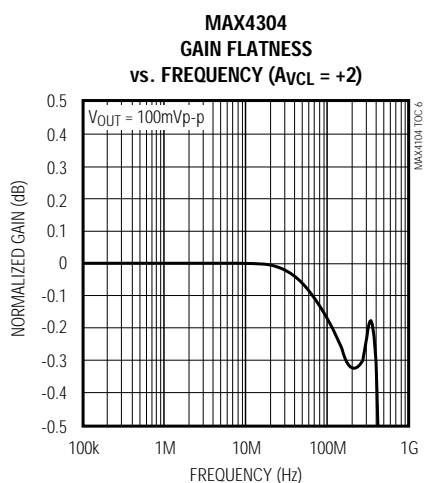
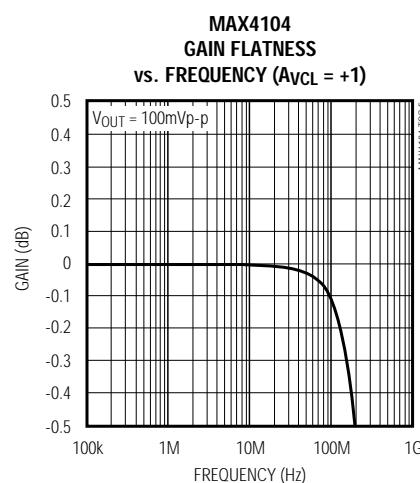
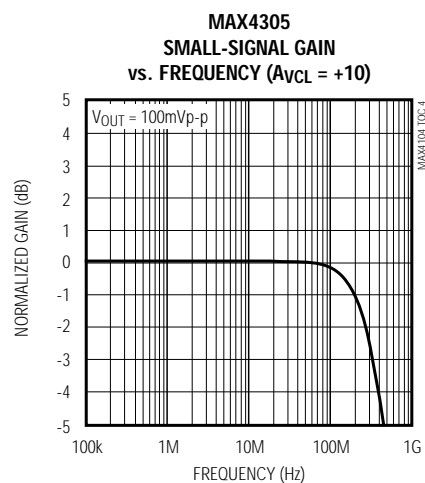
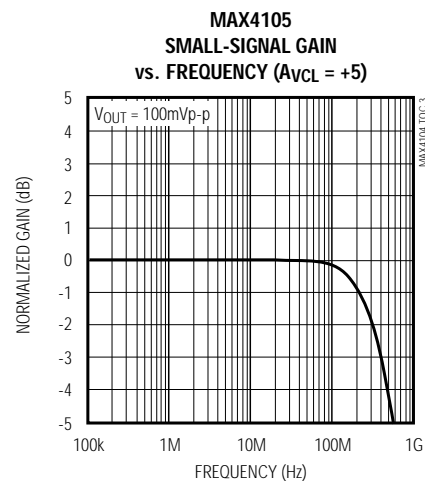
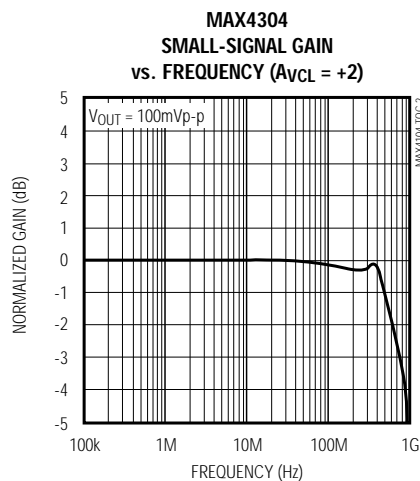
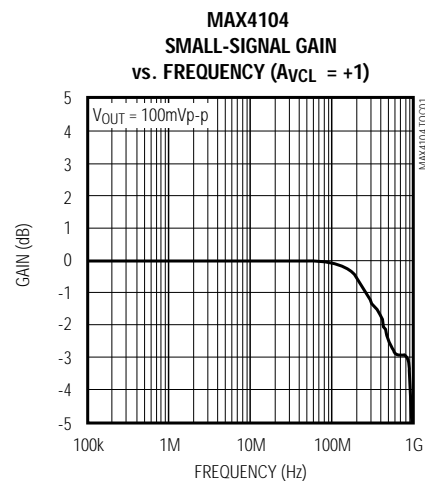
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
-3dB Bandwidth	$BW_{(-3dB)}$	$V_{OUT} = 100mVp-p$	MAX4104		625		MHz
			MAX4304		740		
			MAX4105		410		
			MAX4305		340		
0.1dB Bandwidth	$BW_{(0.1)}$	$V_{OUT} = 100mVp-p$	MAX4104		100		MHz
			MAX4304		60		
			MAX4105		80		
			MAX4305		70		
Full-Power Bandwidth	FPBW	$V_{OUT} = 2Vp-p$	MAX4104		115		MHz
			MAX4304		285		
			MAX4105		370		
			MAX4305		320		
Slew Rate	SR	$V_{OUT} = 2Vp-p$	MAX4104		400		$V/\mu s$
			MAX4304		1000		
			MAX4105		1400		
			MAX4305		1400		
Settling Time to 0.1%	$t_s$	$V_{OUT} = 2Vp-p$	to 0.1%		20		ns
			to 0.01%		25		
Spurious-Free Dynamic Range	SFDR	$V_{OUT} = 2Vp-p$	MAX4104/ MAX4304	$f_C = 5MHz$	-88		dBc
				$f_C = 20MHz$	-67		
			MAX4105/ MAX4305	$f_C = 5MHz$	-74		
				$f_C = 20MHz$	-61		
Differential Gain Error	DG	NTSC, $R_L = 150\Omega$	MAX4104/MAX4304		0.01		%
			MAX4105/MAX4305		0.02		
Differential Phase Error	DP	NTSC, $R_L = 150\Omega$	MAX4104/MAX4304		0.01		degrees
			MAX4105/MAX4305		0.02		
Input Voltage Noise Density	$e_n$	$f = 1MHz$			2.1		$nV/\sqrt{Hz}$
Input Current Noise Density	$i_n$	$f = 1MHz$			3.1		$pA/\sqrt{Hz}$
Output Impedance	$Z_{OUT}$	$f = 10MHz$			1		$\Omega$

MAX4104/MAX4105/MAX4304/MAX4305

# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## Typical Operating Characteristics

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $R_F = 330\Omega$ ,  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

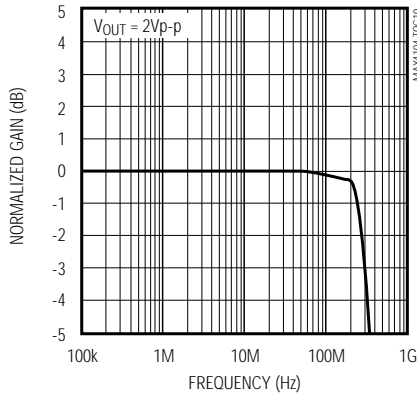


# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

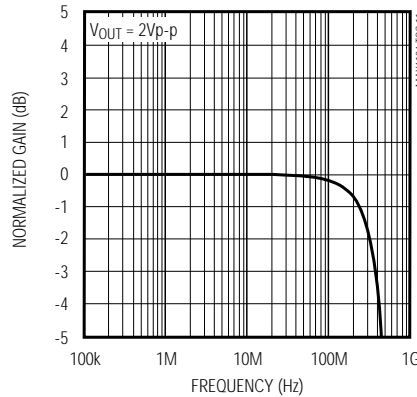
## Typical Operating Characteristics (continued)

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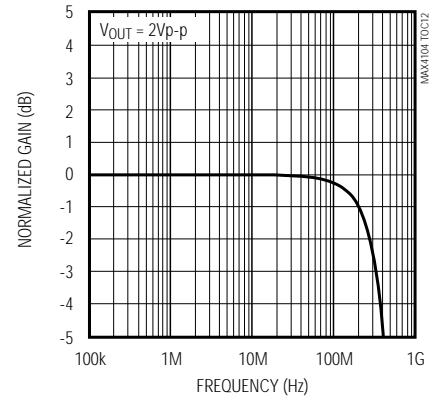
**MAX4304**  
LARGE-SIGNAL GAIN  
vs. FREQUENCY ( $A_{VCL} = +2$ )



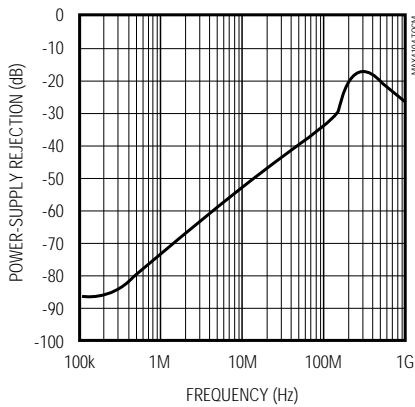
**MAX4105**  
LARGE-SIGNAL GAIN  
vs. FREQUENCY ( $A_{VCL} = +5$ )



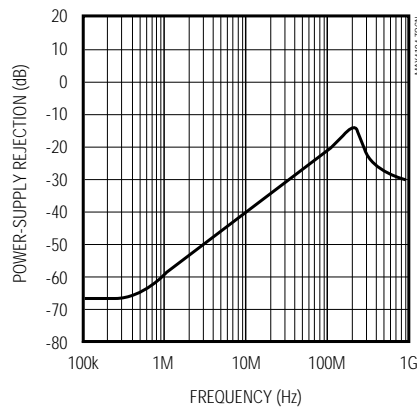
**MAX4305**  
LARGE-SIGNAL GAIN  
vs. FREQUENCY ( $A_{VCL} = +10$ )



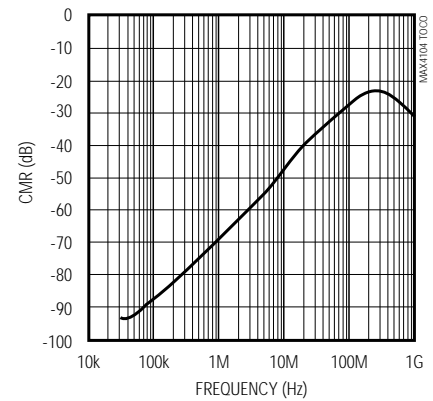
**POSITIVE POWER-SUPPLY REJECTION**  
vs. FREQUENCY



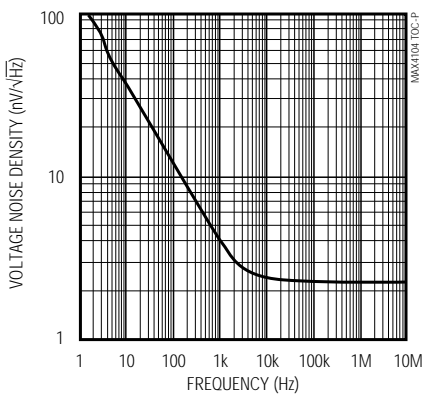
**NEGATIVE POWER-SUPPLY REJECTION**  
vs. FREQUENCY



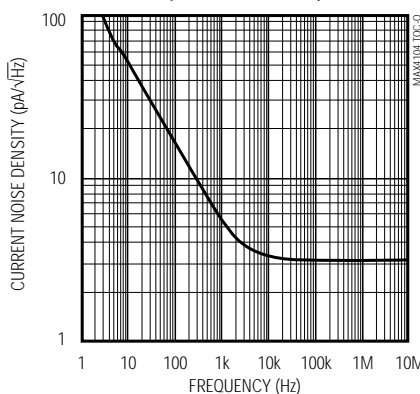
**COMMON-MODE REJECTION**  
vs. FREQUENCY



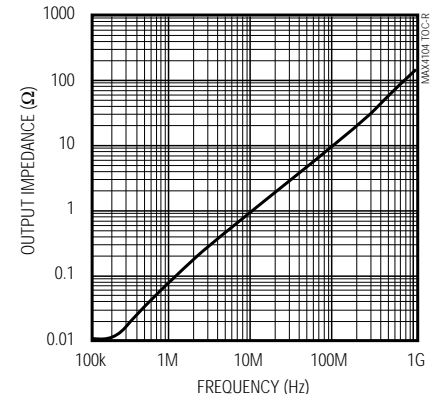
**VOLTAGE NOISE DENSITY vs. FREQUENCY**  
(INPUT REFERRED)



**CURRENT NOISE DENSITY vs. FREQUENCY**  
(INPUT REFERRED)



**CLOSED-LOOP OUTPUT IMPEDANCE**  
vs. FREQUENCY

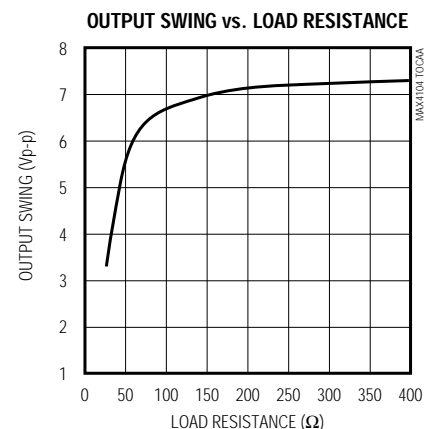
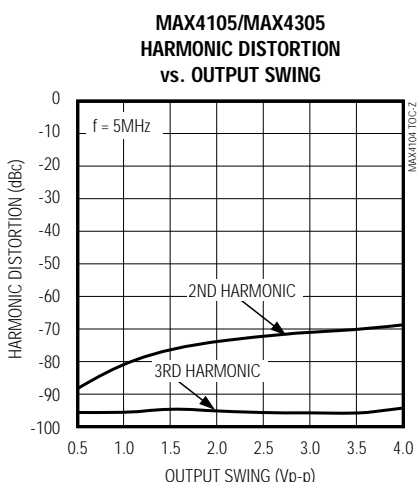
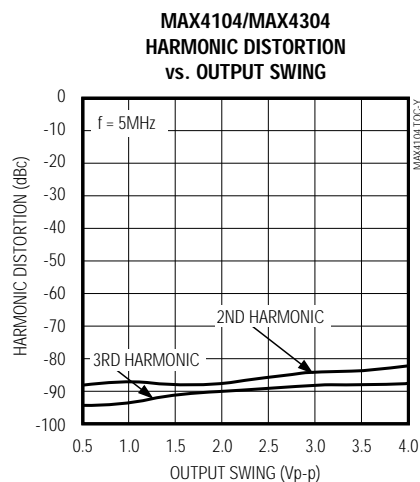
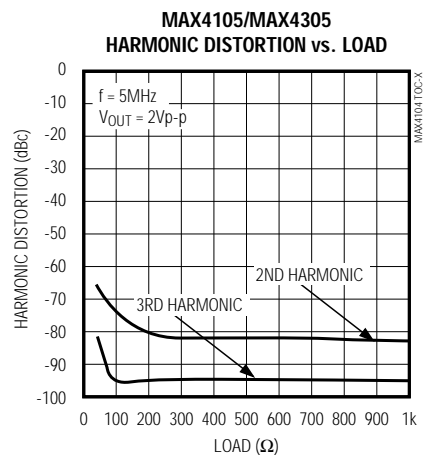
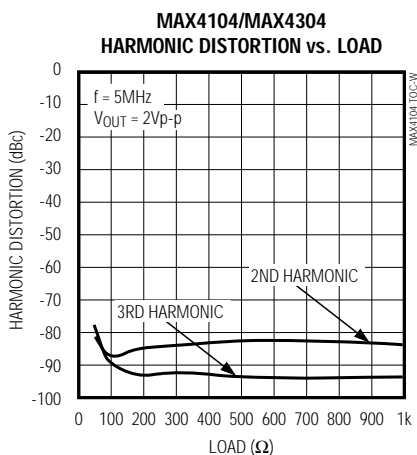
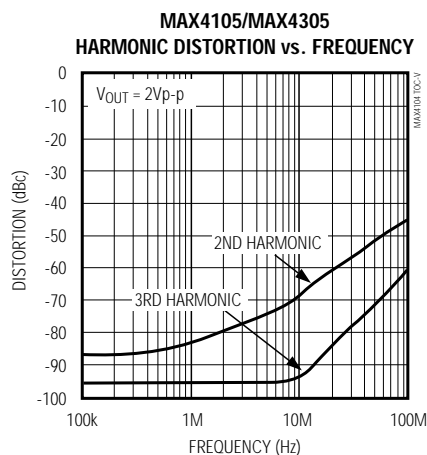
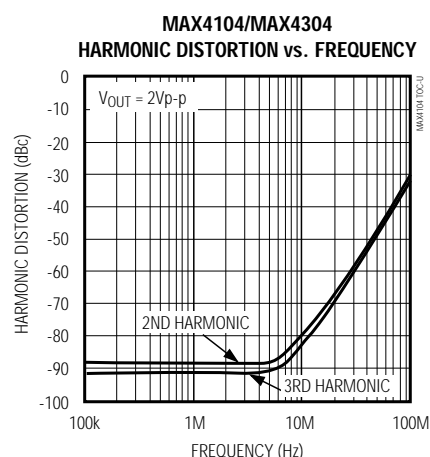
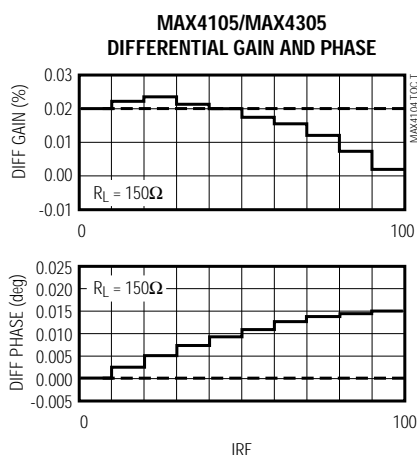
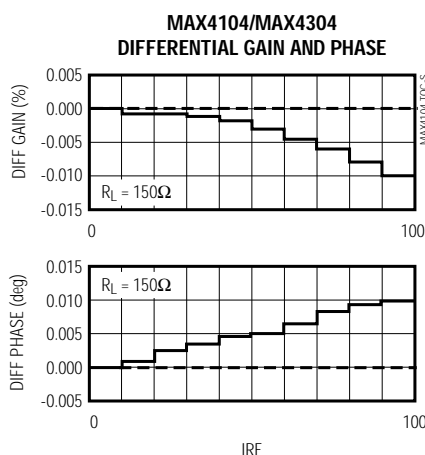


MAX4104/MAX4105/MAX4304/MAX4305

# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## Typical Operating Characteristics (continued)

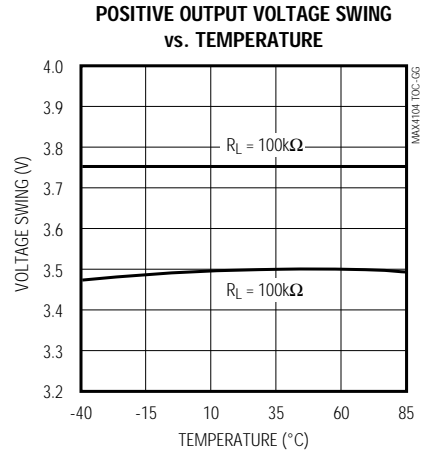
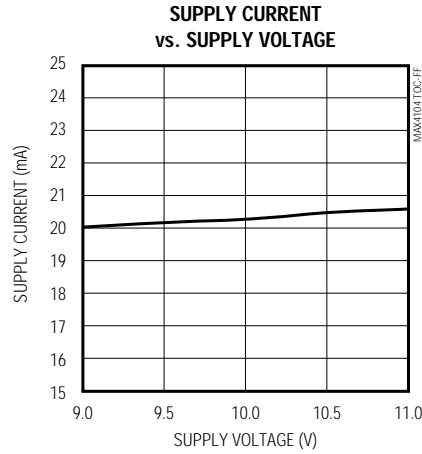
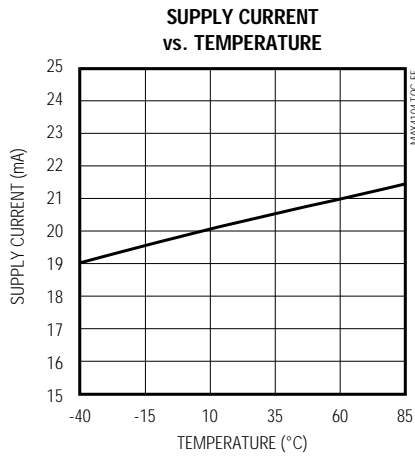
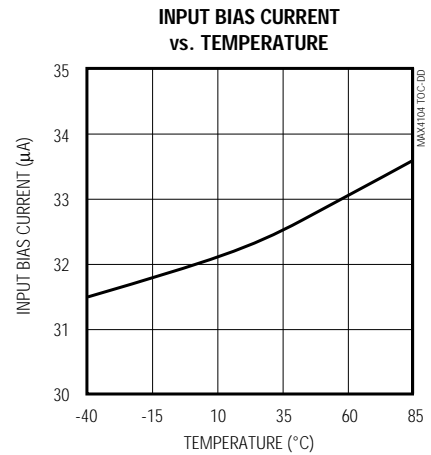
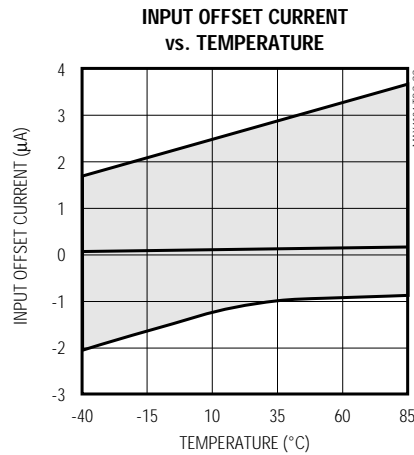
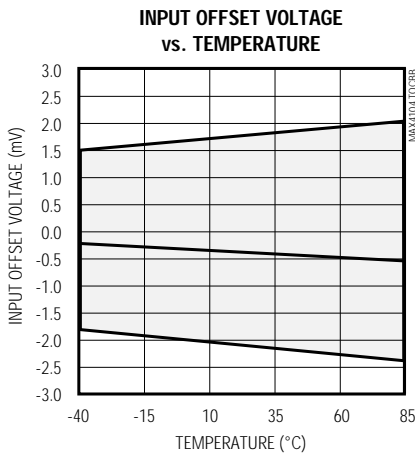
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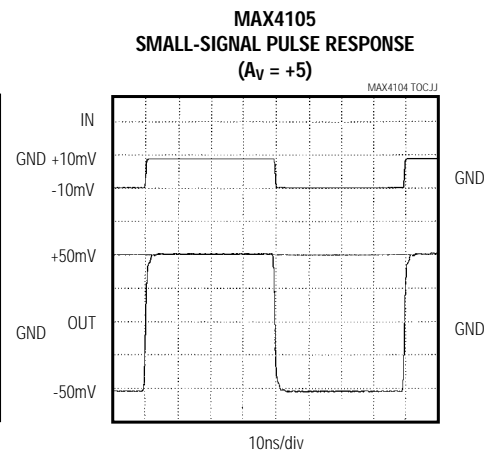
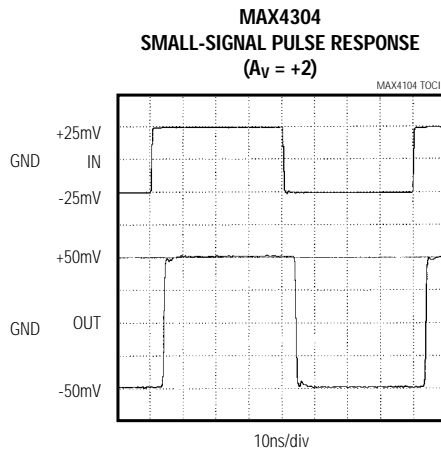
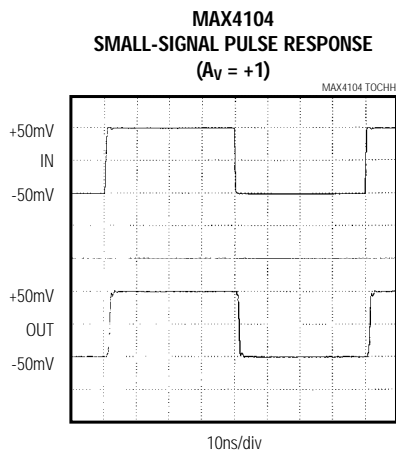
# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## Typical Operating Characteristics (continued)

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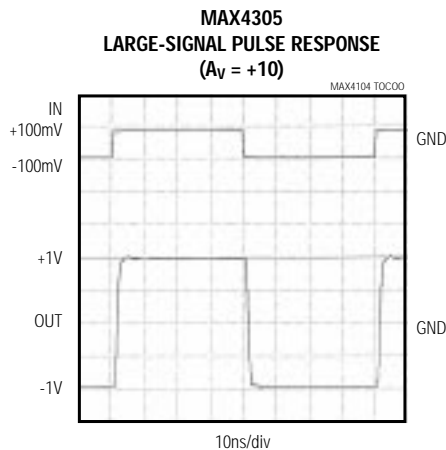
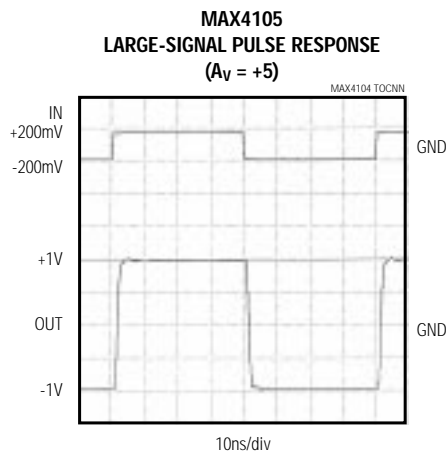
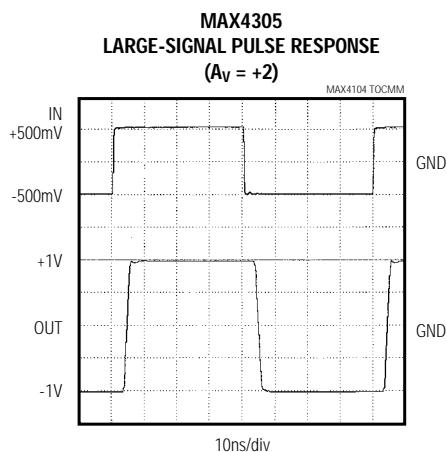
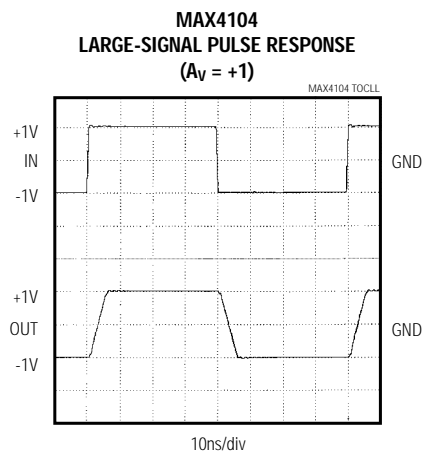
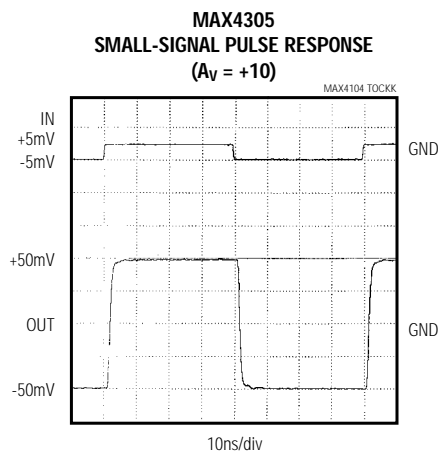
MAX4104/MAX4105/MAX4304/MAX4305



# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## Typical Operating Characteristics (continued)

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# 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

## Pin Description

PIN		NAME	FUNCTION
SOT23-5	SO		
—	1, 5, 8	N.C.	Not internally connected.
4	2	IN-	Amplifier Inverting Input
3	3	IN+	Amplifier Noninverting Input
2	4	VEE	Negative Power Supply
1	6	OUT	Amplifier Output
5	7	VCC	Positive Power Supply

## Detailed Description

The MAX4104/MAX4105/MAX4304/MAX4305 are ultra-high-speed, low-noise amplifiers featuring -3dB bandwidths up to 880MHz, 0.1dB gain flatness up to 100MHz, and low differential gain and phase errors of 0.01% and 0.01°, respectively. These devices operate on dual power supplies ranging from  $\pm 3.5\text{V}$  to  $\pm 5.5\text{V}$  and require only 20mA of supply current.

The MAX4104/MAX4304/MAX4105/MAX4305 are optimized for minimum closed-loop gains of +1V/V, +2V/V, +5V/V and +10V/V (respectively) with corresponding -3dB bandwidths of 880MHz, 730MHz, 430MHz, and 350MHz. Each device in this family features a low input voltage noise density of only 2.1nV/ $\sqrt{\text{Hz}}$  (at 1MHz), an output current drive of  $\pm 70\text{mA}$ , and spurious-free dynamic range as low as -88dBc (5MHz,  $R_L = 100\Omega$ ).

## Applications Information

### Layout and Power-Supply Bypassing

The MAX4104/MAX4105/MAX4304/MAX4305 have an extremely high bandwidth, and consequently require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Regardless of whether or not a constant-impedance board is used, it is best to observe the following guidelines when designing the board:

- 1) Do not use wire-wrapped boards (they are much too inductive) or breadboards (they are much too capacitive).
- 2) Do not use IC sockets. IC sockets increase reactances.
- 3) Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- 4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
- 5) Bear in mind that, in general, surface-mount components have shorter bodies and lower parasitic reactance, resulting in greatly improved high-frequency performance over through-hole components.

The bypass capacitors should include 1nF and 0.1 $\mu\text{F}$  ceramic surface-mount capacitors between each supply pin and the ground plane, located as close to the package as possible. Optionally, place a 10 $\mu\text{F}$  tantalum capacitor at the power supply pins' point of entry to the PC board to ensure the integrity of incoming supplies. The power-supply trace should lead directly from the tantalum capacitor to the VCC and VEE pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components.

Input termination resistors and output back-termination resistors, if used, should be surface-mount types, and should be placed as close to the IC pins as possible.

### DC and Noise Errors

The MAX4104/MAX4105/MAX4304/MAX4305 output offset voltage,  $V_{OUT}$  (Figure 1), can be calculated with the following equation:

$$V_{OUT} = [V_{OS} + (I_{B+} \times R_S) + (I_{B-} \times (R_F \parallel R_G))] [1 + R_F / R_G]$$

where:

$V_{OS}$  = input offset voltage (in volts)

$1 + R_F/R_G$  = amplifier closed-loop gain (dimensionless)

$I_{B+}$  = noninverting input bias current (in amps)

$I_{B-}$  = inverting input bias current (in amps)

$R_G$  = gain-setting resistor (in ohms)

$R_F$  = feedback resistor (in ohms)

$R_S$  = source resistor at noninverting input (in ohms)

The following equation represents output noise density:

$$e_{n(OUT)} = \left[ 1 + \frac{R_F}{R_G} \right] \sqrt{(i_n \times R_S)^2 + [i_n \times (R_F \parallel R_G)]^2} + e_n^2$$

## 740MHz, Low-Noise, Low-Distortion Op Amps in SOT23-5

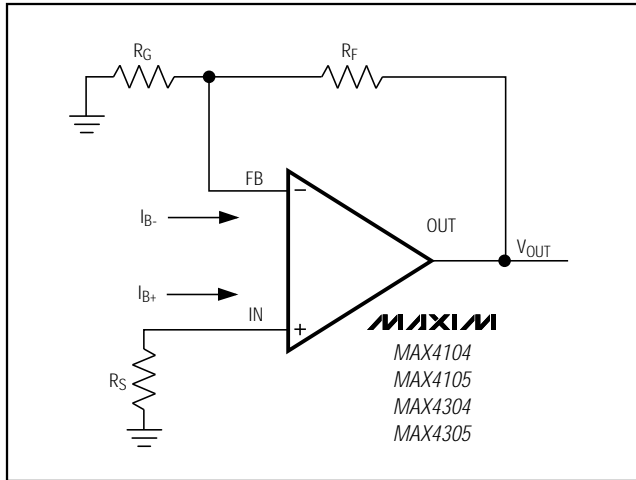


Figure 1. Output Offset Voltage

where:

$i_n$  = input current noise density (in  $\text{pA}/\sqrt{\text{Hz}}$ )

$e_n$  = input voltage noise density (in  $\text{nV}/\sqrt{\text{Hz}}$ )

The MAX4104/MAX4105/MAX4304/MAX4305 have a very low,  $2.1\text{nV}/\sqrt{\text{Hz}}$  input voltage noise density and  $3.1\text{pA}/\sqrt{\text{Hz}}$  input current noise density.

An example of DC-error calculations, using the MAX4304 typical data and the typical operating circuit with  $R_F = R_G = 330\Omega$  ( $R_F \parallel R_G = 165\Omega$ ) and  $R_S = 50\Omega$  gives:

$$V_{OUT} = \left[ (32 \times 10^{-6})(50) + (32 \times 10^{-6})(165) + 1 \times 10^{-3} \right] [1 + 1]$$

$$V_{OUT} = 15.8\text{mV}$$

Calculating total output noise in a similar manner yields the following:

$$e_{n(OUT)} = [1 + 1] \sqrt{(3.1 \times 10^{-12} \times 50)^2 + (3.1 \times 10^{-12} \times 165)^2 + (2.1 \times 10^{-9})^2}$$

$$e_{n(OUT)} = 4.3\text{nV}/\sqrt{\text{Hz}}$$

With a 200MHz system bandwidth, this calculates to  $60.8\mu\text{VRMS}$  (approximately  $365\mu\text{Vp-p}$ , using the six-sigma calculation).

### ADC Input Buffers

Input buffer amplifiers can be a source of significant error in high-speed ADC applications. The input buffer is usually required to rapidly charge and discharge the ADC's input, which is often capacitive. In addition, the input impedance of a high-speed ADC often changes

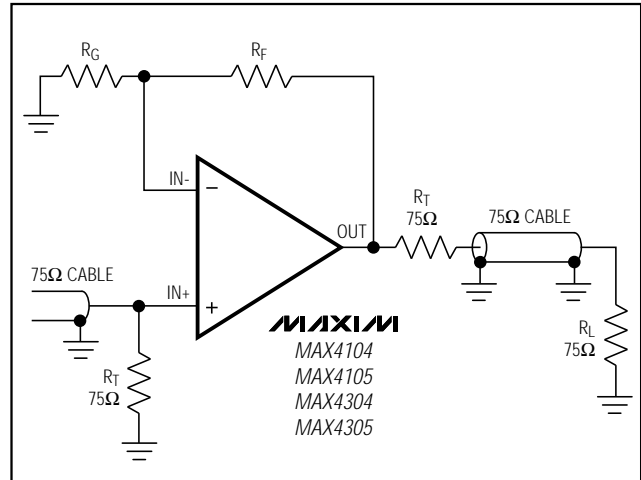


Figure 2. Video Line Driver

very rapidly during the conversion cycle—a condition that demands an amplifier with very low output impedance at high frequencies to maintain measurement accuracy. The combination of high-speed, fast slew rate, low noise, and low-distortion available in the MAX4104/MAX4105/MAX4304/MAX4305 makes them ideally suited for use as buffer amplifiers in high-speed ADC applications.

### Video Line Driver

The MAX4104/MAX4105/MAX4304/MAX4305 are optimized to drive coaxial transmission lines when the cable is terminated at both ends, as shown in Figure 2. To minimize reflections and maximize power transfer, select the termination resistors to match the characteristic impedance of the transmission line. Cable frequency response can cause variations in the flatness of the signal.

### Driving Capacitive Loads

The MAX4104/MAX4105/MAX4304/MAX4305 provide maximum AC performance when driving no output load capacitance. This is the case when driving a correctly terminated transmission line (i.e., a back-terminated cable).

In most amplifier circuits, driving a large load capacitance increases the chance of oscillations occurring. The amplifier's output impedance and the load capacitor combine to add a pole and excess phase to the loop response. If the pole's frequency is low enough and phase margin is degraded sufficiently, oscillations may result.

A second concern when driving capacitive loads originates from the amplifier's output impedance, which

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MAX4104/MAX4105/MAX4304/MAX4305

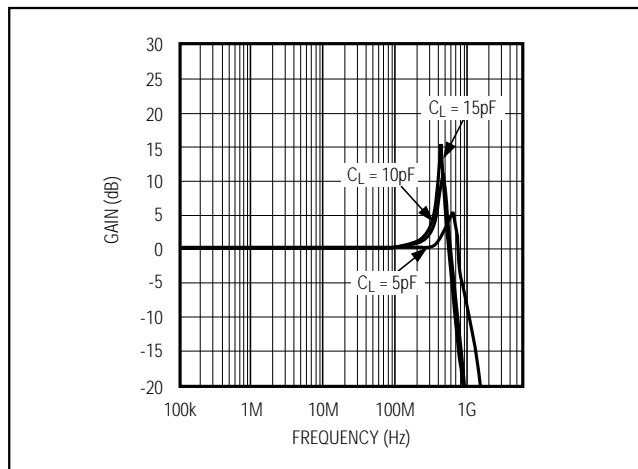


Figure 3a. MAX4104 Frequency Response with Capacitive Load and No Isolation Resistor

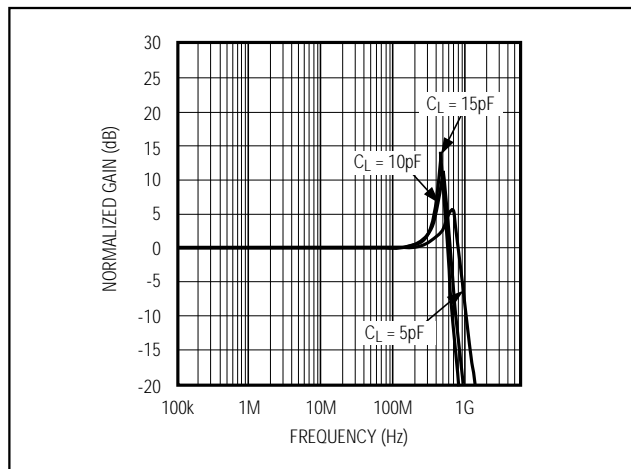


Figure 3b. MAX4304 Frequency Response with Capacitive Load and No Isolation Resistor

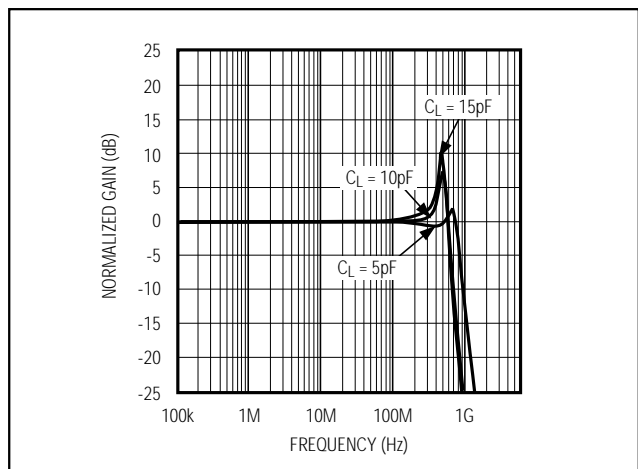


Figure 3c. MAX4105 Frequency Response with Capacitive Load and No Isolation Resistor

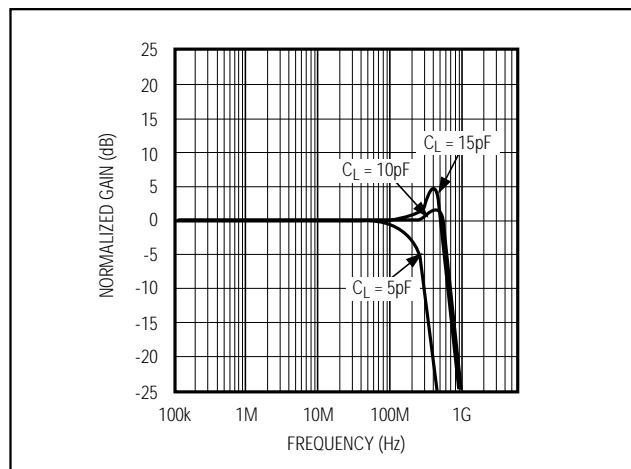


Figure 3d. MAX4305 Frequency Response with Capacitive Load and No Isolation Resistor

appears inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's phase margin.

The MAX4104/MAX4105/MAX4304/MAX4305 drive capacitive loads up to 10pF without oscillation. However, some peaking may occur in the frequency domain (Figure 3). To drive larger capacitance loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load (Figure 4).

The value of  $R_{ISO}$  depends on the circuit's gain and the capacitive load (Figure 5). Figure 6 shows the MAX4104/MAX4105/MAX4304/MAX4305 frequency response with the isolation resistor and a capacitive

load. With higher capacitive values, bandwidth is dominated by the RC network formed by  $R_{ISO}$  and  $C_L$ ; the bandwidth of the amplifier itself is much higher. Also note that the isolation resistor forms a divider that decreases the voltage delivered to the load.

## Maxim's High-Speed Evaluation Boards

The MAX4104 evaluation kit manual shows a suggested layout for Maxim's high-speed, single-amplifier evaluation boards. This board was developed using the techniques described previously (see *Layout and Power-Supply Bypassing* section). The smallest available surface-mount resistors were used for the feedback and back-termination resistors to minimize the

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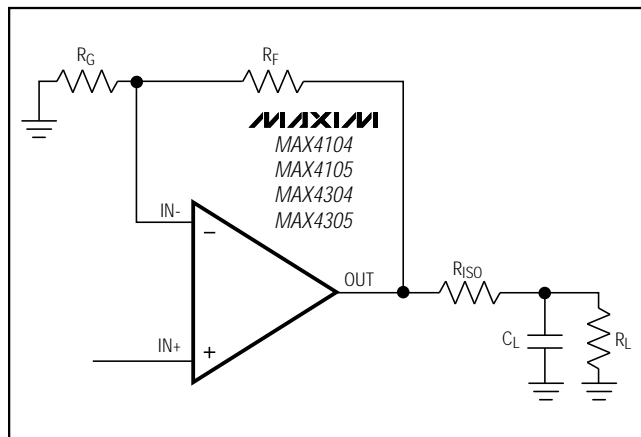


Figure 4. Using an Isolation Resistor ( $R_{ISO}$ ) for High Capacitive Loads

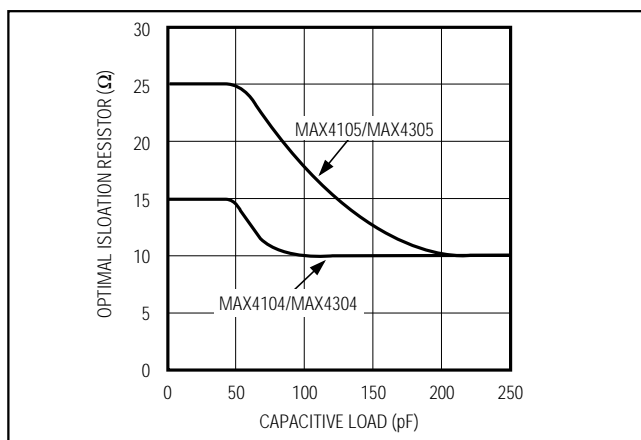


Figure 5. Optimal Isolation Resistor ( $R_{ISO}$ ) vs. Capacitive Load

## Pin Configurations (continued)

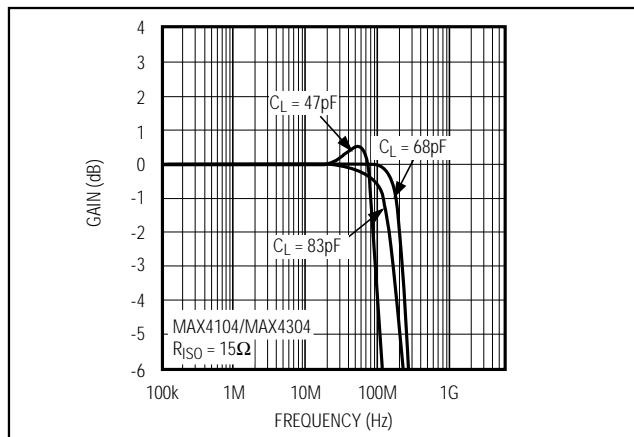
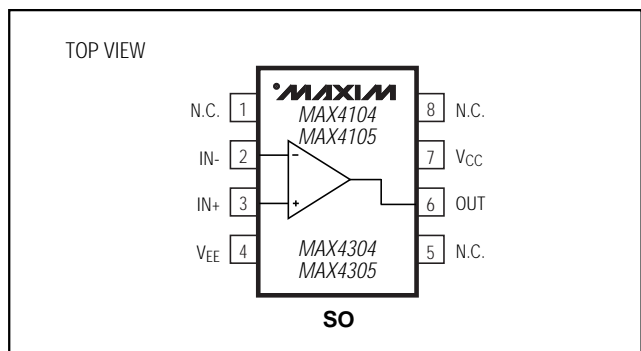


Figure 6. Frequency Responses vs. Capacitive Load with  $15\Omega$  Isolation Resistor

distance from the IC to these resistors, thus reducing the capacitance associated with longer lead lengths.

SMA connectors were used for best high-frequency performance. Because distances are extremely short, performance is unaffected by the fact that inputs and outputs do not match a  $50\Omega$  line. However, in applications that require lead lengths greater than  $1/4$  of the wavelength of the highest frequency of interest, constant-impedance traces should be used.

Fully assembled evaluation boards are available for the MAX4104 in an 8-pin SO package.

## Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
<b>MAX4105</b> ESA	-40°C to +85°C	8 SO	—
MAX4105EUK-T	-40°C to +85°C	5 SOT23-5	ACCP
<b>MAX4304</b> ESA	-40°C to +85°C	8 SO	—
MAX4304EUK-T	-40°C to +85°C	5 SOT23-5	ACCQ
<b>MAX4305</b> ESA*	-40°C to +85°C	8 SO	—
MAX4305EUK-T	-40°C to +85°C	5 SOT23-5	ACCR

\*Future product—contact factory for availability.

## Chip Information

TRANSISTOR COUNT: 44

SUBSTRATE CONNECTED TO  $V_{EE}$