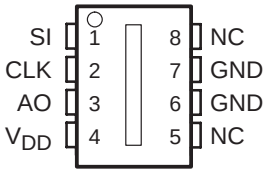
- **128 × 1 Sensor-Element Organization**
- **400 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity for 256 Gray-Scale (8-Bit) Applications**
- **Output Referenced to Ground**
- **Low Image Lag (0.5% Typical)**
- **Operation to 2 MHz**
- **Single 5-V Supply**

(TOP VIEW)

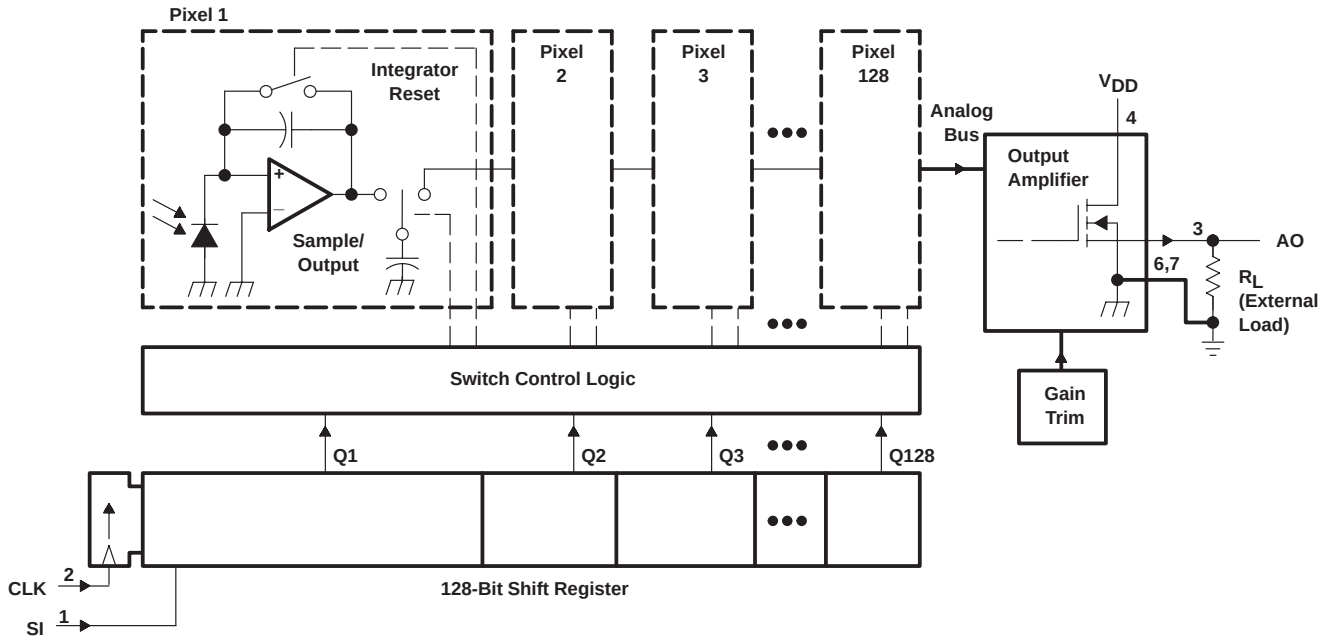


NC − No internal connection

description

The TSL401 linear sensor array consists of a 128 × 1 array of photodiodes and associated charge amplifier circuitry. The pixels measure 63.5 µm (H) × 50 µm (W) with 63.5-µm center-to-center spacing and 13.5 µm between pixels. Operation is simplified by internal logic requiring only a serial input (SI) signal and a clock.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
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Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	3	Analog output
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
NC	5, 8	No internal connection
SI	1	Serial input. This input defines the start of the data-out sequence.
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.

detailed description

The sensor consists of 128 photodiode pixels, arranged in a linear array. Light energy striking a pixel generates photocurrent, which is then integrated. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and the integration time. The integration time is the interval between two consecutive output periods.

A 128-bit shift register controls the output period of the device. An output period is initiated by applying a logic level 1 to SI for one positive-going clock edge (see Figure 1). This logic one is clocked through a 128-bit shift register, in which one bit is associated with each pixel. When a given bit is high, the associated pixel signal is coupled to the analog output (AO) through an output amplifier. When the bit goes low, the integrator is reset.

AO is a source follower that requires an external pulldown resistor. The source-follower configuration permits an analog wired-OR hookup of multiple devices. When the device is not in the output phase, the output is in a high-impedance state. The output is nominally 0 V for no light input and 2 V for a nominal full-scale output.

The TSL401 is intended for use in a wide variety of applications, including mark and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning, and optical linear and rotary encoding.

absolute maximum ratings†

Supply voltage, V_{DD} . . . . . 7 V
Digital input current range, I_I . . . . . −20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Figures 1 and 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ	565		700	nm
Clock frequency, f_{clock}	5		2000	kHz
Sensor integration time, t_{int}	0.0645		100	ms
Setup time, serial input, $t_{su(SI)}$	0			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 1)	20			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

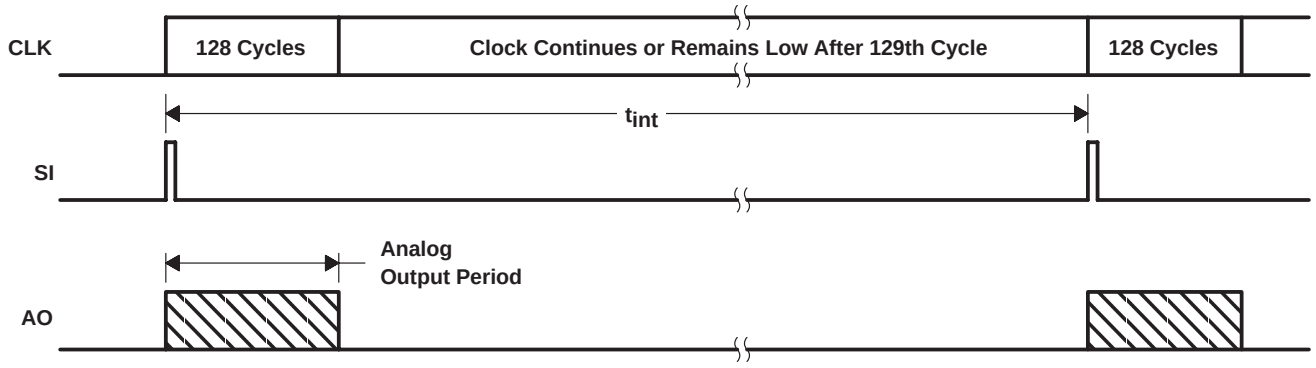


Figure 1. Timing Waveforms

electrical characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 565 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 20 μW/cm² (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Analog output voltage (white, average over 128 pixels)		1.8	2	2.2	V
	Analog output voltage (dark, each pixel)	E_e = 0	0	0.15	0.3	V
PRNU	Pixel response nonuniformity	See Note 3		±5%	±7.5%	
	Linearity of analog output voltage	See Note 4		±0.4%		F.S.
	Output noise voltage	See Note 5		1		mVrms
	Saturation exposure		136	175		nJ/cm²
	Analog output saturation voltage		3	3.5		V
I_{DD}	Supply current			2.5	4	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			1	μA
I_{IL}	Low-level input current	V_I = 0			1	μA
C_i	Input capacitance			5		pF

NOTES: 2. Clock duty cycle is assumed to be 50%.
3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. Peak-to-peak noise is the variation of a single-pixel output under constant illumination as observed over a 5-second period.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(H)}$	Clock pulse duration (high)		50			ns
$t_{w(L)}$	Clock pulse duration (low)		50			ns
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		350		ns
t_v	Valid time	R_L = 330 Ω, C_L = 50 pF, See Note 2	1/(2 f_{clock})			s

NOTE 2: Clock duty cycle is assumed to be 50%.

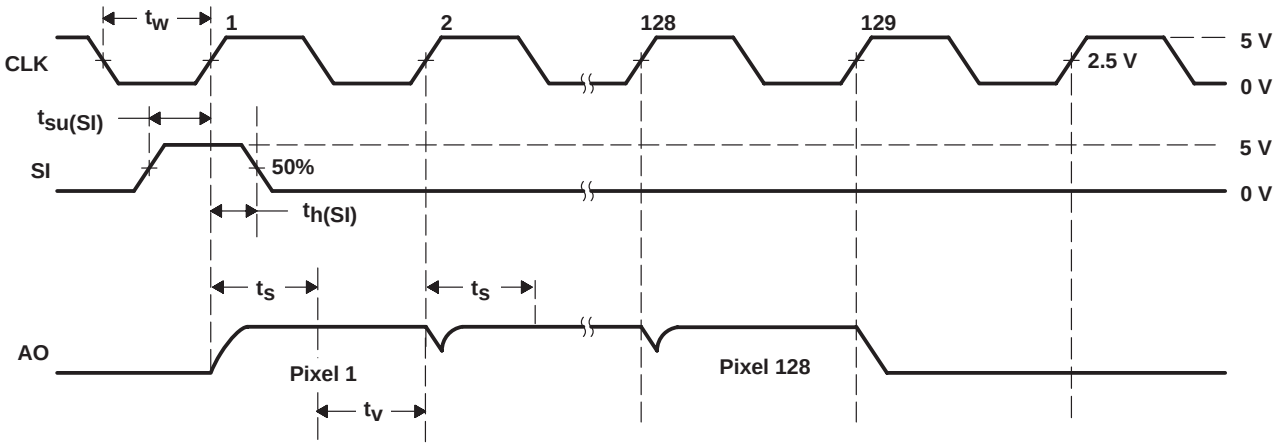


Figure 2. Operational Waveforms

TYPICAL CHARACTERISTICS

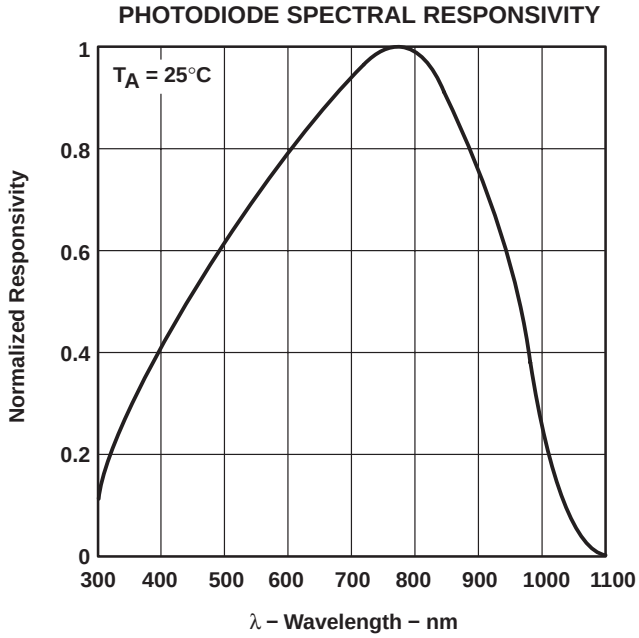
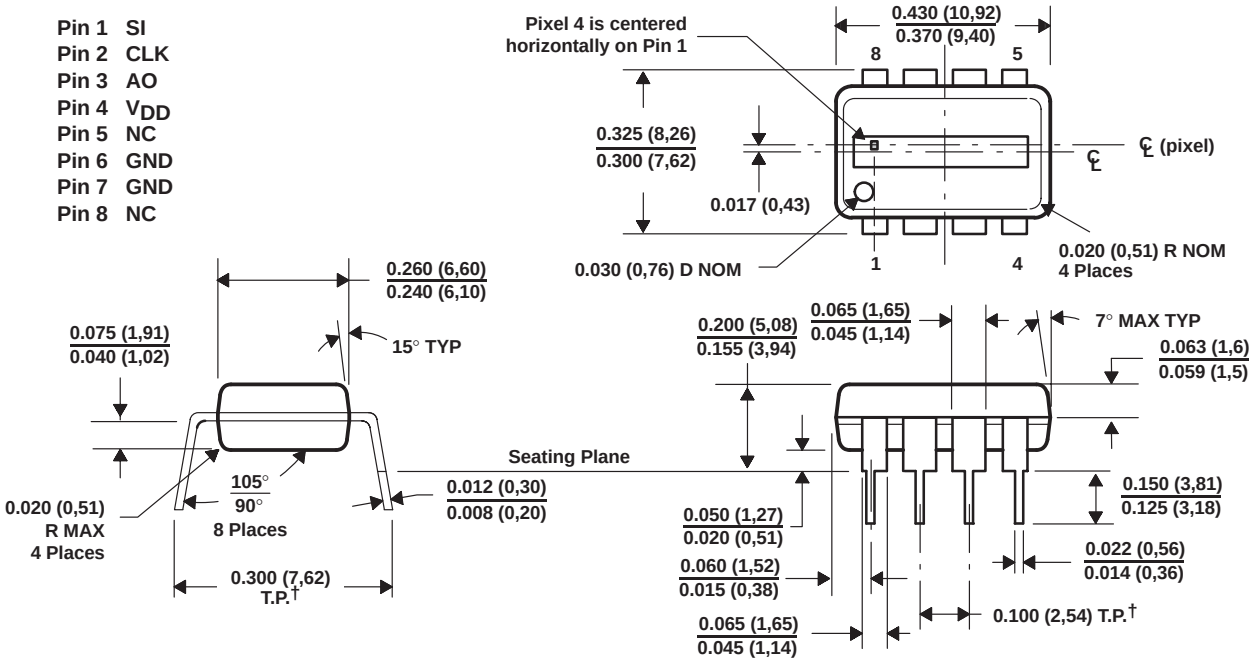


Figure 3

APPLICATIONS INFORMATION

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound.



† True position when unit is installed

NOTES: A. All linear dimensions are in inches and parenthetically in millimeters.
B. This drawing is subject ot change without notice.

Figure 4. Packaging Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSL401	OBSOLETE	XCEPT	COB	14		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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