SA58671

1.2 W/channel stereo class-D audio amplifier

Rev. 02 — 24 October 2008 Product data sheet

1. General description

The SA58671 is a stereo, filter-free class-D audio amplifier which is available in a 16 bump WLCSP (Wafer Level Chip-Size Package).

The SA58671 features independent shutdown controls for each channel. The gain can be set at 6 dB, 12 dB, 18 dB or 24 dB using G0 and G1 gain select pins. Improved immunity to noise and RF rectification is increased by high PSRR and differential circuit topology. Fast start-up time and very small WLCSP package makes it an ideal choice for both cellular handsets and PDAs.

The SA58671 delivers 1.3 W/channel at 5 V and 720 mW/channel at 3.6 V into 8 Ω. It delivers 1.2 W/channel at 5 V into 4 Ω. The maximum power efficiency is excellent at 70 % to 74 % into 4 Ω and 84 % to 88 % into 8 Ω. The SA58671 provides thermal and short-circuit shutdown protection.

2. Features

- Output power:
  - 1.2 W/channel into 4 Ω at 5 V
  - 1.3 W/channel into 8 Ω at 5 V
  - 720 mW/channel into 8 Ω at 3.6 V
- Supply voltage: 2.5 V to 5.5 V
- Independent shutdown control for each channel
- Selectable gain: 6 dB, 12 dB, 18 dB and 24 dB
- High SVRR: −77 dB at 217 Hz
- Fast start-up time: 3.5 ms
- Low supply current
- Low shutdown current
- Short-circuit and thermal protection
- Space savings with 2.06 mm × 2.11 mm 16 bump WLCSP package
- Low junction to ambient thermal resistance of 110 K/W with adequate heat sinking of WLCSP

3. Applications

- Wireless and cellular handsets and PDA
- Portable DVD player
- USB speaker
- Notebook PC

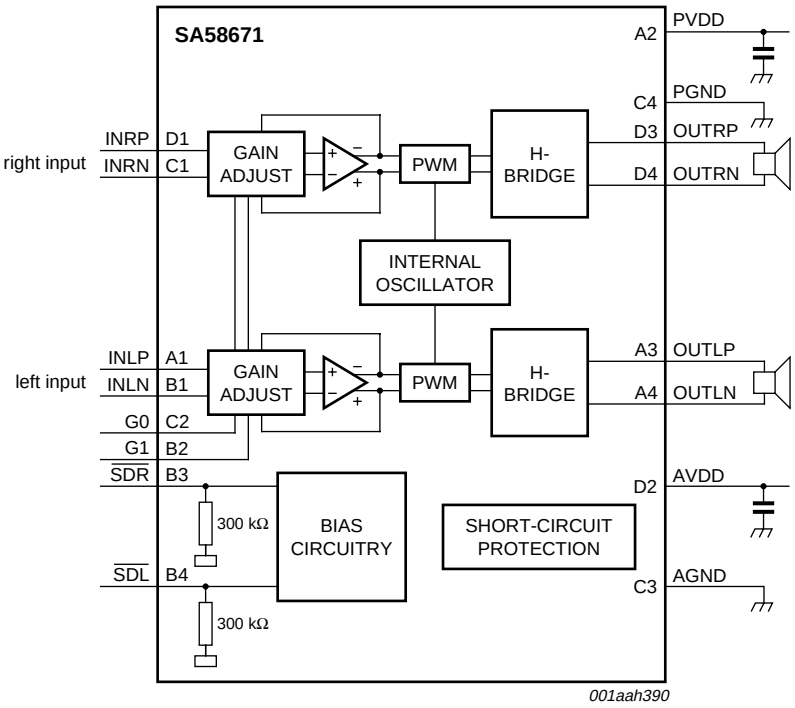
- Portable radio and gaming
- Educational toy

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SA58671UK	WLCSP16	wafer level chip-size package; 16 bumps; 2.06 × 2.11 × 0.6 mm	SA58671UK

5. Block diagram



Refer to Table 6 for gain selection.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

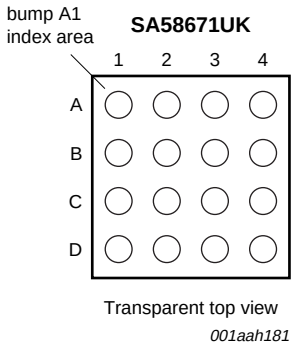
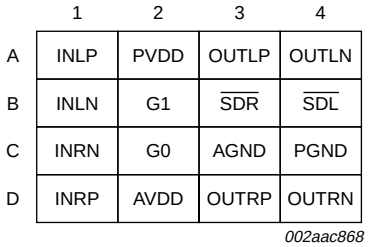


Fig 2. Pin configuration for WLCSP16



Transparent top view.

Fig 3. Bump mapping for WLCSP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
INLP	A1	left channel positive input
INLN	B1	left channel negative input
INRN	C1	right channel negative input
INRP	D1	right channel positive input
PVDD	A2	power supply voltage (level same as AVDD)
G1	B2	gain select input 1
G0	C2	gain select input 0
AVDD	D2	analog supply voltage (level same as PVDD)
OUTLP	A3	left channel positive output
$\overline{SDR}$	B3	right channel shutdown input (active LOW)
AGND	C3	analog ground
OUTRP	D3	right channel positive output
OUTLN	A4	left channel negative output
$\overline{SDL}$	B4	left channel shutdown input (active LOW)
PGND	C4	power ground
OUTRN	D4	right channel negative output

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	active mode	[1]	–0.3	+6.0	V
		shutdown mode		–0.3	+7.0	V
V_I	input voltage			–0.3	V_{DD} + 0.3	V
P	power dissipation	derating factor 9.12 mW/K				
		T_{amb} = 25 °C		-	1.2	W
		T_{amb} = 75 °C		-	690	mW
		T_{amb} = 85 °C		-	600	mW
T_{amb}	ambient temperature	operating in free air		–40	+85	°C
T_j	junction temperature	operating		–40	+150	°C
T_{stg}	storage temperature			–65	+85	°C

[1] V_{DD} is the supply voltage on pin PVDD and pin AVDD.

8. Static characteristics

Table 4. Static characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	operating	2.5	-	5.5	V
I_{DD}	supply current	V_{DD} = 5.5 V; no load	-	6	9	mA
		V_{DD} = 3.6 V; no load	-	5	7.5	mA
		V_{DD} = 2.5 V; no load	-	4	6	mA
$I_{DD(sd)}$	shutdown mode supply current	no input signal; V_{SDR} = V_{SDL} = GND	-	10	1000	nA
$\lvert V_{O(offset)} \rvert$	output offset voltage	measured differentially; inputs AC grounded; $G_{v(cl)}$ = 6 dB; V_{DD} = 2.5 V to 5.5 V	-	5	25	mV
PSRR	power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V	-	–75	–55	dB
$V_{i(cm)}$	common-mode input voltage		0.5	-	V_{DD} – 0.8	V
CMRR	common mode rejection ratio	inputs are shorted together; V_{DD} = 2.5 V to 5.5 V	-	–69	–50	dB
V_{IH}	HIGH-level input voltage	V_{DD} = 2.5 V to 5.5 V; pins $\overline{SDL}$, $\overline{SDR}$, G0, G1	1.3	-	V_{DD}	V
V_{IL}	LOW-level input voltage	V_{DD} = 2.5 V to 5.5 V; pins $\overline{SDL}$, $\overline{SDR}$, G0, G1	0	-	0.35	V
I_{IH}	HIGH-level input current	V_{DD} = 5.5 V; V_I = V_{DD}	-	-	50	µA
I_{IL}	LOW-level input current	V_{DD} = 5.5 V; V_I = 0 V	-	-	5	µA
R_{DSon}	drain-source on-state resistance	V_{DD} = 5.5 V	-	500	-	mΩ
		V_{DD} = 3.6 V	-	570	-	mΩ
		V_{DD} = 2.5 V	-	700	-	mΩ
$Z_{o(sd)}$	shutdown mode output impedance	V_{SDR} = V_{SDL} = 0.35 V	-	2	-	kΩ
f_{sw}	switching frequency	V_{DD} = 2.5 V to 5.5 V	250	300	350	kHz
$G_{v(cl)}$	closed-loop voltage gain	V_{G0} = V_{G1} = 0.35 V	5.5	6	6.5	dB
		V_{G0} = V_{DD}; V_{G1} = 0.35 V	11.5	12	12.5	dB
		V_{G0} = 0.35 V; V_{G1} = V_{DD}	17.5	18	18.5	dB
		V_{G0} = V_{G1} = V_{DD}	23.5	24	24.5	dB

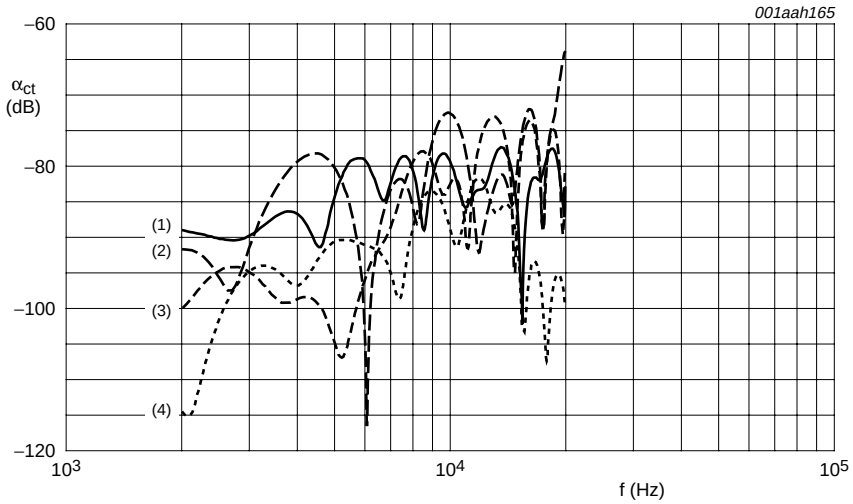
9. Dynamic characteristics

Table 5. Dynamic characteristics

T_{amb} = 25 °C; R_L = 8 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	per channel; f = 1 kHz; THD+N = 10 %				
		R_L = 8 Ω; V_{DD} = 5.0 V	-	1.3	-	W
		R_L = 8 Ω; V_{DD} = 3.6 V	-	0.72	-	W
		R_L = 4 Ω; V_{DD} = 5.0 V	-	1.2	-	W
THD+N	total harmonic distortion-plus-noise	V_{DD} = 5.0 V; $G_{v(cl)}$ = 6 dB; f = 1 kHz				
		P_o = 1 W	-	0.14	-	%
		P_o = 0.5 W	-	0.11	-	%
SVRR	supply voltage ripple rejection	$G_{v(cl)}$ = 6 dB; f = 217 Hz				
		V_{DD} = 5.0 V	-	–77	-	dB
		V_{DD} = 3.6 V	-	–73	-	dB
CMRR	common mode rejection ratio	V_{DD} = 5.0 V; $G_{v(cl)}$ = 6 dB; f = 217 Hz	-	–69	-	dB
Z_i	input impedance	$G_{v(cl)}$ = 6 dB	-	28.1	-	kΩ
		$G_{v(cl)}$ = 12 dB	-	17.3	-	kΩ
		$G_{v(cl)}$ = 18 dB	-	9.8	-	kΩ
		$G_{v(cl)}$ = 24 dB	-	5.2	-	kΩ
$t_{d(sd\text{-}startup)}$	delay time from shutdown to start-up	V_{DD} = 3.6 V	-	3.5	-	ms
$V_{n(o)}$	output noise voltage	V_{DD} = 3.6 V; f = 20 Hz to 20 kHz; inputs are AC grounded				
		no weighting	-	35	-	μV
		A weighting	-	27	-	μV

10. Typical performance curves



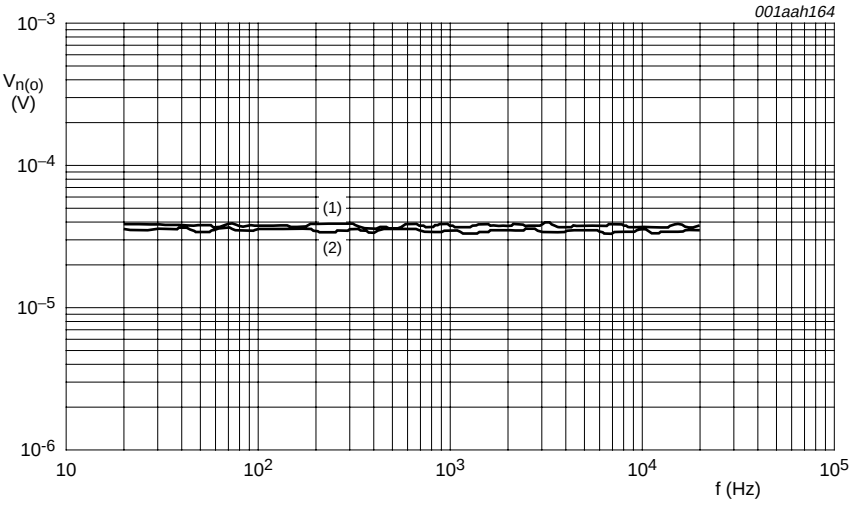
(1) V_{DD} = 3.6 V; L channel to R channel

(2) V_{DD} = 3.6 V; R channel to L channel

(3) V_{DD} = 5.0 V; L channel to R channel

(4) V_{DD} = 5.0 V; R channel to L channel

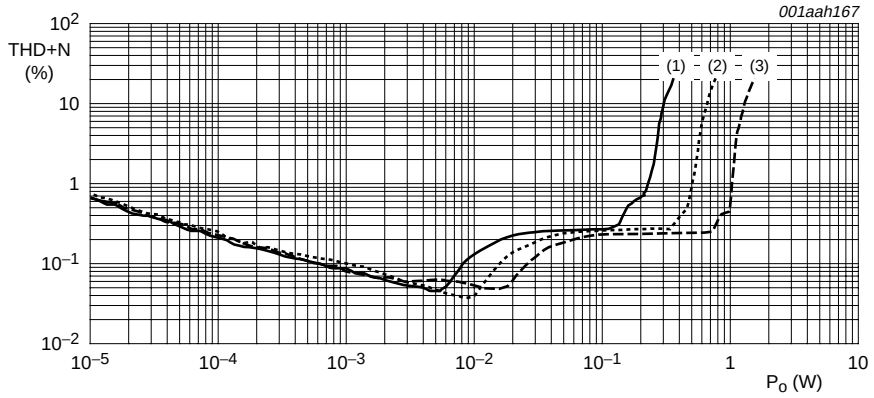
Fig 4. Crosstalk (stepped all-to-one) as a function of frequency



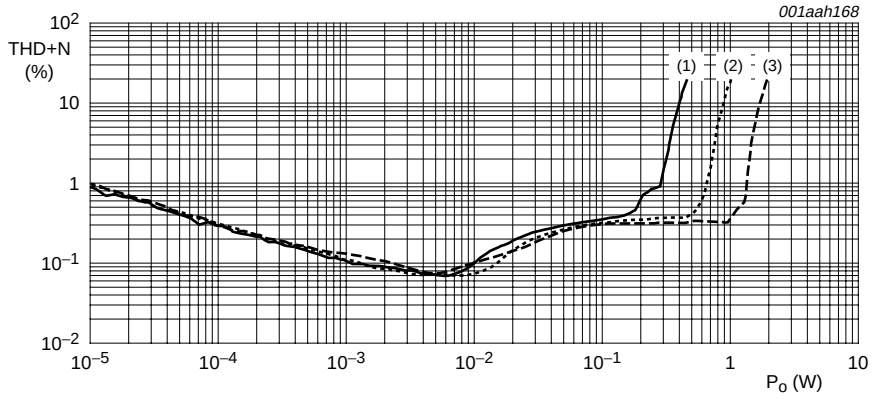
(1) Left channel

(2) Right channel

Fig 5. RMS output noise voltage as a function of frequency



a. $R_L = 8\ \Omega$



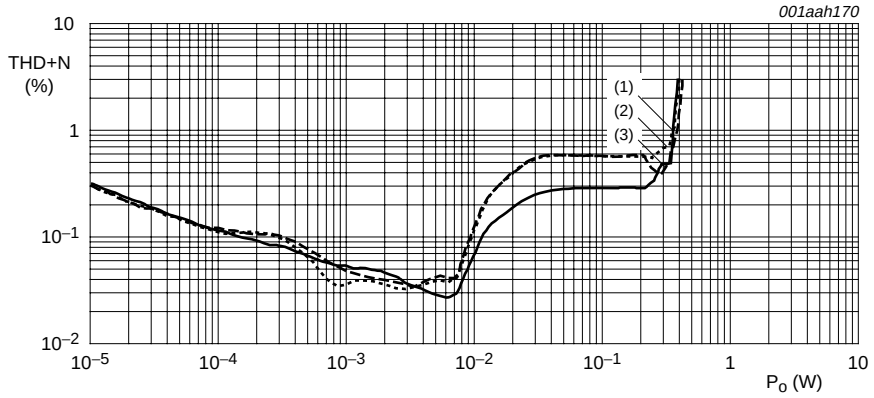
b. $R_L = 4\ \Omega$

(1) $V_{DD} = 2.5$ V

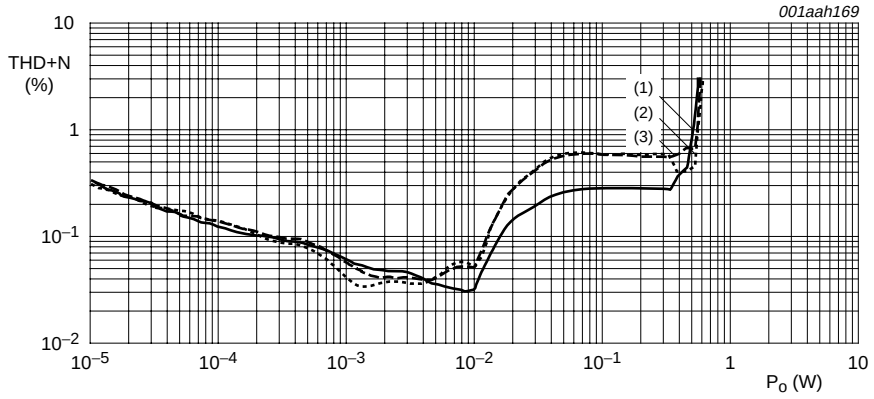
(2) $V_{DD} = 3.6$ V

(3) $V_{DD} = 5.0$ V

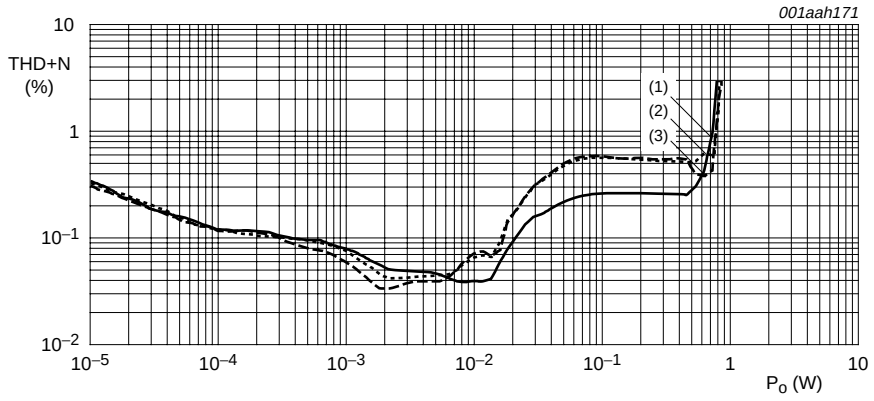
Fig 6. Total harmonic distortion-plus-noise as a function of output power; $G_{v(cl)} = 6$ dB



a. V_{DD} = 3.0 V



b. V_{DD} = 3.6 V



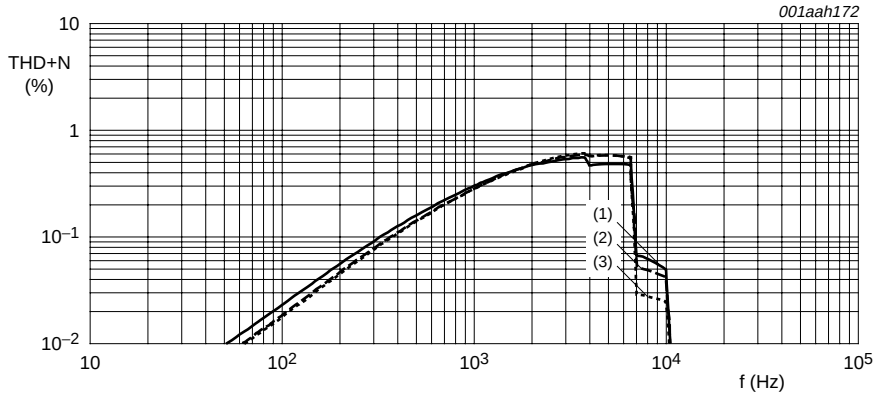
c. V_{DD} = 4.2 V

(1) f_i = 1 kHz

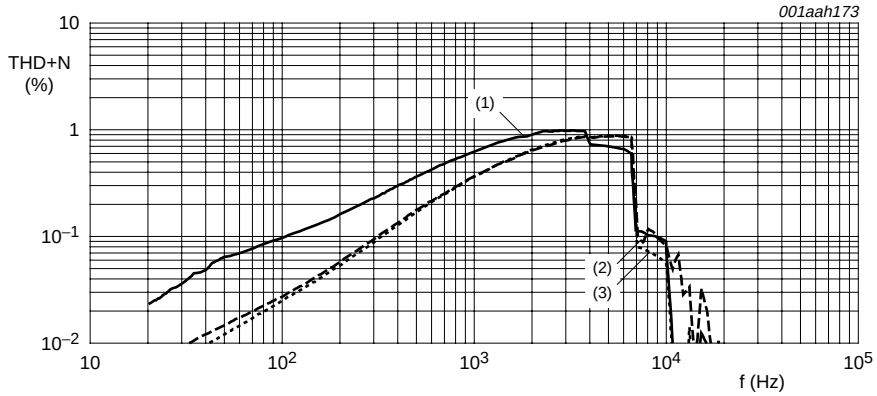
(2) f_i = 3 kHz

(3) f_i = 5 kHz

Fig 7. Total harmonic distortion-plus-noise as a function of output power; R_L = 8 Ω; $G_{v(cl)}$ = 6 dB



a. R_L = 8 Ω



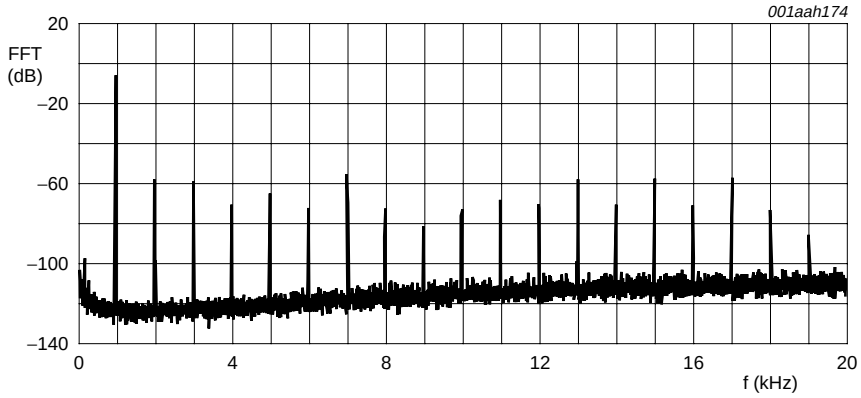
b. R_L = 4 Ω

(1) V_I = 900 mV

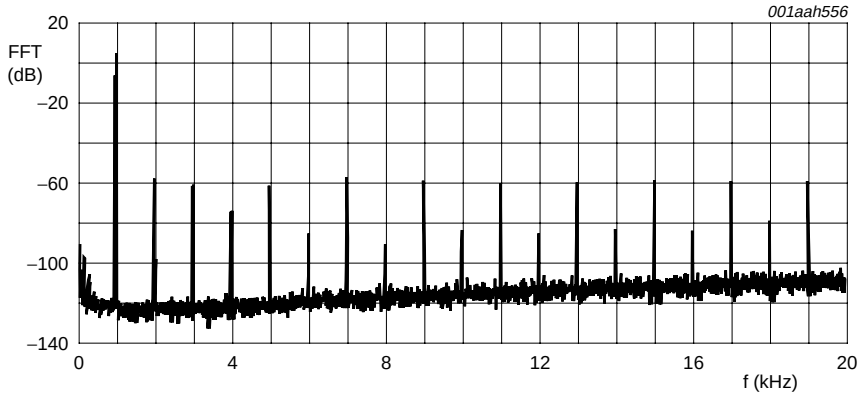
(2) V_I = 725 mV

(3) V_I = 525 mV

Fig 8. Total harmonic distortion-plus-noise as a function of frequency; V_{DD} = 3.6 V

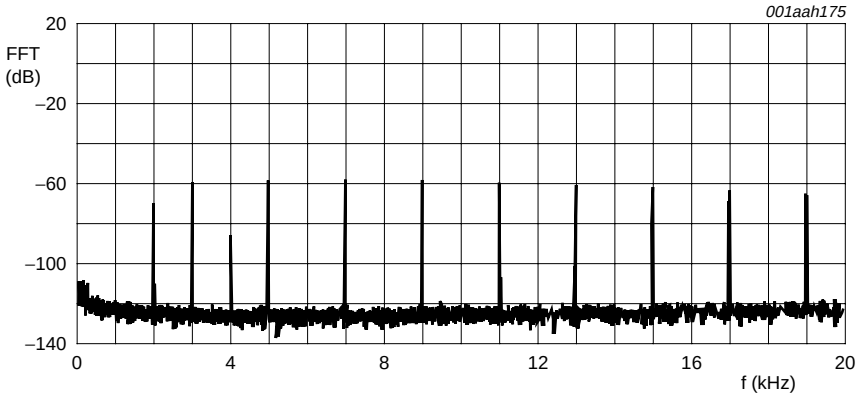


a. channel 1

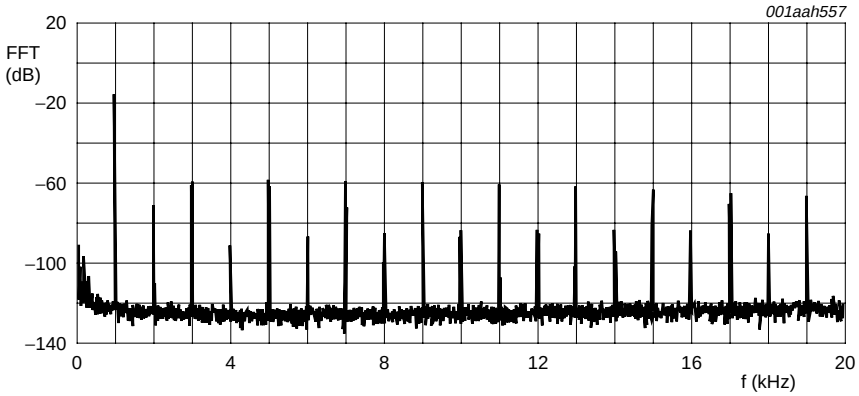


b. channel 2

Fig 9. FFT spectrum as a function of frequency; f_i = 1 kHz; V_I = 0 dB; V_{DD} = 3.6 V; R_L = 8 Ω

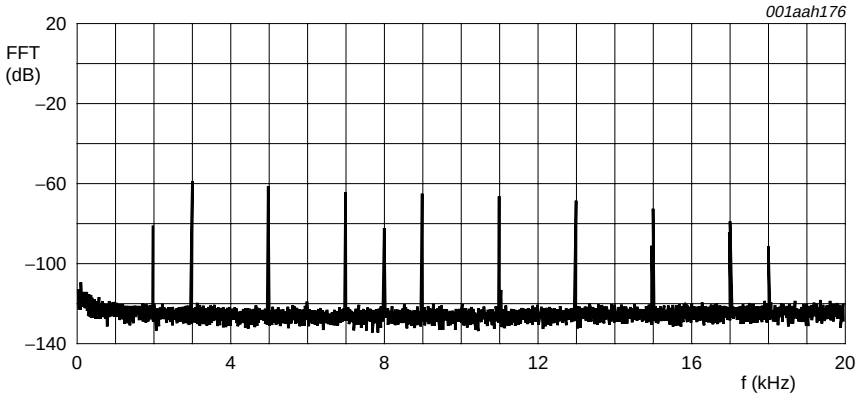


a. channel 1

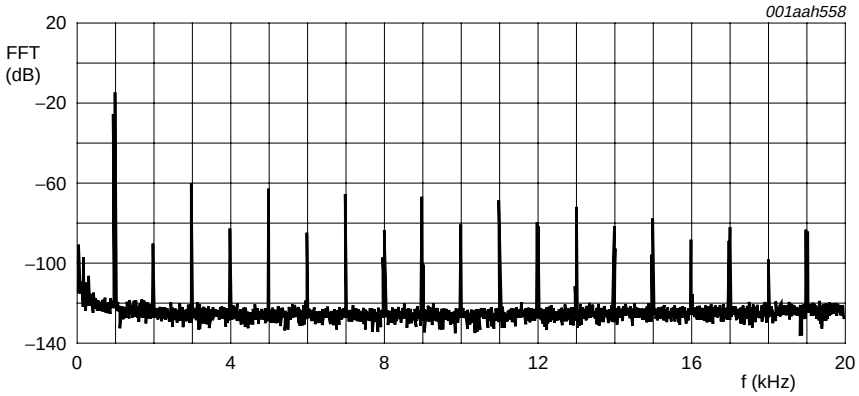


b. channel 2

Fig 10. FFT spectrum as a function of frequency; f_i = 1 kHz; V_I = −10 dB; V_{DD} = 3.6 V; R_L = 8 Ω

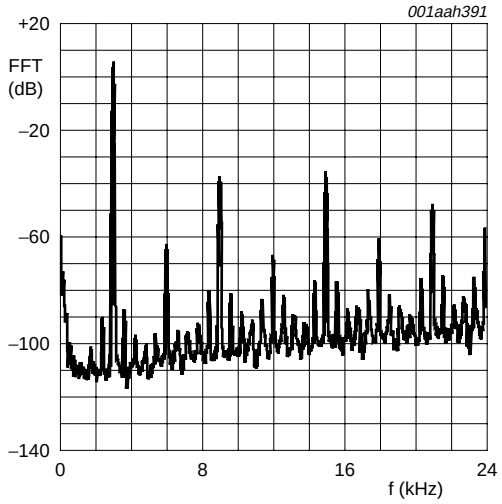


a. channel 1

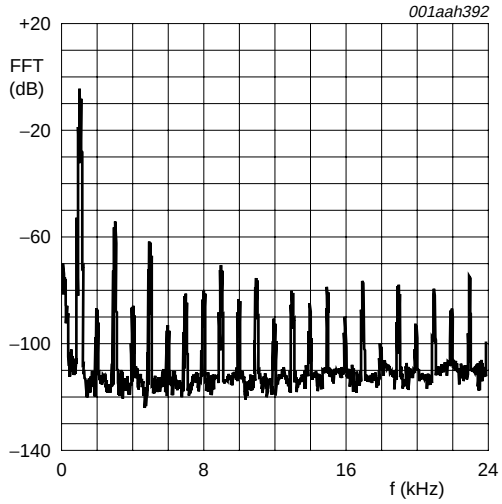


b. channel 2

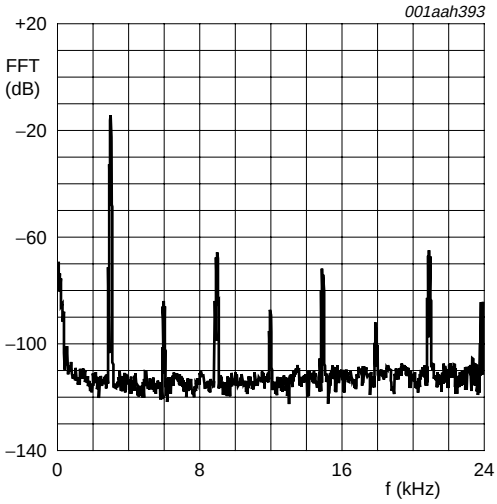
Fig 11. FFT spectrum as a function of frequency; f_i = 1 kHz; V_I = −20 dB; V_{DD} = 3.6 V; R_L = 8 Ω



a. V_I = 0 dB

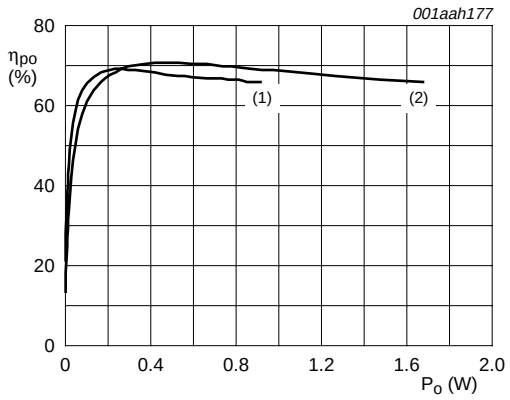


b. V_I = –10 dB

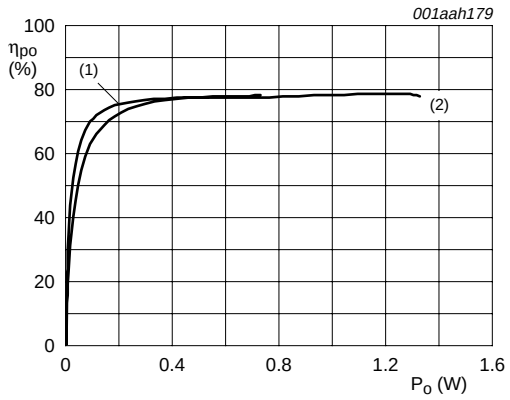


c. V_I = –20 dB

Fig 12. FFT spectrum as a function of frequency; f_i = 3 kHz; V_{DD} = 3.6 V; R_L = 8 Ω



a. R_L = 4 Ω

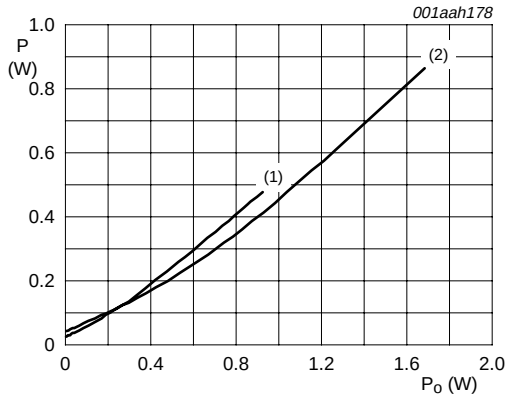


b. R_L = 8 Ω

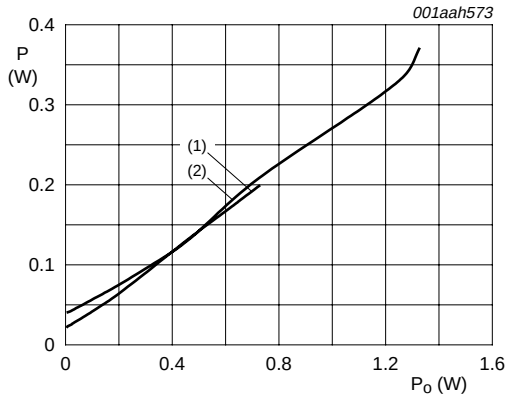
(1) V_{DD} = 3.6 V

(2) V_{DD} = 5.0 V

Fig 13. Output power efficiency as a function of output power



a. R_L = 4 Ω



b. R_L = 8 Ω

(1) V_{DD} = 3.6 V

(2) V_{DD} = 5.0 V

Fig 14. Power dissipation as a function of output power

11. Application information

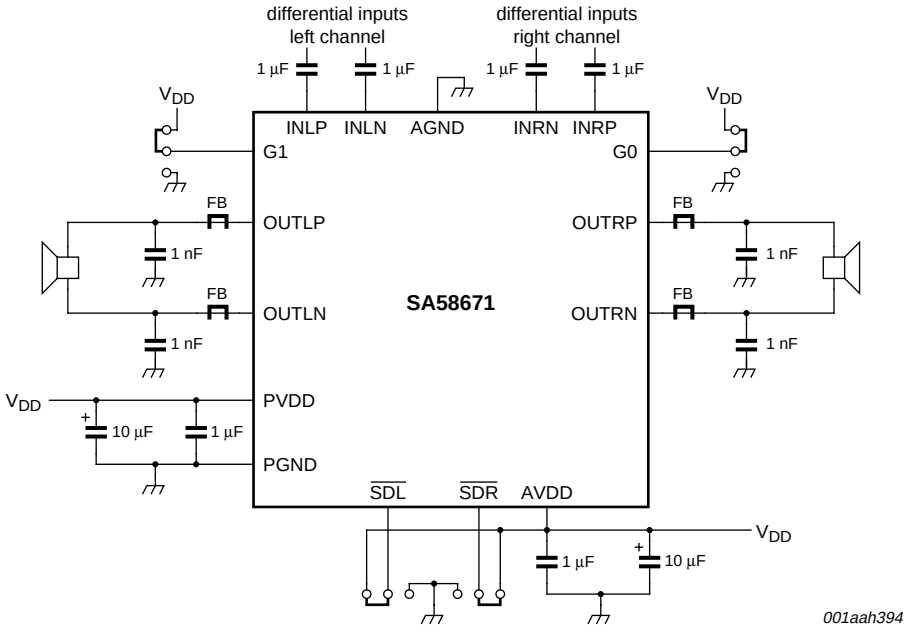


Fig 15. SA58671 application schematic

11.1 Power supply decoupling considerations

The SA58671 is a stereo class-D audio amplifier that requires proper power supply decoupling to ensure the rated performance for THD+N and power efficiency. To decouple high frequency transients, power supply spikes and digital noise on the power bus line, a low Equivalent Series Resistance (ESR) capacitor of typically 1 µF is placed as close as possible to the PVDD pins of the device. It is important to place the decoupling capacitor at the power pins of the device because any resistance or inductance in the PCB trace between the device and the capacitor can cause a loss in efficiency. Additional decoupling using a larger capacitor, 4.7 µF or greater, may be done on the power supply connection on the PCB to filter low frequency signals. Usually this is not required due to high PSRR of the device.

11.2 Input capacitor selection

The SA58671 does not require input coupling capacitors when used with a differential audio source that is biased from 0.5 V to V_{DD} − 0.8 V. In other words, the input signal must be biased within the common-mode input voltage range. If high pass filtering is required or if it is driven using a single-ended source, input coupling capacitors are required.

The 3 dB cut-off frequency created by the input coupling capacitor and the input resistors (see Table 6) is calculated by Equation 1:

$$f_{-3dB} = \frac{1}{2\pi \times R_i \times C_i} \quad (1)$$

Table 6. Gain selection

G1	G0	Gain (V/V)	Gain (dB)	Input impedance (kΩ)
LOW	LOW	2	6	28.1
LOW	HIGH	4	12	17.3
HIGH	LOW	8	18	9.8
HIGH	HIGH	16	24	5.2

Since the value of the input decoupling capacitor and the input resistance determined by the gain setting affects the low frequency performance of the audio amplifier, it is important to consider this during the system design. Small speakers in wireless and cellular phones usually do not respond well to low frequency signals, so the 3 dB cut-off frequency may be increased to block the low frequency signals to the speakers. Not using input coupling capacitors may increase the output offset voltage.

Equation 1 is solved for C_i:

$$C_i = \frac{1}{2\pi \times R_i \times f_{-3dB}} \quad (2)$$

11.3 PCB layout considerations

Component location is very important for performance of the SA58671. Place all external components very close to the device. Placing decoupling capacitors directly at the power supply pins increases efficiency because the resistance and inductance in the trace between the device power supply pins and the decoupling capacitor causes a loss in power efficiency.

The trace width and routing are also very important for power output and noise considerations.

For high current terminals (PVDD, PGND and audio output), the trace widths should be maximized to ensure proper performance and output power. Use at least 500 μm wide traces.

For the input pins (INRP, INRN, INLP and INLN), the traces must be symmetrical and run side-by-side to maximize common-mode cancellation.

11.4 Filter-free operation and ferrite bead filters

A ferrite bead low-pass filter can be used to reduce radio frequency emissions in applications that have circuits sensitive to frequencies greater than 1 MHz. A ferrite bead low-pass filter functions well for amplifiers that must pass FCC unintentional radiation requirements for frequencies greater than 30 MHz. Choose a bead with high-impedance at high frequencies and very low-impedance at low frequencies. In order to prevent distortion of the output signal, select a ferrite bead with adequate current rating.

For applications in which there are circuits that are EMI sensitive to low frequency (< 1 MHz) and there are long leads from amplifier to speaker, it is necessary to use an LC output filter.

11.5 Efficiency and thermal considerations

The maximum ambient temperature depends on the heat transferring ability of the heat spreader on the PCB layout. In Table 3 “Limiting values”, power dissipation, the power derating factor is given as 9.12 mW/K. The device thermal resistance, $R_{th(j-a)}$ is the reciprocal of the power derating factor. Convert the power derating factor to $R_{th(j-a)}$ by Equation 3:

$$R_{th(j-a)} = \frac{1}{derating\ factor} = \frac{1}{0.00912} = 110\ K/W \quad (3)$$

For a maximum allowable junction temperature, T_j = 150 °C and $R_{th(j-a)}$ = 110 K/W and a maximum device dissipation of 0.6 W (300 mW per channel) and for 1.2 W per channel output power, 4 Ω load, 5 V supply, the maximum ambient temperature is calculated using Equation 4:

$$T_{amb(max)} = T_{j(max)} - (R_{th(j-a)} \times P_{max}) = 150 - (110 \times 0.60) = 84\ °C \quad (4)$$

The maximum ambient temperature is 84 °C at maximum power dissipation for 5 V supply and 4 Ω load. If the junction temperature of the SA58671 rises above 150 °C, the thermal protection circuitry turns the device off; this prevents damage to IC. Using speakers greater than 4 Ω further enhances thermal performance and battery lifetime by reducing the output load current and increasing amplifier efficiency.

11.6 Additional thermal information

The SA58671 16 bump WLCSP package ground bumps are soldered directly to the PCB heat spreader. By the use of thermal vias, the bumps may be soldered directly to a ground plane or special heat sinking layer designed into the PCB. The thickness and area of the heat spreader may be maximized to optimize heat transfer and achieve lowest package thermal resistance.

12. Test information

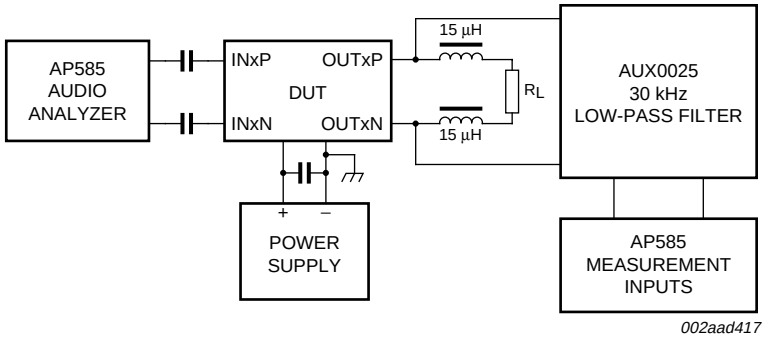
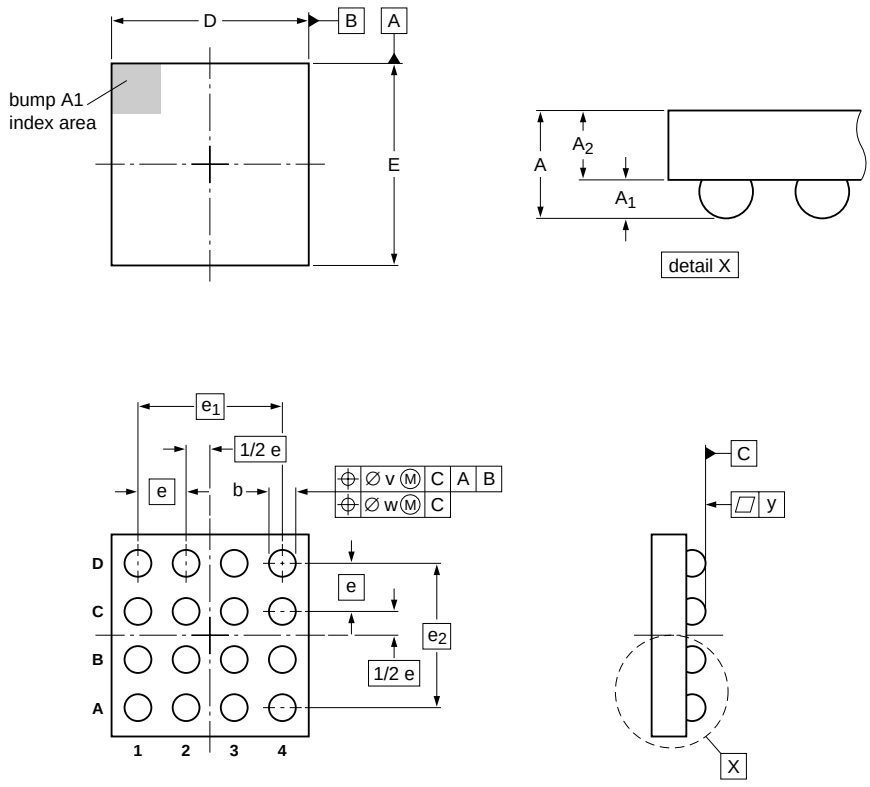


Fig 16. Test circuit

13. Package outline

WLCSP16: wafer level chip-size package; 16 bumps; 2.06 x 2.11 x 0.6 mm **SA58671UK**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	0.64	0.26 0.22	0.38 0.34	0.34 0.30	2.08 2.04	2.13 2.09	0.5	1.5	1.5	0.01	0.04	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SA58671UK						~~07-10-11~~ 07-10-17

Fig 17. Package outline WLCSP16

14. Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

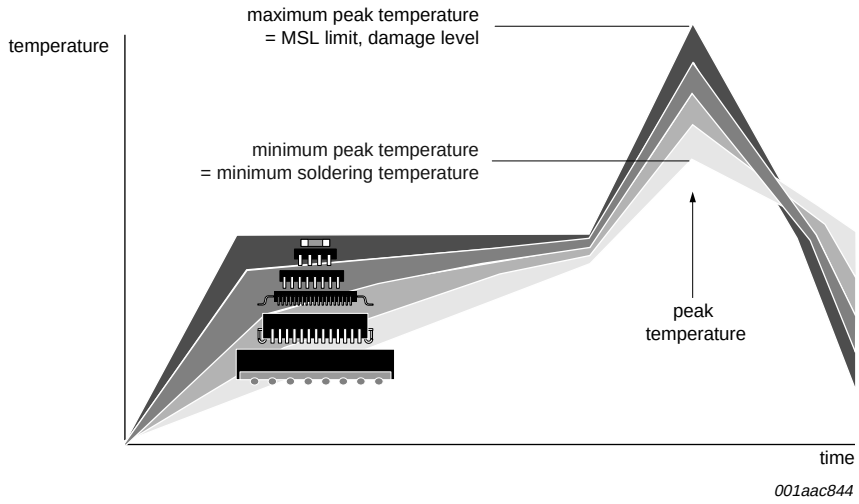
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15. Abbreviations

Table 8. Abbreviations

Acronym	Description
DUT	Device Under Test
DVD	Digital Video Disc
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
LC	inductor-capacitor filter
PC	Personal Computer
PCB	Printed-Circuit Board
PDA	Personal Digital Assistant
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulator
USB	Universal Serial Bus
WLCSP	Wafer Level Chip-Size Package

16. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58671_2	20081024	Product data sheet	-	SA58671_1
Modifications:	• Table 4 "Static characteristics": – added "$I_{DD(sd)}$, shutdown mode supply current" specification • Updated soldering information			
SA58671_1	20071221	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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