# Dual 90MHz, 22V/µs 16-Bit Accurate Operational Amplifier

## FEATURES

- **90MHz Gain Bandwidth, f = 100kHz**
- **Maximum Input Offset Voltage: 125µV**
- **Settling Time: 900ns ($A_V$ = –1, 150µV, 10V Step)**
- **22V/µs Slew Rate**
- Low Distortion: –96.5dB for 100kHz, $10V_{P-P}$
- Maximum Input Offset Voltage Drift: 3µV/°C
- Maximum Inverting Input Bias Current: 10nA
- Minimum DC Gain: 300V/mV
- Minimum Output Swing into 2k: ±12.8V
- Unity-Gain Stable
- Input Noise Voltage: $5nV/\sqrt{Hz}$
- Input Noise Current: $0.6pA/\sqrt{Hz}$
- Total Input Noise Optimized for $1k\Omega < R_S < 20k\Omega$
- Specified at ±5V and ±15V Supplies

## APPLICATIONS

- Precision Instrumentation
- High Accuracy Data Acquisition Systems
- 16-Bit DAC Current-to-Voltage Converter
- ADC Buffer
- Low Distortion Active Filters
- Photodiode Amplifiers

## DESCRIPTION

The LT®1469 is a dual, precision high speed operational amplifier with 16-bit accuracy and 900ns settling to 150µV for 10V steps. This unique blend of precision and AC performance makes the LT1469 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

The 90MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance.

The 22V/µs slew rate of the LT1469 improves large signal performance compared to other precision op amps in applications such as active filters and instrumentation amplifiers.

The LT1469 is available in a space saving 4mm × 4mm leadless package, as well as in small outline and DIP packages. A single version, the LT1468, is also available.

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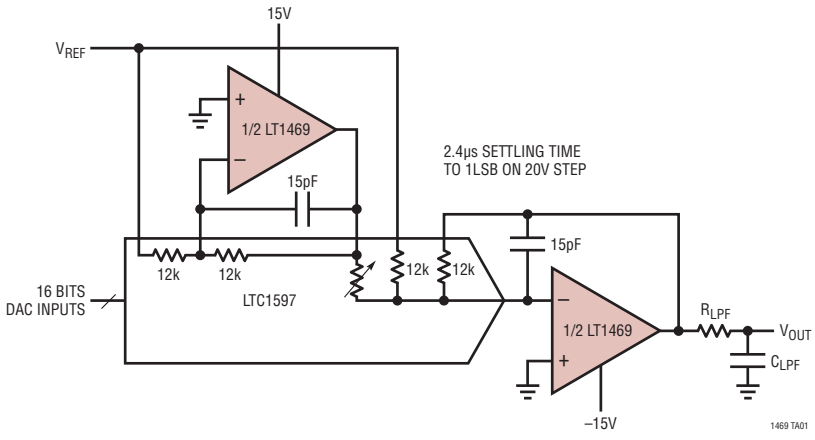
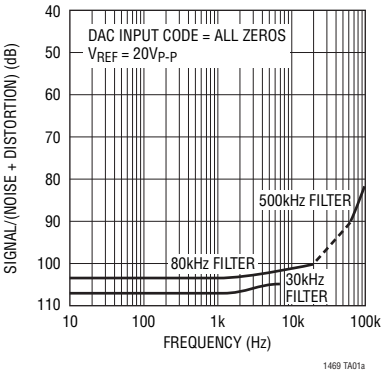
## TYPICAL APPLICATION

**16-Bit DAC I-to-V Converter and Reference Inverter for Bipolar Output Swing ($V_{OUT}$ = –10V to 10V)**



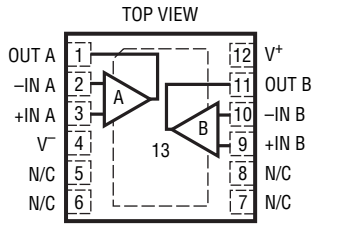

**Bipolar Multiplying Mode (LTC1597) Signal-to-(Noise + Distortion)**



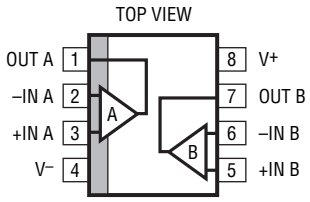
## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V^+$ to $V^-$).....36V
Input Current (Note 2).....±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4).... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
S8 and N8 Package..... 300°C

## PIN CONFIGURATION




DF PACKAGE
12-LEAD (4mm × 4mm) PLASTIC DFN
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 43°C/W
EXPOSED PAD (PIN 13) MUST BE CONNECTED TO $V^-$




N8 PACKAGE
8-LEAD PDIP
S8 PACKAGE
8-LEAD PLASTIC SO
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W (N8)
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 190°C/W (S8)

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT1469CN8#PBF | NA | LT1469CN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1469IN8#PBF | NA | LT1469IN8 | 8-Lead PDIP | –40°C to 85°C |
| LT1469CS8#PBF | LT1469CS8#TRPBF | 1469 | 8-Lead Plastic Small Outline | 0°C to 70°C |
| LT1469IS8#PBF | LT1469IS8#TRPBF | 1469I | 8-Lead Plastic Small Outline | –40°C to 85°C |
| LT1469ACDF#PBF | LT1469ACDF#TRPBF | 1469 | 12-Lead (4mm × 4mm) Plastic DFN | 0°C to 70°C |
| LT1469AIDF#PBF | LT1469AIDF#TRPBF | 1469 | 12-Lead (4mm × 4mm) Plastic DFN | –40°C to 85°C |
| LT1469CDF#PBF | LT1469CDF#TRPBF | 1469 | 12-Lead (4mm × 4mm) Plastic DFN | 0°C to 70°C |
| LT1469IDF#PBF | LT1469IDF#TRPBF | 1469 | 12-Lead (4mm × 4mm) Plastic DFN | –40°C to 85°C |
| **LEAD BASED FINISH** | **TAPE AND REEL** | **PART MARKING** | **PACKAGE DESCRIPTION** | **TEMPERATURE RANGE** |
| LT1469CN8 | NA | LT1469CN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1469IN8 | NA | LT1469IN8 | 8-Lead PDIP | –40°C to 85°C |
| LT1469CS8 | LT1469CS8#TR | 1469 | 8-Lead Plastic Small Outline | 0°C to 70°C |
| LT1469IS8 | LT1469IS8#TR | 1469I | 8-Lead Plastic Small Outline | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | N8, S8 Packages | ±15V<br>±5V | | 50<br>50 | 125<br>200 | µV<br>µV |
| | | LT1469A, DF Package | ±15V<br>±5V | | 50<br>50 | 125<br>200 | µV<br>µV |
| | | LT1469, DF Package | ±15V<br>±5V | | 100<br>150 | 225<br>300 | µV<br>µV |
| $I_{OS}$ | Input Offset Current | | ±5V to ±15V | | 13 | ±50 | nA |
| $I_B-$ | Inverting Input Bias Current | | ±5V to ±15V | | 3 | ±10 | nA |
| $I_B+$ | Noninverting Input Bias Current | | ±5V to ±15V | | –10 | ±40 | nA |
| | Input Noise Voltage | 0.1Hz to 10Hz | ±5V to ±15V | | 0.3 | | $\mu V_{P-P}$ |
| $e_n$ | Input Noise Voltage Density | f = 10kHz | ±5V to ±15V | | 5 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Noise Current Density | f = 10kHz | ±5V to ±15V | | 0.6 | | $pA/\sqrt{Hz}$ |
| $R_{IN}$ | Input Resistance | Common Mode, $V_{CM}$ = ±12.5V<br>Differential | ±15V<br>±15V | 100<br>50 | 240<br>150 | | MΩ<br>kΩ |
| $C_{IN}$ | Input Capacitance | | ±15V | | 4 | | pF |
| $V_{CM}$ | Input Voltage Range (Positive) | Guaranteed by CMRR | ±15V<br>±5V | 12.5<br>2.5 | 13.5<br>3.6 | | V<br>V |
| | Input Voltage Range (Negative) | Guaranteed by CMRR | ±15V<br>±5V | | –14.3<br>–4.4 | –12.5<br>–2.5 | V<br>V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±12.5V<br>$V_{CM}$ = ±2.5V | ±15V<br>±5V | 96<br>96 | 110<br>112 | | dB<br>dB |
| | Minimum Supply Voltage | Guaranteed by PSRR | | | ±2.5 | ±4.5 | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4.5V to ±15V | | 100 | 112 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT}$ = ±12.5V, $R_L$ = 10k<br>$V_{OUT}$ = ±12.5V, $R_L$ = 2k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 10k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 2k | ±15V<br>±15V<br>±5V<br>±5V | 300<br>300<br>200<br>200 | 2000<br>2000<br>8000<br>8000 | | V/mV<br>V/mV<br>V/mV<br>V/mV |
| $V_{OUT}$ | Maximum Output Swing | $R_L$ = 10k<br>$R_L$ = 2k<br>$R_L$ = 10k<br>$R_L$ = 2k | ±15V<br>±15V<br>±5V<br>±5V | ±13.0<br>±12.8<br>±3.0<br>±2.8 | ±13.6<br>±13.5<br>±3.7<br>±3.6 | | V<br>V<br>V<br>V |
| $I_{OUT}$ | Maximum Output Current | $V_{OUT}$ = ±12.5V<br>$V_{OUT}$ = ±2.5V | ±15V<br>±5V | ±15<br>±15 | ±22<br>±22 | | mA<br>mA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0V, 0.2V Overdrive (Note 3) | ±15V | ±25 | ±40 | | mA |
| SR | Slew Rate | $A_V$ = –10, $R_L$ = 2k (Note 6) | ±15V<br>±5V | 15<br>11 | 22<br>17 | | V/µs<br>V/µs |
| FPBW | Full-Power Bandwidth | 10V Peak, (Note 7)<br>3V Peak, (Note 7) | ±15V<br>±5V | | 350<br>900 | | kHz<br>kHz |
| GBW | Gain Bandwidth Product | f = 100kHz, $R_L$ = 2k | ±15V<br>±5V | 60<br>55 | 90<br>88 | | MHz<br>MHz |
| $t_r$, $t_f$ | Rise Time, Fall Time | $A_V$ = 1, 10% to 90%, 0.1V Step | ±15V<br>±5V | | 11<br>12 | | ns<br>ns |
| OS | Overshoot | $A_V$ = 1, 0.1V Step | ±15V<br>±5V | | 30<br>35 | | %<br>% |
| $t_{PD}$ | Propagation Delay | $A_V$ = 1, 50% $V_{IN}$ to 50% $V_{OUT}$, 0.1V Step | ±15V<br>±5V | | 9<br>10 | | ns<br>ns |

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C. $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_S$ | Settling Time | 10V Step, 0.01%, $A_V$ = –1<br>10V Step, 150µV, $A_V$ = –1<br>5V Step, 0.01%, $A_V$ = –1 | ±15V<br>±15V<br>±5V | | 760<br>900<br>770 | | ns<br>ns<br>ns |
| THD | Total Harmonic Distortion | $A_V$ = –1, $V_{OUT}$ = 10$V_{P-P}$, f = 100kHz<br>$A_V$ = 1, $V_{OUT}$ = 20$V_{P-P}$, f = 1kHz | ±15V<br>±15V | | –96.5<br>–125 | | dB<br>dB |
| $R_{OUT}$ | Output Resistance | $A_V$ = 1, f = 100kHz | ±15V | | 0.02 | | Ω |
| | Channel Separation | $V_{OUT}$ = ±12.5V, $R_L$ = 2k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 2k | ±15V<br>±5V | 100<br>100 | 130<br>130 | | dB<br>dB |
| $I_S$ | Supply Current | Per Amplifier | ±15V<br>±5V | | 4.1<br>3.8 | 5.2<br>5 | mA<br>mA |
| $\Delta V_{OS}$ | Input Offset Voltage Match | S8, DF A-Grade | ±15V<br>±5V | | 30<br>50 | 225<br>350 | µV<br>µV |
| $\Delta I_B$– | Inverting Input Bias Current Match | | ±5V to ±15V | | 2 | 18 | nA |
| $\Delta I_B$+ | Noninverting Input Bias Current Match | | ±5V to ±15V | | 5 | 78 | nA |
| ΔCMRR | Common Mode Rejection Match | $V_{CM}$ = ±12.5V (Note 9)<br>$V_{CM}$ = ±2.5V (Note 9) | ±15V<br>±5V | 93<br>93 | 113<br>115 | | dB<br>dB |
| ΔPSRR | Power Supply Rejection Match | $V_S$ = ±4.5V to ±15V (Note 9) | | 97 | 115 | | dB |

**The ● denotes the specifications which apply over the full operating temperature range, 0°C ≤ $T_A$ ≤ 70°C. $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | N8, S8 Packages | ±15V<br>±5V | ●<br>● | | | 350<br>350 | µV<br>µV |
| | | LT1469A, DF Package | ±15V<br>±5V | ●<br>● | | | 225<br>275 | µV<br>µV |
| | | LT1469, DF Package | ±15V<br>±5V | ●<br>● | | | 450<br>450 | µV<br>µV |
| $\Delta V_{OS}/\Delta T$ | Input Offset Voltage Drift | (Note 8) | ±15V<br>±5V | ●<br>● | | 1<br>1 | 5<br>3 | µV/°C<br>µV/°C |
| $I_{OS}$ | Input Offset Current | | ±5V to ±15V | ● | | | ±80 | nA |
| $\Delta I_{OS}/\Delta T$ | Input Offset Current Drift | (Note 8) | ±5V to ±15V | ● | | 60 | | pA/°C |
| $I_B$– | Inverting Input Bias Current | | ±5V to ±15V | ● | | | ±20 | nA |
| $\Delta I_B$–/ΔT | Inverting Input Bias Current Drift | (Note 8) | ±5V to ±15V | ● | | 40 | | pA/°C |
| $I_B$+ | Noninverting Input Bias Current | | ±5V to ±15V | ● | | | ±60 | nA |
| $V_{CM}$ | Input Voltage Range (Positive) | Guaranteed by CMRR | ±15V<br>±5V | ●<br>● | 12.5<br>2.5 | | | V<br>V |
| | Input Voltage Range (Negative) | Guaranteed by CMRR | ±15V<br>±5V | ●<br>● | | | –12.5<br>–2.5 | V<br>V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±12.5V | ±15V | ● | 94 | | | dB |
| | | $V_{CM}$ = ±2.5V | ±5V | ● | 94 | | | dB |
| | Minimum Supply Voltage | Guaranteed by PSRR | | ● | | | ±4.5 | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4.5V to ±15V | | ● | 95 | | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT}$ = ±12.5V, $R_L$ = 10k<br>$V_{OUT}$ = ±12.5V, $R_L$ = 2k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 10k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 2k | ±15V<br>±15V<br>±5V<br>±5V | ●<br>●<br>●<br>● | 100<br>100<br>100<br>100 | | | V/mV<br>V/mV<br>V/mV<br>V/mV |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, 0°C ≤ $T_A$ ≤ 70°C. $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Maximum Output Swing | $R_L$ = 10k<br>$R_L$ = 2k<br>$R_L$ = 10k<br>$R_L$ = 2k | ±15V<br>±15V<br>±5V<br>±5V | ●<br>●<br>●<br>● | ±12.9<br>±12.7<br>±2.9<br>±2.7 | | | V<br>V<br>V<br>V |
| $I_{OUT}$ | Maximum Output Current | $V_{OUT}$ = ±12.5V<br>$V_{OUT}$ = ±2.5V | ±15V<br>±5V | ●<br>● | ±12.5<br>±12.5 | | | mA<br>mA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0V, 0.2V Overdrive (Note 3) | ±15V | ● | ±17 | | | mA |
| SR | Slew Rate | $A_V$ = –10, $R_L$ = 2k (Note 6) | ±15V<br>±5V | ●<br>● | 13<br>9 | | | V/µs<br>V/µs |
| GBW | Gain Bandwidth Product | f = 100kHz, $R_L$ = 2k | ±15V<br>±5V | ●<br>● | 55<br>50 | | | MHz<br>MHz |
| | Channel Separation | $V_{OUT}$ = ±12.5V, $R_L$ = 2k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 2k | ±15V<br>±5V | ●<br>● | 98<br>98 | | | dB<br>dB |
| $I_S$ | Supply Current | Per Amplifier | ±15V<br>±5V | ●<br>● | | | 6.5<br>6.3 | mA<br>mA |
| $\Delta V_{OS}$ | Input Offset Voltage Match | S8, DF A-Grade | ±15V<br>±5V | ●<br>● | | | 600<br>600 | µV<br>µV |
| $\Delta I_B-$ | Inverting Input Bias Current Match | | ±5V to ±15V | ● | | | 38 | nA |
| $\Delta I_B+$ | Noninverting Input Bias Current Match | | ±5V to ±15V | ● | | | 118 | nA |
| ΔCMRR | Common Mode Rejection Match | $V_{CM}$ = ±12.5V (Note 9)<br>$V_{CM}$ = ±2.5V (Note 9) | ±15V<br>±5V | ●<br>● | 91<br>91 | | | dB<br>dB |
| ΔPSRR | Power Supply Rejection Match | $V_S$ = ±4.5V to ±15V (Note 9) | | ● | 92 | | | dB |

**The ● denotes the specifications which apply over the full operating temperature range, –40°C ≤ $T_A$ ≤ 85°C, $V_{CM}$ = 0V unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | N8, S8 Packages | ±15V<br>±5V | ●<br>● | | | 500<br>500 | µV<br>µV |
| | | LT1469A, DF Package | ±15V<br>±5V | ●<br>● | | | 300<br>350 | µV<br>µV |
| | | LT1469, DF Package | ±15V<br>±5V | ●<br>● | | | 600<br>600 | µV<br>µV |
| $\Delta V_{OS}/\Delta T$ | Input Offset Voltage Drift | (Note 8) | ±15V<br>±5V | ●<br>● | | 1<br>1 | 6<br>5 | µV/°C<br>µV/°C |
| $I_{OS}$ | Input Offset Current | | ±5V to ±15V | ● | | | ±120 | nA |
| $\Delta I_{OS}/\Delta T$ | Input Offset Current Drift | (Note 8) | ±5V to ±15V | ● | | 120 | | pA/°C |
| $I_B-$ | Inverting Input Bias Current | | ±5V to ±15V | ● | | | ±40 | nA |
| $\Delta I_B-/\Delta T$ | Inverting Input Bias Current Drift | (Note 8) | ±5V to ±15V | ● | | 80 | | pA/°C |
| $I_B+$ | Noninverting Input Bias Current | | ±5V to ±15V | ● | | | ±80 | nA |
| $V_{CM}$ | Input Voltage Range (Positive) | Guaranteed by CMRR | ±15V<br>±5V | ●<br>● | 12.5<br>2.5 | | | V<br>V |
| | Input Voltage Range (Negative) | Guaranteed by CMRR | ±15V<br>±5V | ●<br>● | | | –12.5<br>–2.5 | V<br>V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, –40°C ≤ $T_A$ ≤ 85°C, $V_{CM}$ = 0V unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±12.5V<br>$V_{CM}$ = ±2.5V | ±15V<br>±5V | ●<br>● | 92<br>92 | | | dB<br>dB |
| | Minimum Supply Voltage | Guaranteed by PSRR | | ● | | | ±4.5 | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4.5V to ±15V | | ● | 93 | | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT}$ = ±12,5V, $R_L$ = 10k<br>$V_{OUT}$ = ±12.5V, $R_L$ = 2k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 10k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 2k | ±15V<br>±15V<br>±5V<br>±5V | ●<br>●<br>●<br>● | 75<br>75<br>75<br>75 | | | V/mV<br>V/mV<br>V/mV<br>V/mV |
| $V_{OUT}$ | Maximum Output Swing | $R_L$ = 10k<br>$R_L$ = 2k<br>$R_L$ = 10k<br>$R_L$ = 2k | ±15V<br>±15V<br>±5V<br>±5V | ●<br>●<br>●<br>● | ±12.8<br>±12.6<br>±2.8<br>±2.6 | | | V<br>V<br>V<br>V |
| $I_{OUT}$ | Maximum Output Current | $V_{OUT}$ = ±12.5V<br>$V_{OUT}$ = ±2.5V | ±15V<br>±5V | ●<br>● | ±7<br>±7 | | | mA<br>mA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0V, 0.2V Overdrive (Note 3) | ±15V | ● | ±12 | | | mA |
| SR | Slew Rate | $A_V$ = –10, $R_L$ = 2k (Note 6) | ±15V<br>±5V | ●<br>● | 9<br>6 | | | V/µs<br>V/µs |
| GBW | Gain Bandwidth Product | f = 100kHz, $R_L$ = 2k | ±15V<br>±5V | ●<br>● | 45<br>40 | | | MHz<br>MHz |
| | Channel Separation | $V_{OUT}$ = ±12.5V, $R_L$ = 2k<br>$V_{OUT}$ = ±2.5V, $R_L$ = 2k | ±15V<br>±5V | ●<br>● | 96<br>96 | | | dB<br>dB |
| $I_S$ | Supply Current | Per Amplifier | ±15V<br>±5V | ●<br>● | | | 7<br>6.8 | mA<br>mA |
| $\Delta V_{OS}$ | Input Offset Voltage Match | S8, DF A-Grade | ±15V<br>±5V | ●<br>● | | | 800<br>800 | µV<br>µV |
| $\Delta I_B$– | Inverting Input Bias Current Match | | ±5V to ±15V | ● | | | 78 | nA |
| $\Delta I_B$+ | Noninverting Input Bias Current Match | | ±5V to ±15V | ● | | | 158 | nA |
| ΔCMRR | Common Mode Rejection Match | $V_{CM}$ = ±12.5V (Note 9)<br>$V_{CM}$ = ±2.5V (Note 9) | ±15V<br>±5V | ●<br>● | 89<br>89 | | | dB<br>dB |
| ΔPSRR | Power Supply Rejection Match | $V_S$ = ±4.5V to ±15V (Note 9) | | ● | 90 | | | dB |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to less than 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

**Note 4:** The LT1469C and LT1469I are guaranteed functional over the operating temperature range of –40°C to 85°C.

**Note 5:** The LT1469C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1469I is guaranteed to meet specified performance from –40°C to 85°C.

**Note 6:** Slew rate is measured between ±8V on the output with ±12V swing for ±15V supplies and ±2V on the output with ±3V swing for ±5V supplies.

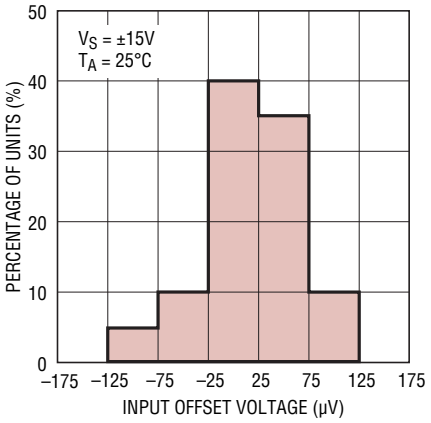
**Note 7:** Full-power bandwidth is calculated from the slew rate. FPBW = $SR/2\pi V_P$.

**Note 8:** This parameter is not 100% tested.

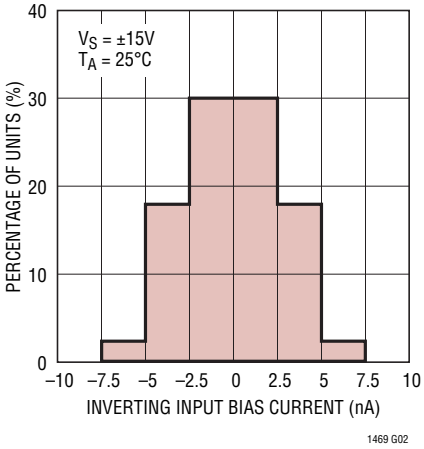
**Note 9:** ΔCMRR and ΔPSRR are defined as follows: 1) CMRR and PSRR are measured in µV/V on each amplifier; 2) the difference between the two sides is calculated in µV/V; 3) the result is converted to dB.

# TYPICAL PERFORMANCE CHARACTERISTICS

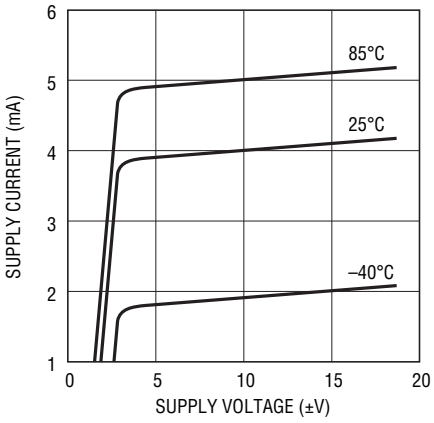
### Distribution of Input Offset Voltage



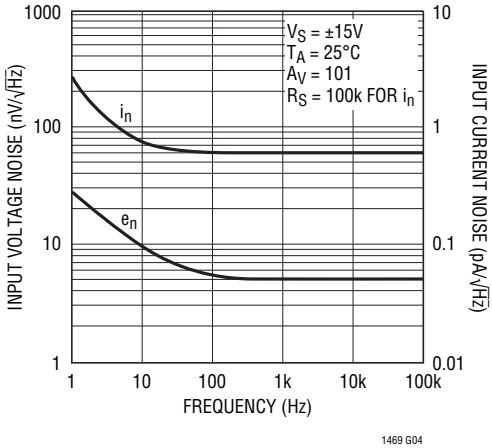

### Distribution of Inverting Input Bias Current



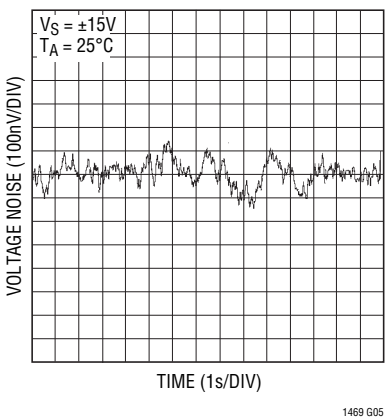

### Supply Current vs Supply Voltage and Temperature



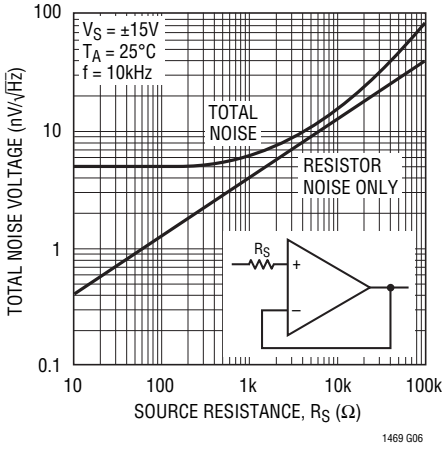

### Input Noise Spectral Density



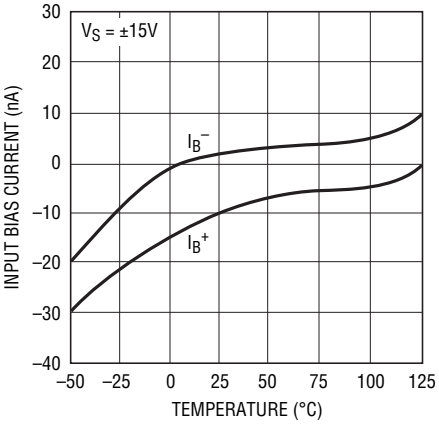

### 0.1Hz to 10Hz Voltage Noise



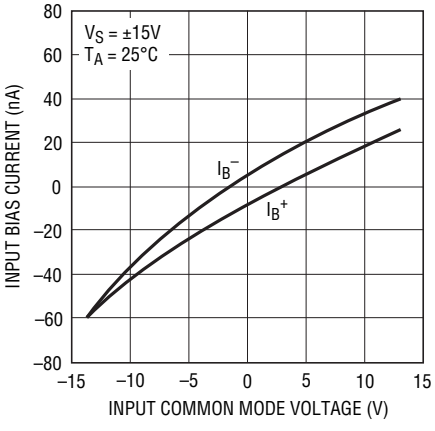

### Total Noise vs Unmatched Source Resistance



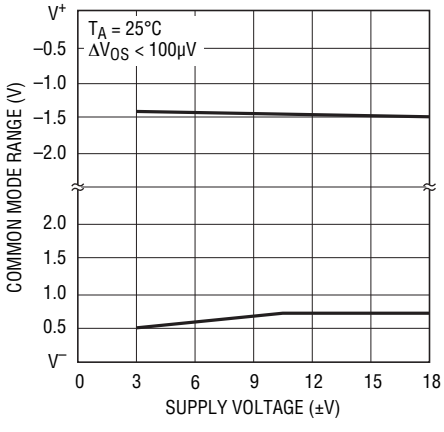

### Input Bias Current vs Temperature




### Input Bias Current vs Input Common Mode Voltage

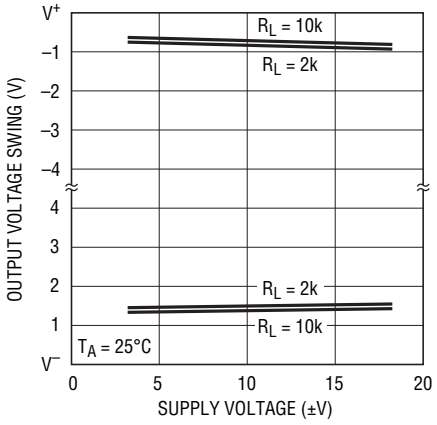



### Input Common Mode Range vs Supply Voltage



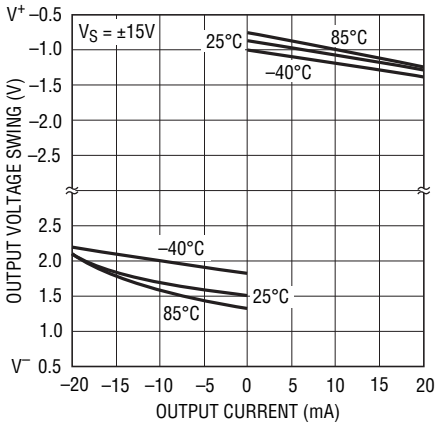
# TYPICAL PERFORMANCE CHARACTERISTICS

### Output Voltage Swing vs Supply Voltage



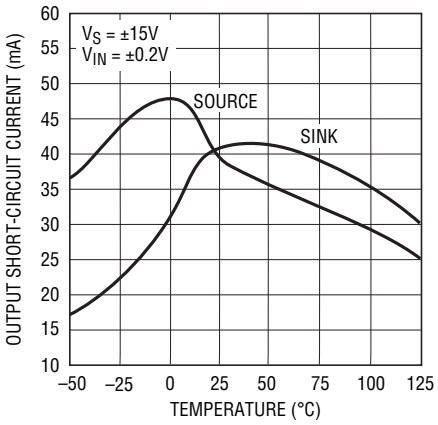

1469 G10

### Output Voltage Swing vs Load Current



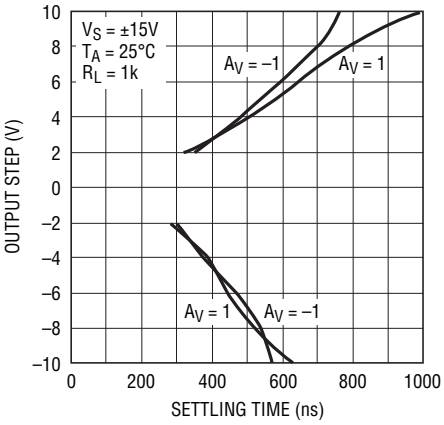

1469 G11

### Output Short-Circuit Current vs Temperature



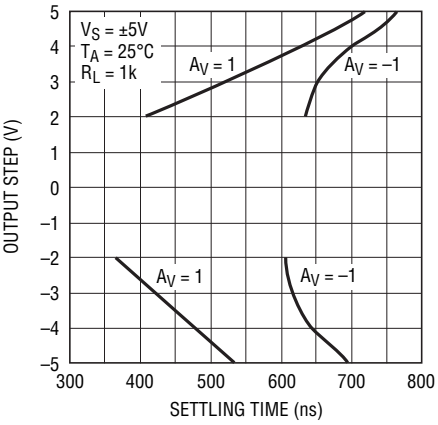

1469 G12

### Settling Time to 0.01% vs Output Step, $V_S = \pm 15V$



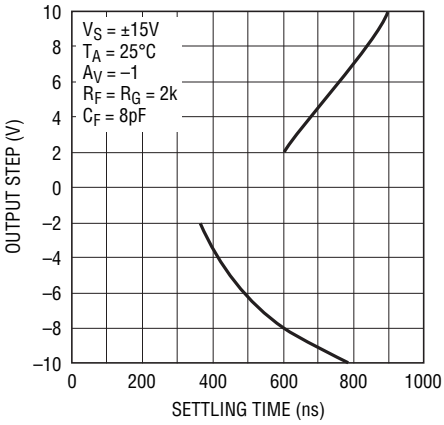

1469 G13

### Settling Time to 0.01% vs Output Step, $V_S = \pm 5V$



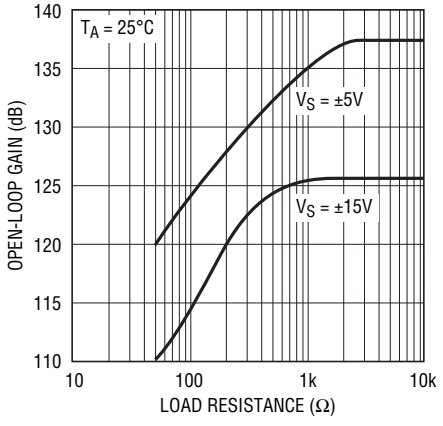

1469 G14

### Settling Time to 150µV vs Output Step



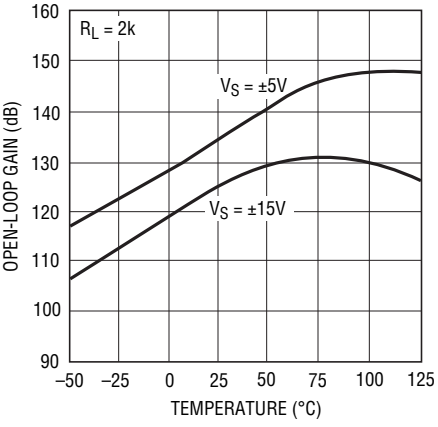

1469 G15

### Open-Loop Gain vs Resistive Load



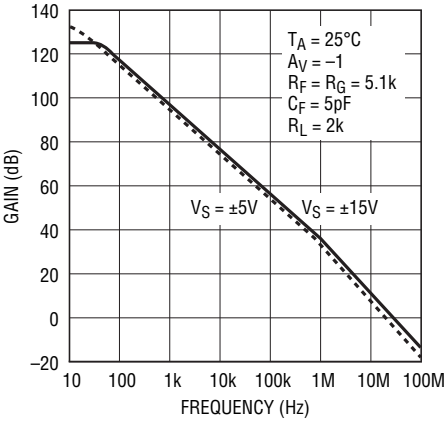

1469 G16

### Open-Loop Gain vs Temperature




1469 G17

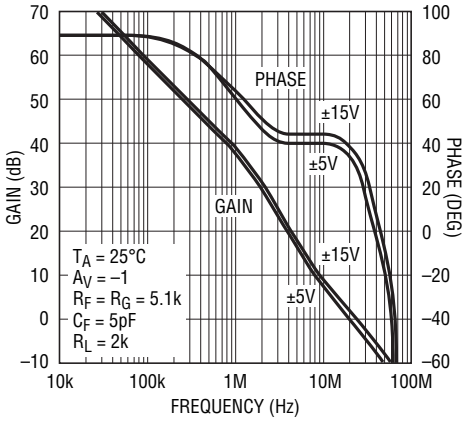
### Open-Loop Gain vs Frequency



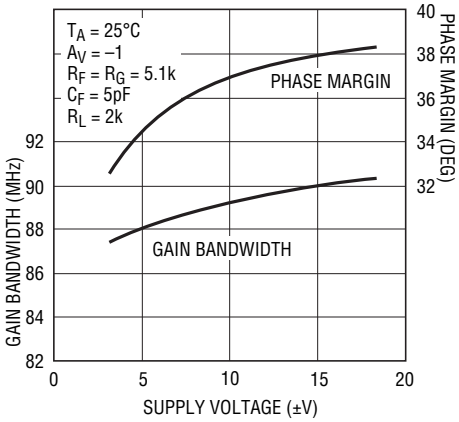

1469 G18

# TYPICAL PERFORMANCE CHARACTERISTICS

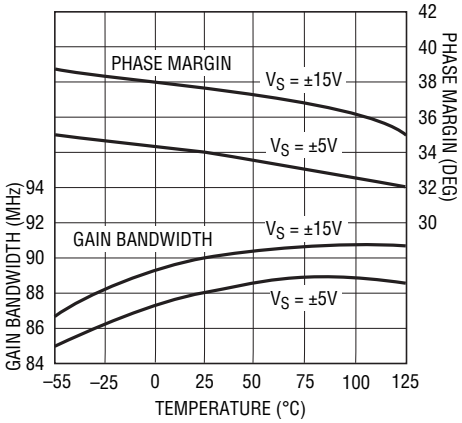
### Open-Loop Gain and Phase vs Frequency



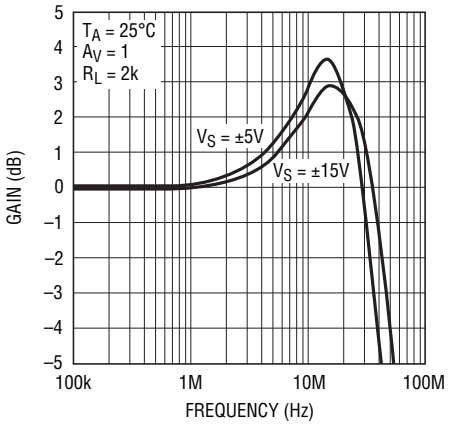

### Gain Bandwidth and Phase Margin vs Supply Voltage



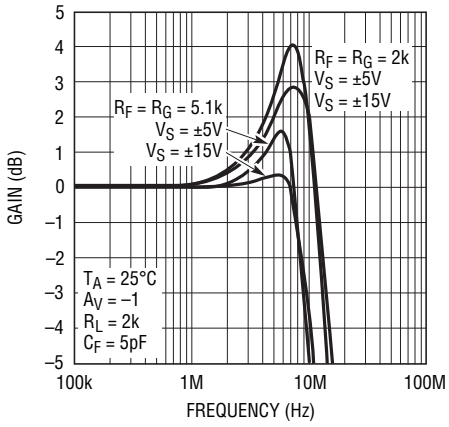

### Gain Bandwidth and Phase Margin vs Temperature



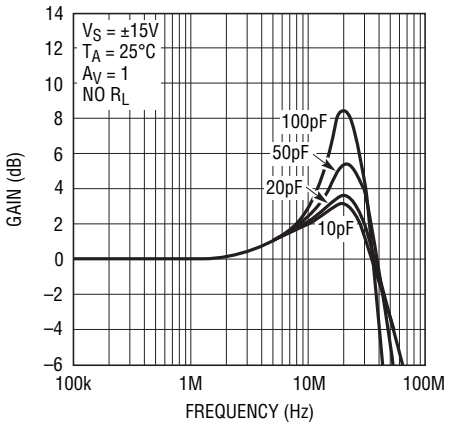

### Gain vs Frequency, $A_V = 1$



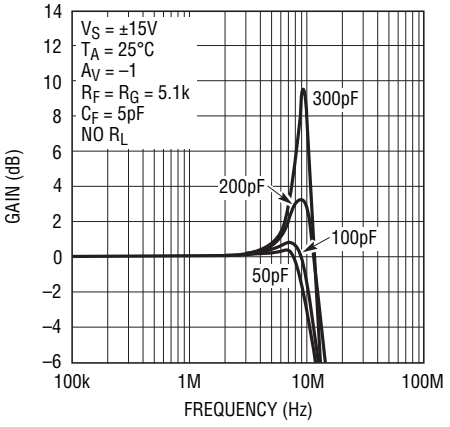

### Gain vs Frequency, $A_V = -1$



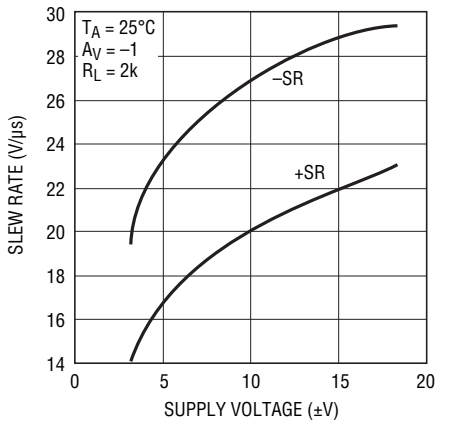

### Gain vs Frequency, $A_V = 1$



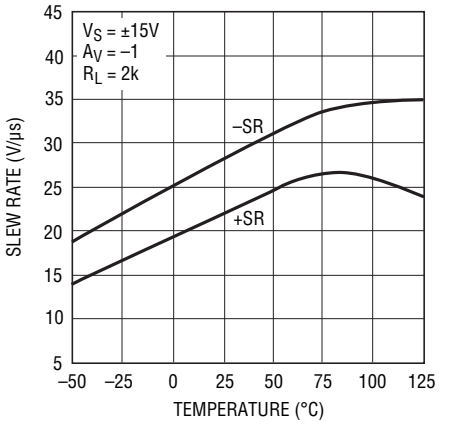

### Gain vs Frequency, $A_V = -1$




### Slew Rate vs Supply Voltage

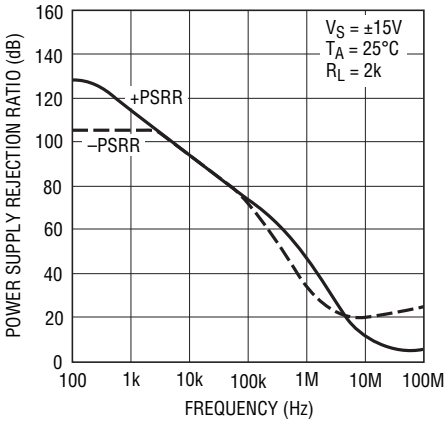



### Slew Rate vs Temperature



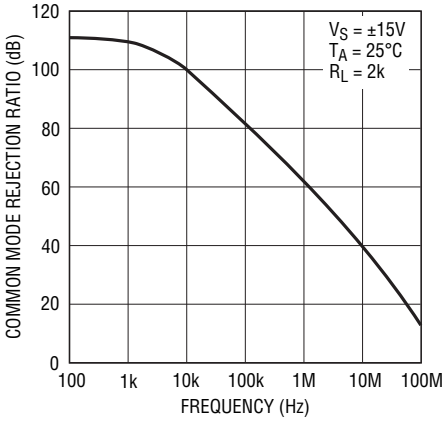
## TYPICAL PERFORMANCE CHARACTERISTICS

### Power Supply Rejection Ratio vs Frequency



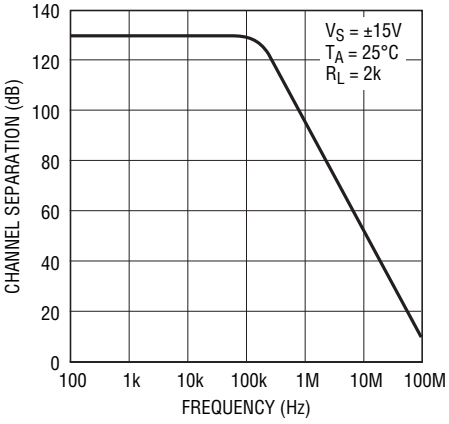

1469 G28

### Common Mode Rejection Ratio vs Frequency



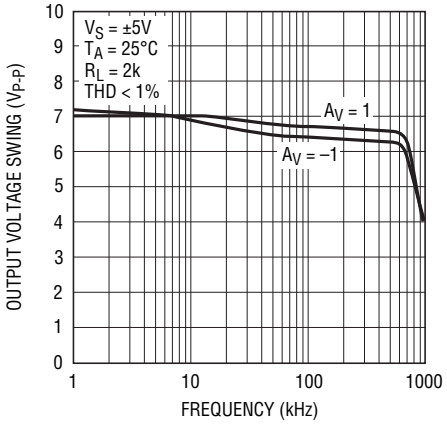

1469 G29

### Channel Separation vs Frequency



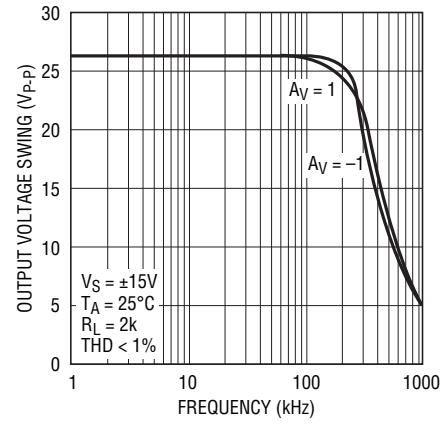

1469 G30

### Undistorted Output Swing vs Frequency, $V_S$ = ±5V



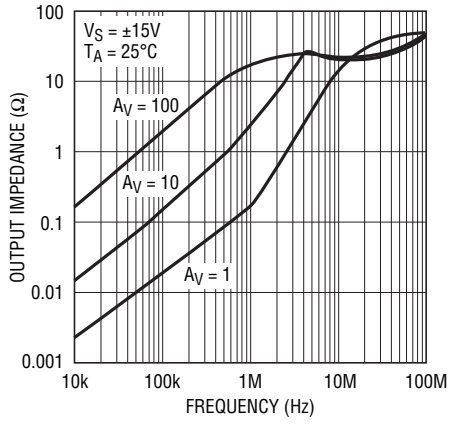

1469 G31

### Undistorted Output Swing vs Frequency, $V_S$ = ±15V



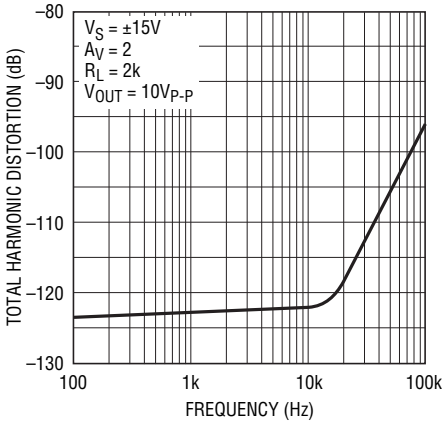

1469 G32

### Output Impedance vs Frequency



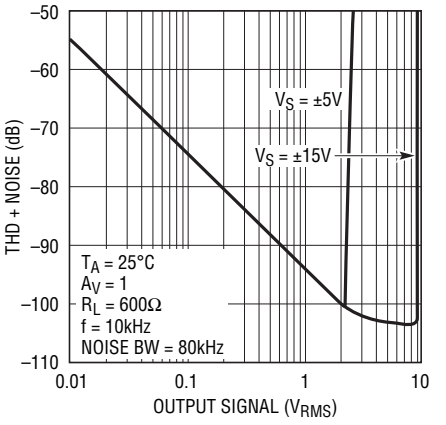

1469 G33

### Total Harmonic Distortion vs Frequency



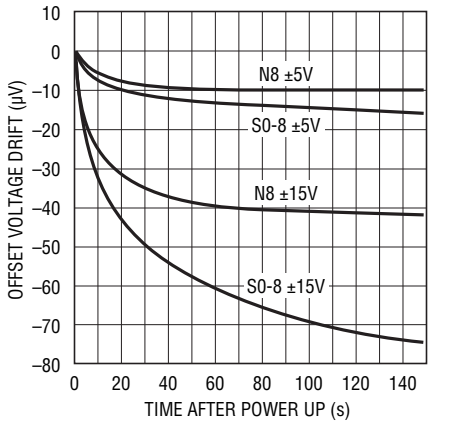

1469 G34

### Total Harmonic Distortion + Noise vs Amplitude




1469 G35

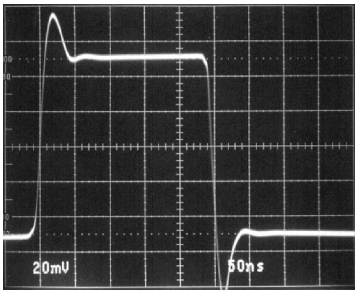
### Warm-Up Drift vs Time




1469 G36

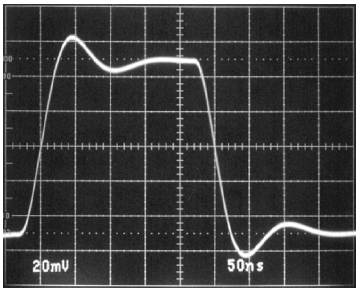
## TYPICAL PERFORMANCE CHARACTERISTICS

**Small-Signal Transient, $A_V = 1$**



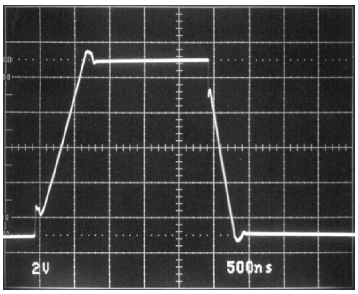

$V_S = \pm 15V$ 1469 G37

**Small-Signal Transient, $A_V = -1$**



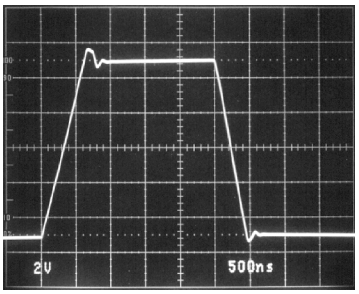

$V_S = \pm 15V$ 1469 G38

**Large-Signal Transient, $A_V = 1$**




$V_S = \pm 15V$ 1469 G39

**Large-Signal Transient, $A_V = -1$**




$V_S = \pm 15V$ 1469 G40

## APPLICATIONS INFORMATION

### Layout and Passive Components

The LT1469 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors (0.01µF to 0.1µF) in parallel with low ESR bypass capacitors (1µF to 10µF tantalum). For best DC performance, use "star" grounding techniques, equalize input trace lengths and minimize leakage (e.g., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum $I_B-$ specification).

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: for inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below).

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of

## APPLICATIONS INFORMATION

the amplifier. Air currents over device leads should be minimized, package leads should be short and the two input leads should be as close together as possible and maintained at the same temperature.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of value $C_F > R_G \bullet C_{IN}/R_F$ should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, $C_F$ should be greater than or equal to $C_{IN}$. An example would be a DAC I-to-V converter as shown on the front page of the data sheet where the DAC can have many tens of picofarads of output capacitance. Another example would be a gain of –1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor.

### Input Considerations

Each input of the LT1469 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If large differential input voltages are anticipated, limit the input current to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA.

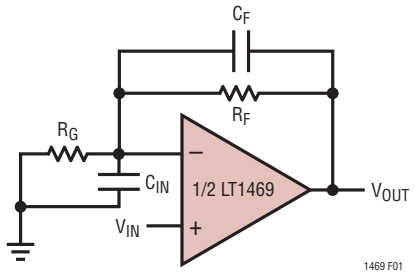



**Figure 1. Nulling Input Capacitance**

The LT1469 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1469 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

### Total Input Noise

The total input noise of the LT1469 is optimized for a source resistance between 1k and 20k. Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 1k, voltage noise of the amplifier dominates. When the source resistance is above 20k, the input noise current is the dominant contributor.

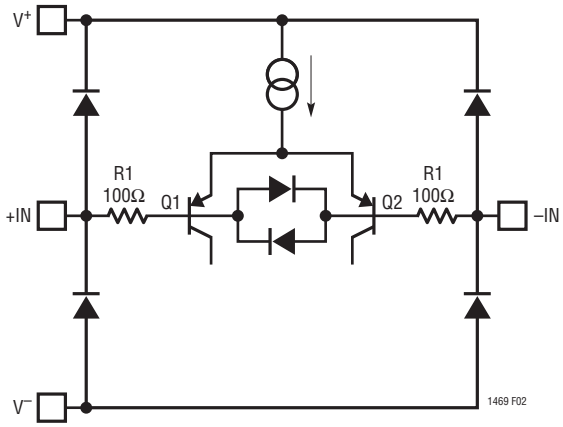



**Figure 2. Input Stage Protection**

## APPLICATIONS INFORMATION

### Capacitive Loading

The LT1469 drives capacitive loads of up to 100pF in unity-gain and 300pF in a gain of –1. When there is a need to drive a larger capacitive load, a small series resistor should be inserted between the output and the load. In addition, a capacitor should be added between the output and the inverting input as shown in Figure 3.

### Settling Time

The LT1469 is a single stage amplifier with an optimal thermal layout that leads to outstanding settling performance. Measuring settling even at the 12-bit level is very challenging, and at the 16-bit level requires a great deal of subtlety and expertise. Fortunately, there are two excellent Linear Technology reference sources for settling measurements—Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements and AN74 extends the state-of-the-art while concentrating on settling time with a 16-bit current output DAC input.

The settling of the DAC I-to-V converter on the front page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 15pF across the 12k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or 2µs. The actual settling time is 2.4µs at the output of the LT1469.

The RC output noise filter adds a slight settling time delay but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

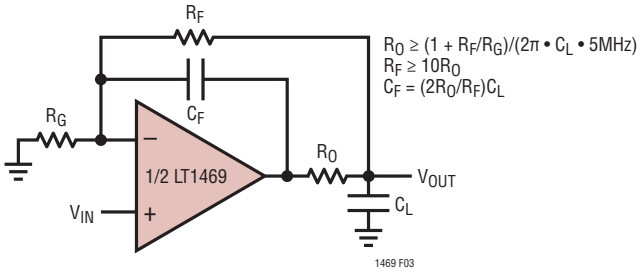
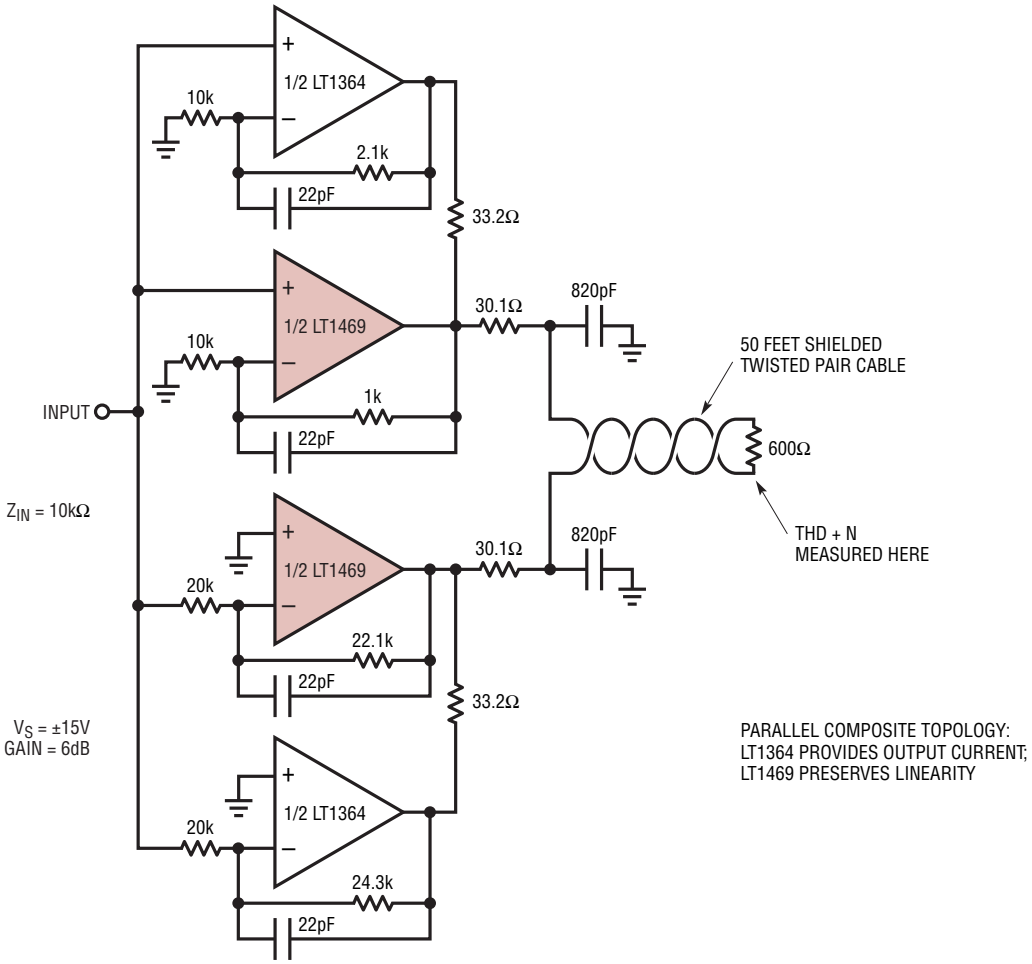



**Figure 3. Driving Capacitive Loads**

# TYPICAL APPLICATIONS

### Ultralow Distortion Balanced Audio Line Driver



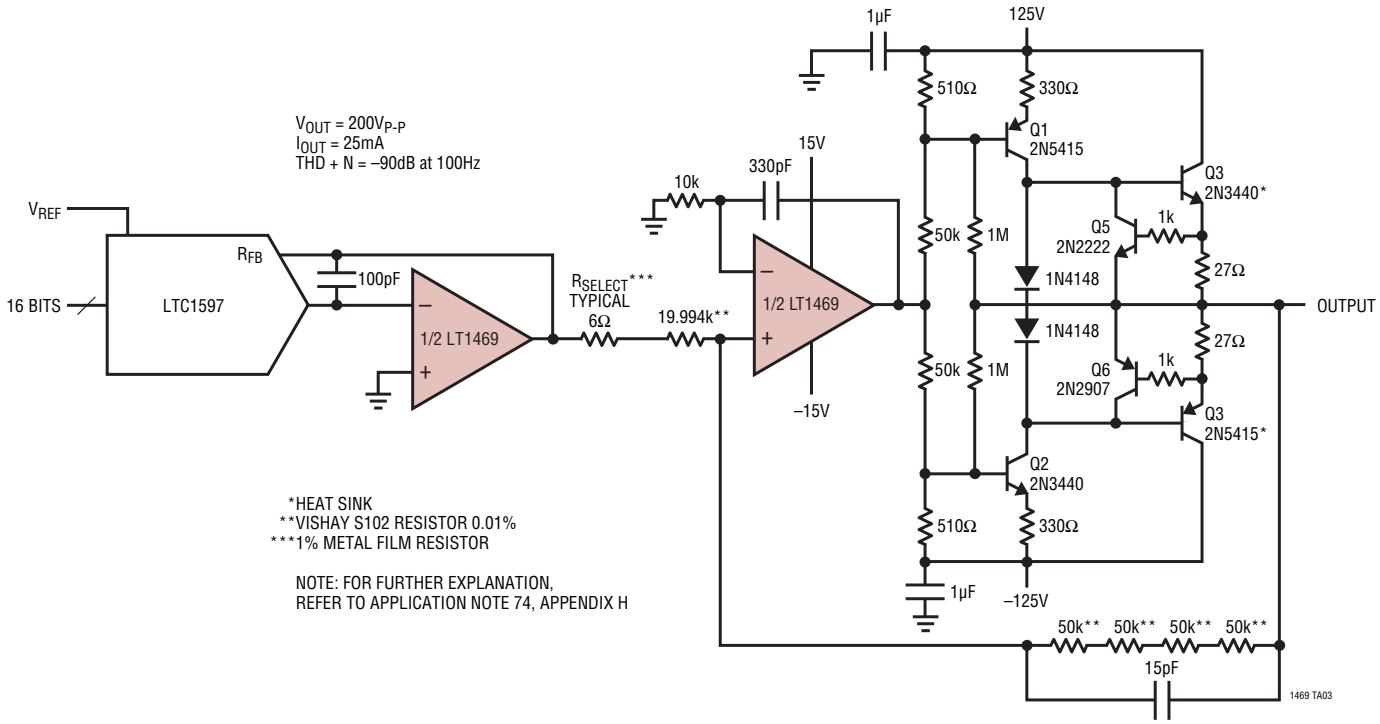

| TOTAL HARMONIC DISTORTION + NOISE | $V_{OUT}$ | FREQUENCY | MEASUREMENT BANDWIDTH |
|---|---|---|---|
| 0.00025% | $10V_{RMS}$ | 1kHz | 22kHz |
| 0.0008% | $10V_{RMS}$ | 20Hz TO 20kHz | 80kHz |
| 0.0006% | 26dBu | 1kHz | 22kHz |

1469 TA02

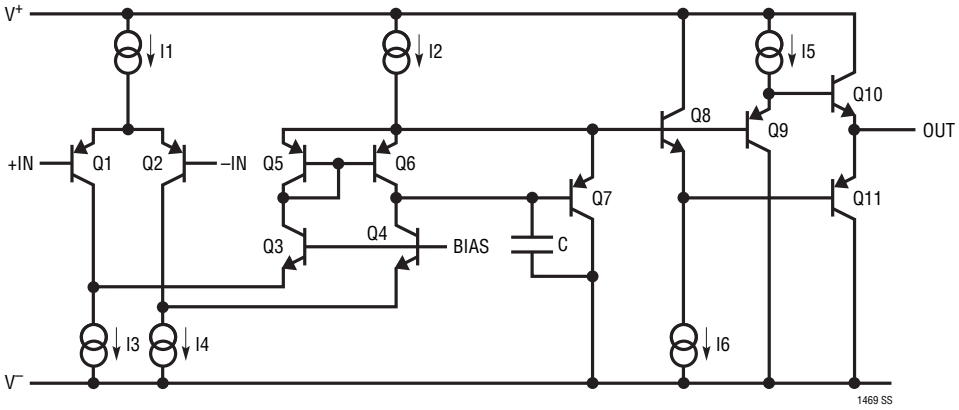
*1dBu = 1 milliwatt into 600Ω

# TYPICAL APPLICATIONS

**Extending 16-Bit DAC Performance to 200V Output Swing**

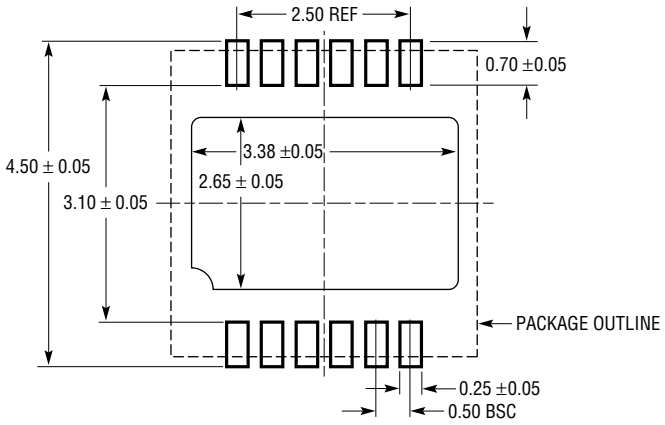


## SIMPLIFIED SCHEMATIC

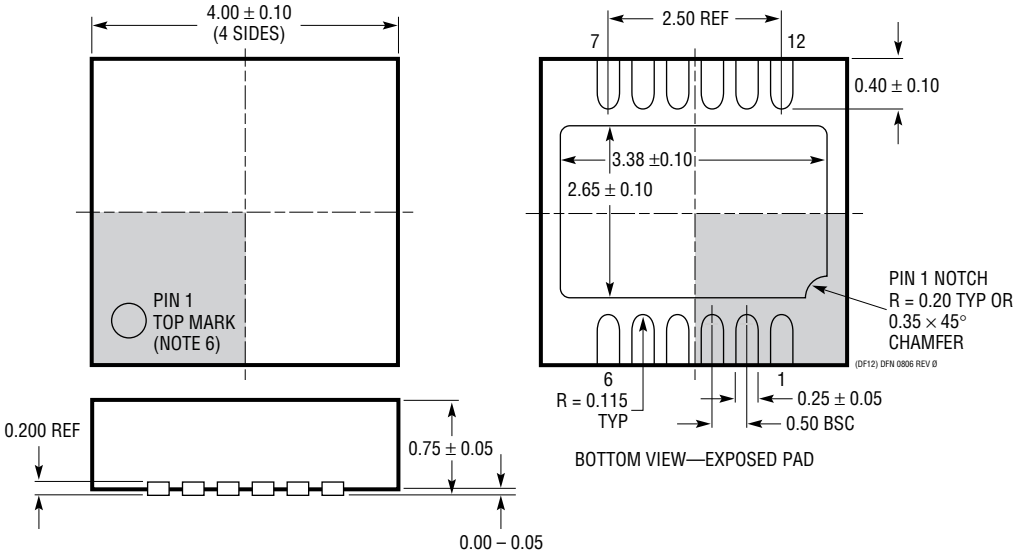


# PACKAGE DESCRIPTION

**DF Package**
**12-Lead Plastic DFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1733 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

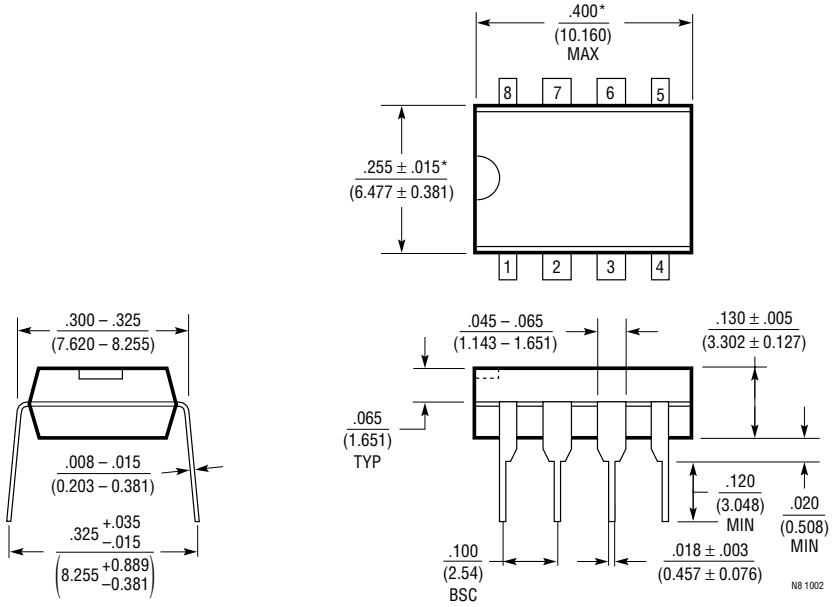



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

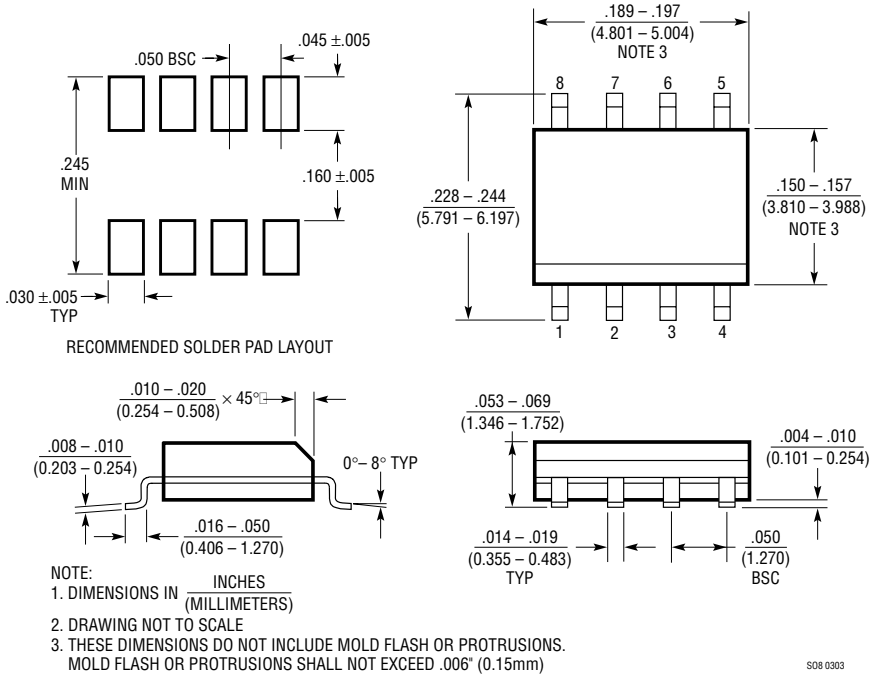
**N8 Package**
**8-Lead PDIP (Narrow 0.300)**
(Reference LTC DWG # 05-08-1510)




NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

**S8 Package**
**8-Lead Plastic Small Outline (Narrow 0.150)**
(Reference LTC DWG # 05-08-1610)




NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

## REVISION HISTORY (Revision history begins at Rev B)

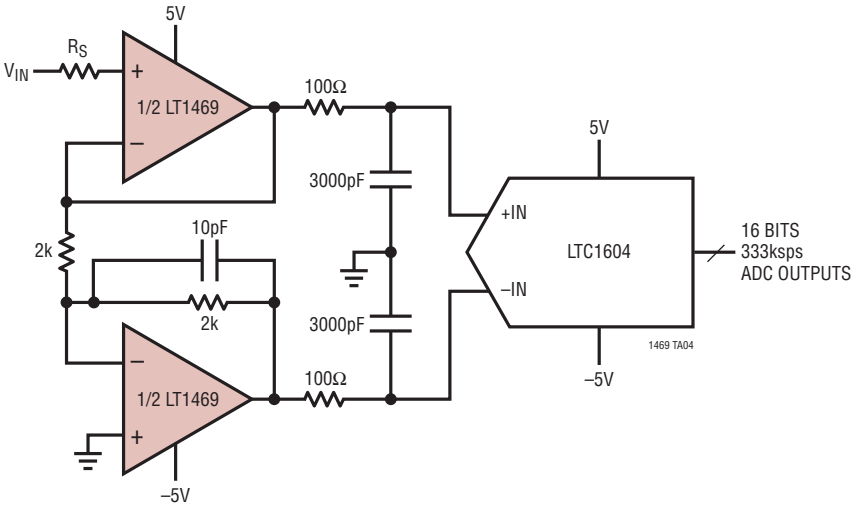
| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| B | 1/11 | Change to Electrical Characteristics | 3, 5, 6 |



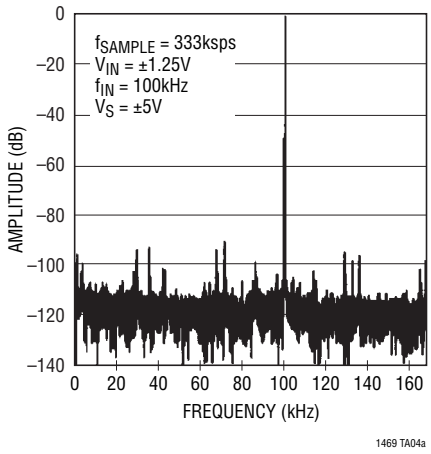
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

**16-Bit Accurate Single Ended to Differential ADC Buffer**




**4096 Point FFT of ADC Output**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT1167 | Precision Instrumentation Amplifier | Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity |
| LT1468 | Single 90MHz, 22V/µs, 16-Bit Accurate Op Amp | 75µV $V_{OS(MAX)}$, Single Version of LT1469 |
| LT1468-2 | Single 200MHz, 30V/µs, 16-Bit Accurate $A_V \geq 2$ Op Amp | 75µV $V_{OS(MAX)}$ |
| LT1469-2 | Dual 200MHz, 30V/µs, 16-Bit Accurate $A_V \geq 2$ Op Amp | 75µV $V_{OS(MAX)}$ |
| LTC1595/LTC1596 | 16-Bit Serial Multiplying $I_{OUT}$ DAC | ±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade |
| LTC1597 | 16-Bit Parallel Multiplying $I_{OUT}$ DAC | ±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors |
| LTC1604 | 16-Bit, 333ksps Sampling ADC | ±2.5V Input, SINAD = 90dB, THD = –100dB |
| LTC1605 | Single 5V, 16-Bit, 100ksps Sampling ADC | Low Power, ±10V Inputs, Parallel/Byte Interface |
| LT1723 | Dual 200MHz, 70V/µs Low Noise Precision Op Amp | $V_S \leq \pm 5V$, $e_n = 3.8nV/\sqrt{Hz}$, –85dBc at 1MHz |
| LT1801 | Dual 80MHz, 25V/µs Low Power Rail-to-Rail Precision Op Amp | $V_S \leq \pm 5V$, $I_{CC} = 1.6mA$, $V_{OS} \leq 350\mu V$ |
| LT6221 | Dual 60MHz, 20V/µs Low Power Rail-to-Rail Precision Op Amp | $V_S \leq \pm 5V$, $I_{CC} = 0.9mA$, $V_{OS} \leq 350\mu V$ |
| LTC6244HV | Dual 50MHz, Low Noise, Precision CMOS Op Amp | $V_S \leq \pm 5V$, $V_{OS} \leq 100\mu V$, $I_B \leq 75pA$ |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