

## Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: -40°C to +85°C
  - Automotive-A: -40°C to +85°C
  - Automotive-E: -40°C to +125°C
- Wide voltage range: 2.20V to 3.60V
- Pin compatible with CY62136V, CY62136CV30/CV33, and CY62136EV30
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 5  $\mu$ A (Industrial)
- Ultra low active power
  - Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

## Functional Description

The CY62136FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an

automatic power down feature that significantly reduces power consumption by 90 percent when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}$  HIGH). The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when:

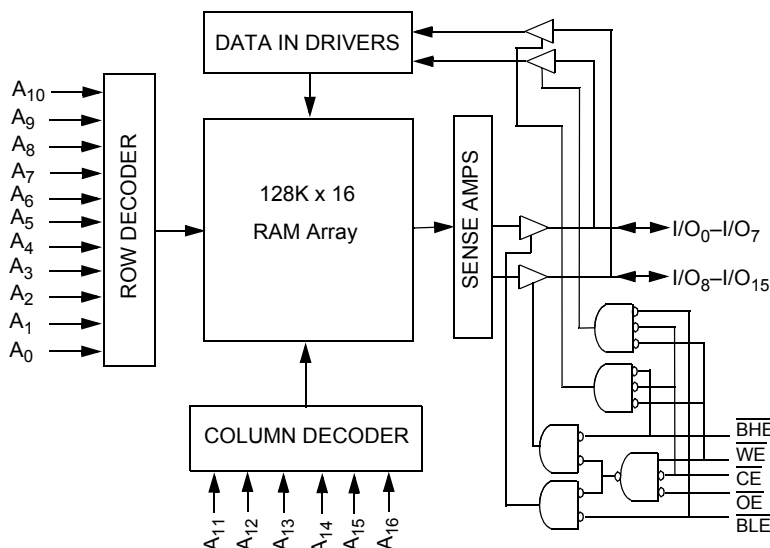
- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- Write operation is active ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the "Truth Table" on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

## Logic Block Diagram



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY62136FV30LL	Industrial/Auto-A	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5
	Auto-E	2.2	3.0	3.6	55	2	3	15	25	1	20

## Pin Configuration

Figure 1. 48-Ball VFBGA Pinout <sup>[2, 3]</sup>

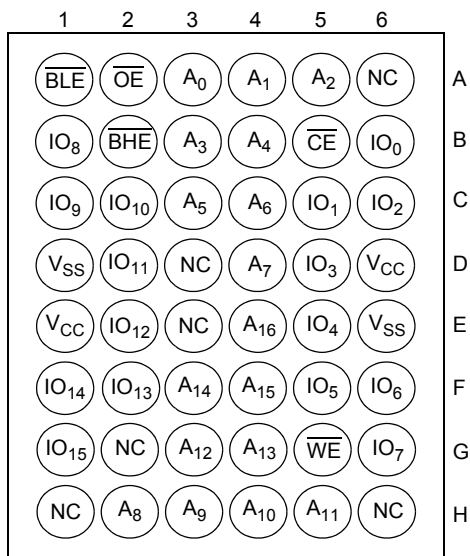
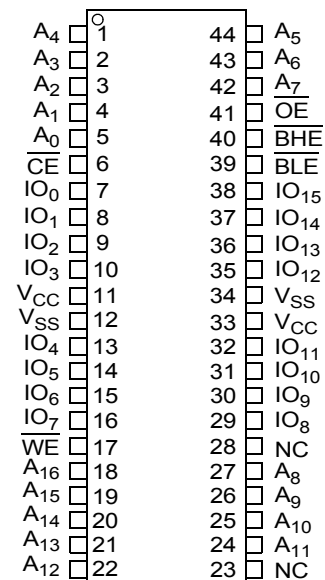


Figure 2. 44-Pin TSOP II <sup>[2]</sup>



### Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, and H6 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb, respectively.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with

Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground

Potential ..... -0.3V to 3.9V ( $V_{CC(max)}$  + 0.3V)

DC Voltage Applied to Outputs

in High Z State <sup>[4, 5]</sup> ..... -0.3V to 3.9V ( $V_{CC(max)}$  + 0.3V)

DC Input Voltage <sup>[4, 5]</sup> ..... -0.3V to 3.9V ( $V_{CC(max)}$  + 0.3V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(MIL-STD-883, Method 3015)

Latch up Current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[6]</sup>
CY62136FV30LL	Ind'I/Auto-A	-40°C to +85°C	2.2V to 3.6V
	Auto-E	-40°C to +125°C	

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-45 (Industrial/Auto-A)			-55 (Auto-E)			Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Typ <sup>[1]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	2.0			2.0			V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6							
V <sub>OL</sub>	Output LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7			0.4			0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6							
V <sub>IH</sub>	Input HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	1.8		V <sub>CC</sub> + 0.3	1.8		V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6							
V <sub>IL</sub>	Input LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	-0.3		0.6	-0.3		0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6							
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-4		+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-4		+4	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub>		13	18		15	25	mA
		f = 1 MHz		1.6	2.5		2	3	
I <sub>SB1</sub>	Automatic CE Power Down Current — CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE, BHE, and BLE), V <sub>CC</sub> = 3.60V		1	5		1	20	μA
I <sub>SB2</sub> <sup>[7]</sup>	Automatic CE Power Down Current — CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V		1	5		1	20	μA

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF

### Notes

4. V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.

5. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.

6. Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.

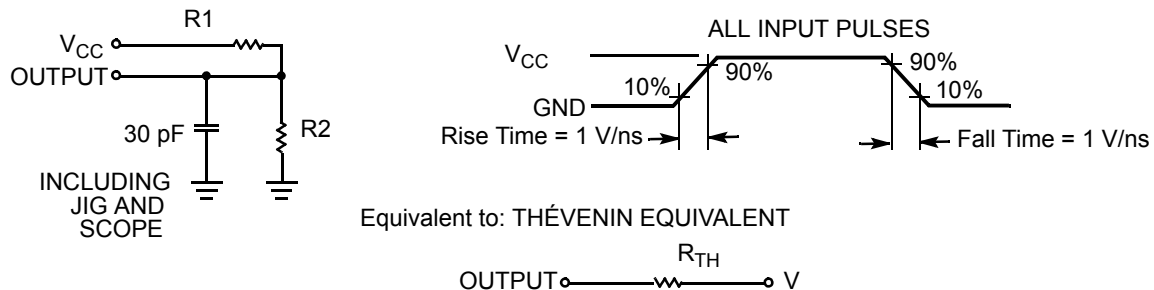
7. Only chip enable (CE) and byte enables (BHE and BLE) are tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> specification. Other inputs can be left floating.

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA	TSOP II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	75	77	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		10	13	°C/W

**Figure 3. AC Test Loads and Waveforms**



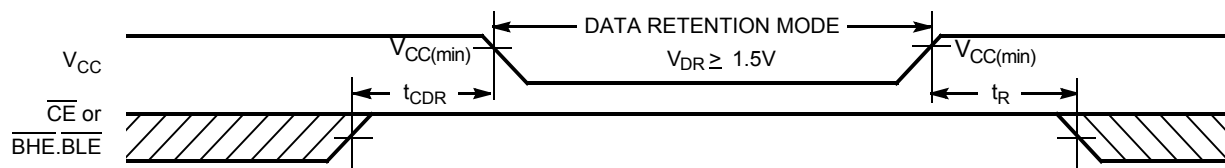
Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
R <sub>TH</sub>	8000	645	$\Omega$
V <sub>TH</sub>	1.20	1.75	V

## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub> <sup>[7]</sup>	Data Retention Current	V <sub>CC</sub> = 1.5V, $\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V			4	μA
		Industrial/Auto-A				
		Auto-E			12	
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Figure 4. Data Retention Waveform<sup>[10]</sup>**



### Notes

8. Tested initially and after any design or process changes that may affect these parameters.

9. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

10. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling chip enable signals or by disabling both BHE and BLE.

## Switching Characteristics

Over the Operating Range <sup>[11, 12]</sup>

Parameter	Description	-45 (Industrial/Auto-A)		-55 (Auto-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		45		55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[13]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[13, 14]</sup>		18		20	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[13]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[13, 14]</sup>		18		20	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power Down		45		55	ns
t <sub>DBE</sub>	$\overline{BLE/BHE}$ LOW to Data Valid		22		25	ns
t <sub>LZBE</sub>	$\overline{BLE/BHE}$ LOW to Low Z <sup>[13]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE/BHE}$ HIGH to High Z <sup>[13, 14]</sup>		18		20	ns
Write Cycle <sup>[15]</sup>						
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	35		40		ns
t <sub>AW</sub>	Address Setup to Write End	35		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		40		ns
t <sub>BW</sub>	$\overline{BLE/BHE}$ LOW to Write End	35		40		ns
t <sub>SD</sub>	Data Setup to Write End	25		25		ns
t <sub>HD</sub>	Data Hold From Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[13, 14]</sup>		18		20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[13]</sup>	10		10		ns

### Notes

11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" on page 4.
12. AC timing parameters are subject to byte enable signals ( $\overline{BHE}$  or  $\overline{BLE}$ ) not switching when chip is disabled. Please see application note [AN13842](#) for further clarification.
13. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
14.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
15. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals are ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 5. Read Cycle No.1: Address Transition Controlled. [16, 17]

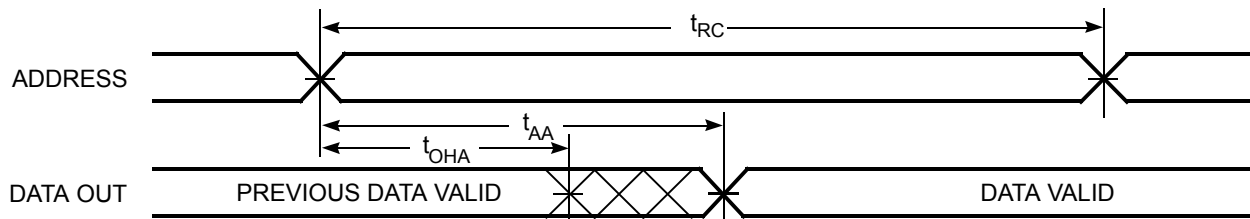
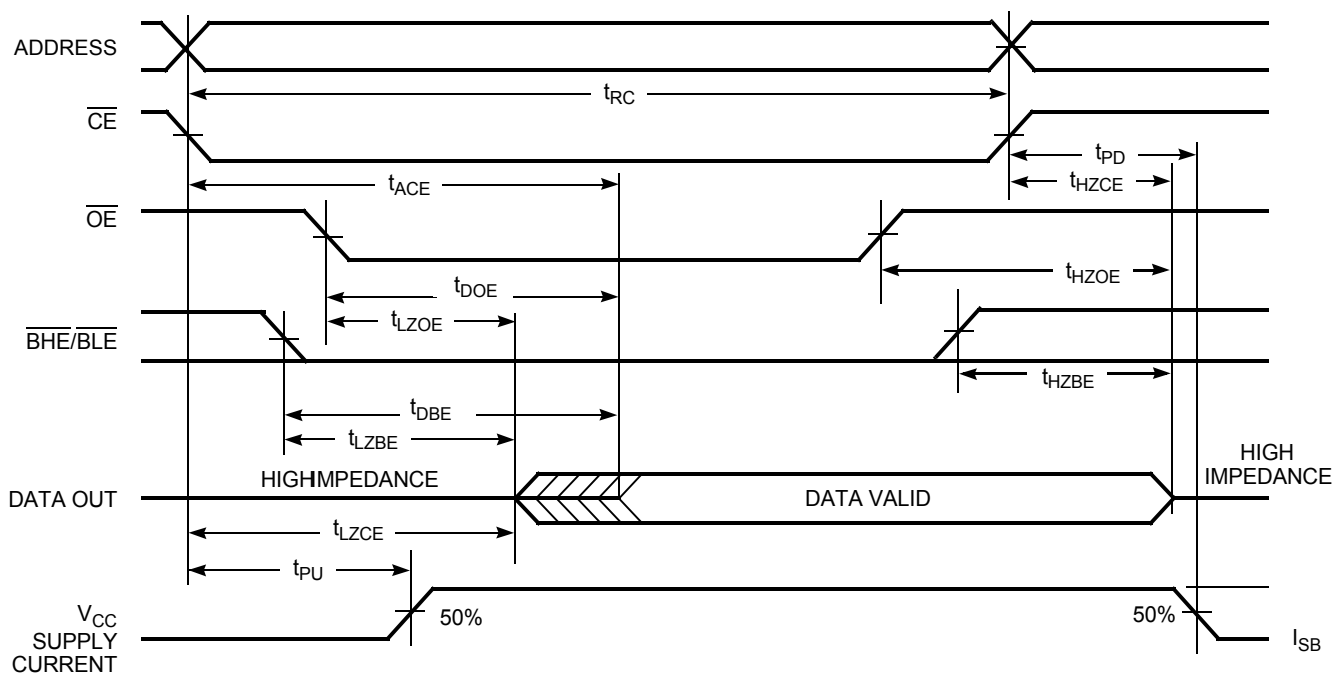


Figure 6. Read Cycle No. 2:  $\overline{OE}$  Controlled [17, 18]

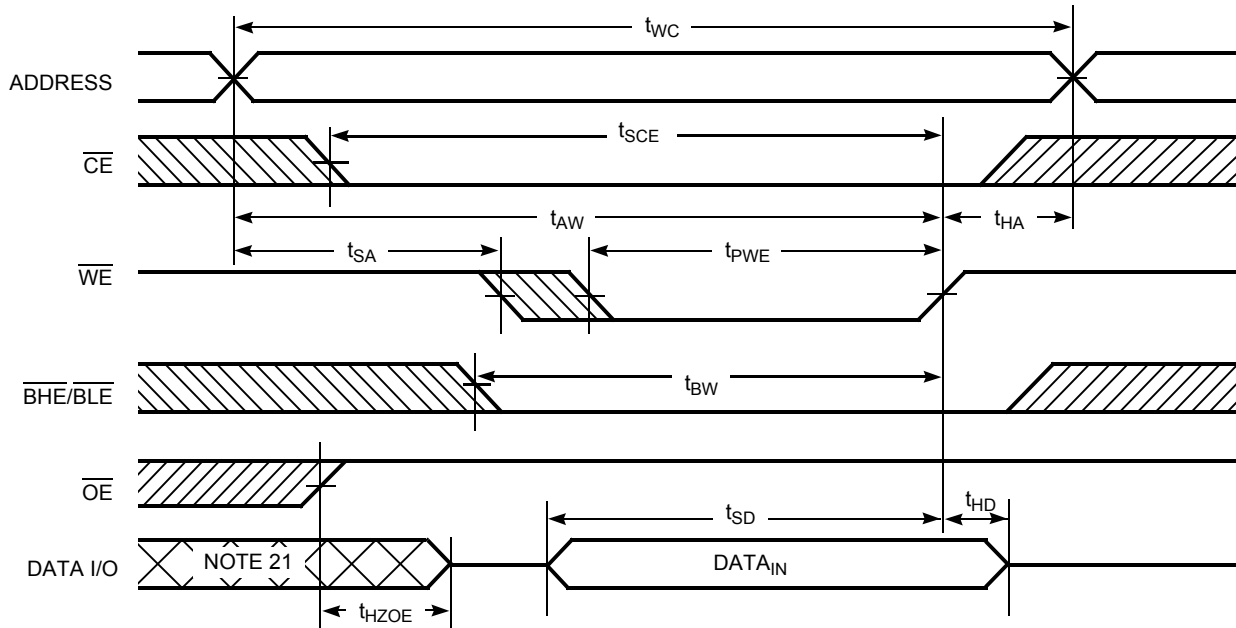


### Notes

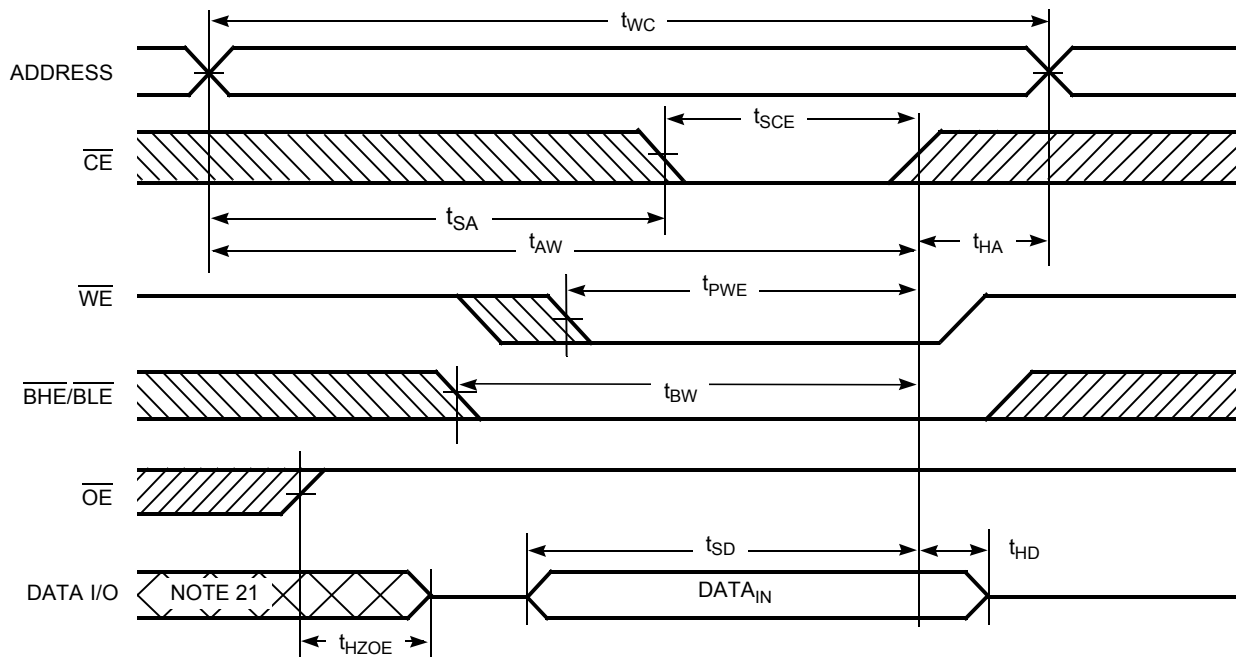
16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$  and  $\overline{BLE}$  =  $V_{IL}$ .
17.  $\overline{WE}$  is HIGH for read cycle.
18. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No 1:  $\overline{\text{WE}}$  Controlled** [15, 19, 20]



**Figure 8. Write Cycle 2:  $\overline{\text{CE}}$  Controlled** [15, 19, 20]

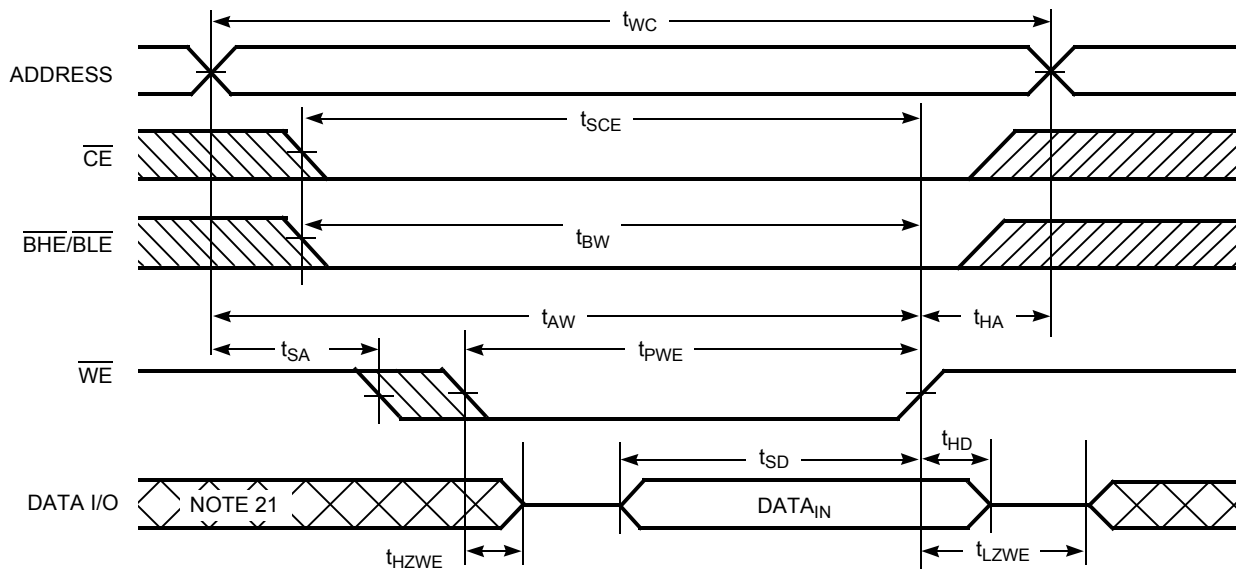


### Notes

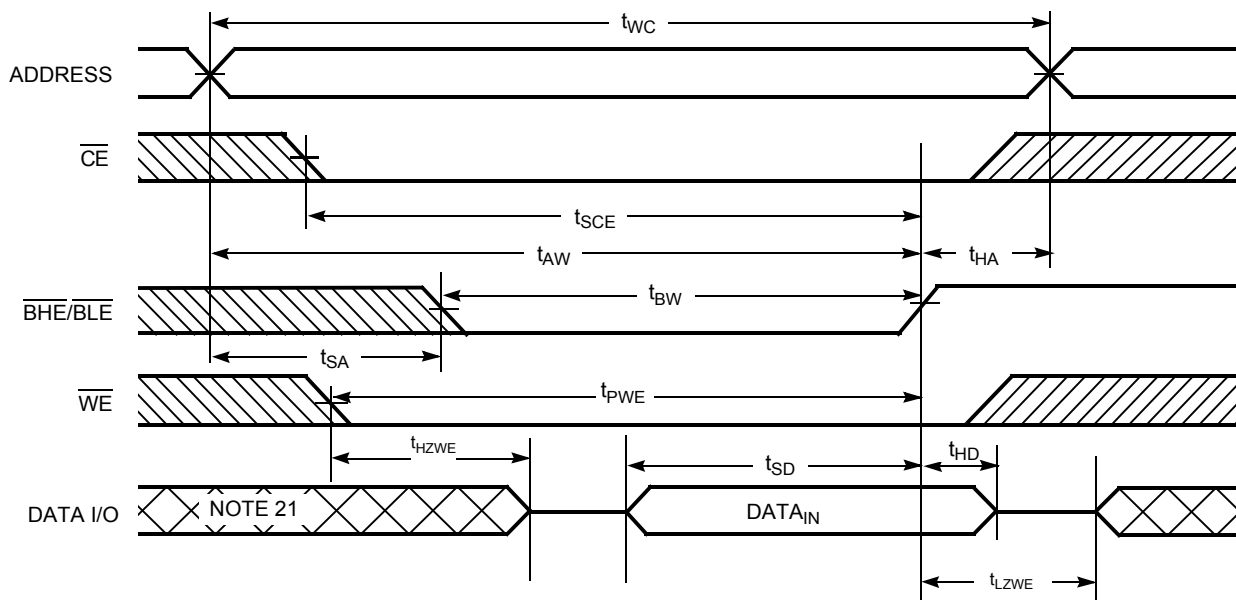
19. Data IO is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
20. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\text{WE} = V_{\text{IH}}$ , the output remains in a high impedance state.
21. During this period, the IOs are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 9. Write Cycle 3:  $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW [20]**



**Figure 10. Write Cycle 4:  $\overline{\text{BHE/BLER}}$  Controlled,  $\overline{\text{OE}}$  LOW [20]**



**Truth Table**

<b><math>\overline{\text{CE}}</math></b>	<b><math>\overline{\text{WE}}</math></b>	<b><math>\overline{\text{OE}}</math></b>	<b><math>\overline{\text{BHE}}</math></b>	<b><math>\overline{\text{BLE}}</math></b>	<b>Inputs or Outputs</b>	<b>Mode</b>	<b>Power</b>
H	X	X	X	X	High Z	Deselect or Power Down	Standby ( $I_{\text{SB}}$ )
X	X	X	H	H	High Z	Deselect or Power Down	Standby ( $I_{\text{SB}}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{\text{CC}}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{\text{CC}}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{\text{CC}}$ )

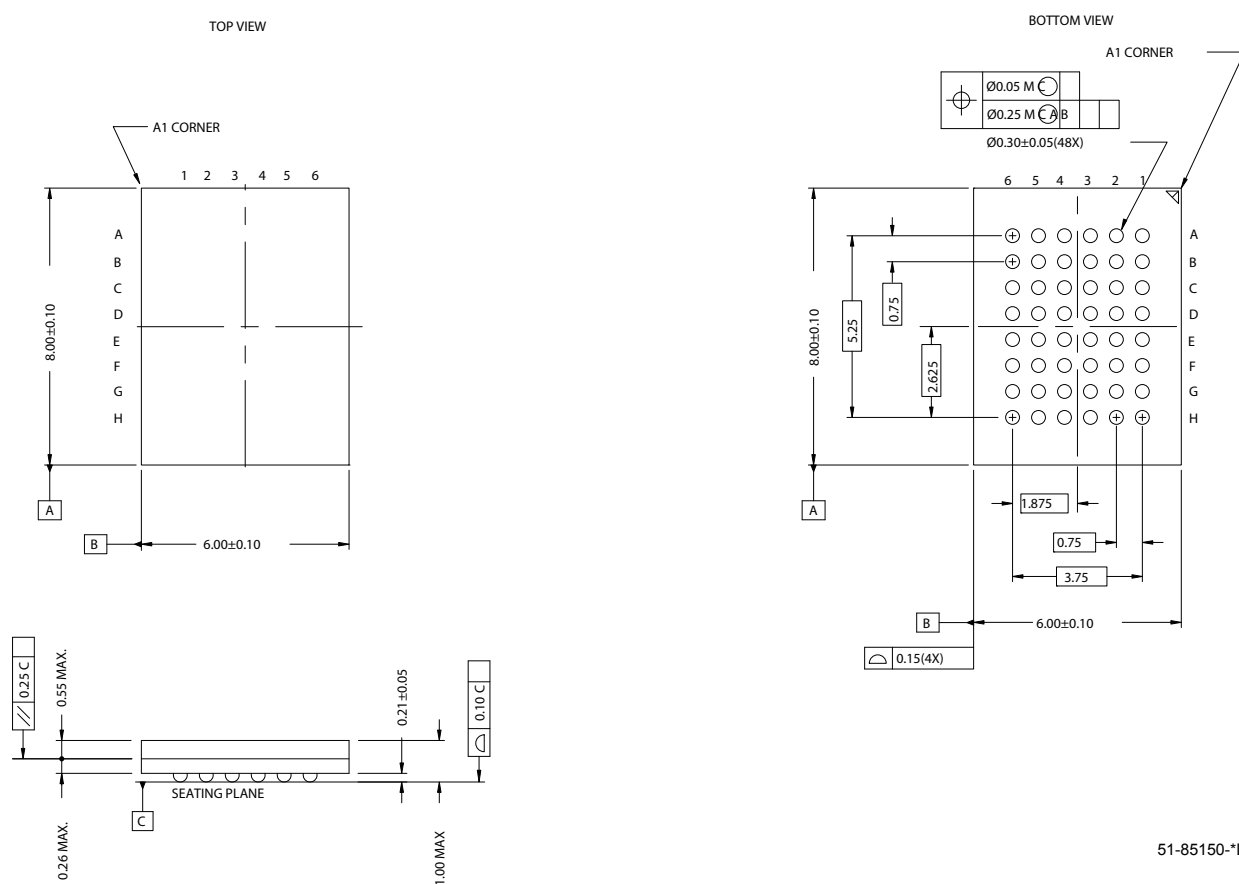
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136FV30LL-45BVXI	51-85150	48-Ball VFBGA (Pb-Free)	Industrial
	CY62136FV30LL-45ZSXI	51-85087	44-Pin TSOP II (Pb-Free)	
	CY62136FV30LL-45ZSXA	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-A
55	CY62136FV30LL-55ZSXE	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-E

Contact your local Cypress sales representative for availability of these parts.

## Package Diagrams

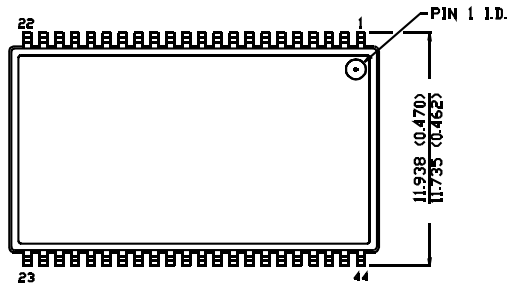
**Figure 11. 48-Ball VFBGA (6 x 8 x 1 mm)**



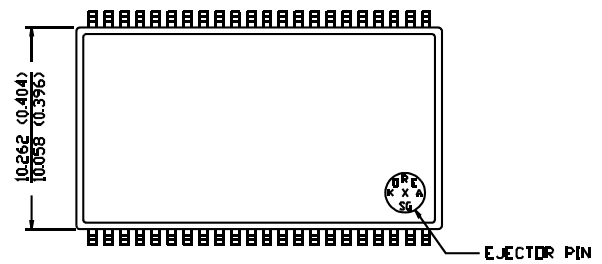
Package Diagrams (continued)

Figure 12. 44-Pin TSOP II

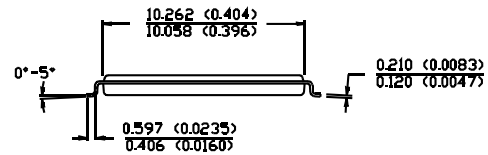
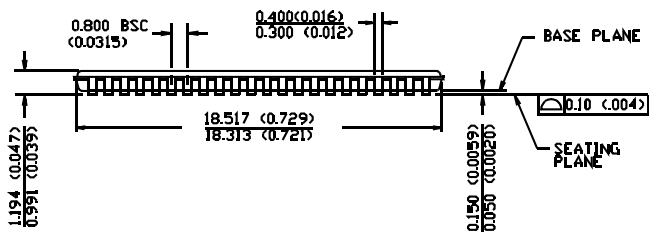
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-\*A

## Document History Page

Document Title: CY62136FV30 MoBL® 2 Mbit (128K x 16) Static RAM Document Number: 001-08402				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	467351	See ECN	NXR	New datasheet
*A	797956	See ECN	VKN	Converted from preliminary to final Changed $I_{SB1(typ)}$ and $I_{SB1(max)}$ specification from 0.5 $\mu A$ to 1.0 $\mu A$ and 2.5 $\mu A$ to 5.0 $\mu A$ , respectively Changed $I_{SB2(typ)}$ and $I_{SB2(max)}$ specification from 0.5 $\mu A$ to 1.0 $\mu A$ and 2.5 $\mu A$ to 5.0 $\mu A$ , respectively Changed $I_{CCDR(typ)}$ and $I_{CCDR(max)}$ specification from 0.5 $\mu A$ to 1.0 $\mu A$ and 2.5 $\mu A$ to 4.0 $\mu A$ , respectively Changed $I_{CC(max)}$ specification from 2.25 $\mu A$ to 2.5 $\mu A$
*B	869500	See ECN	VKN	Added Automotive information Updated Ordering information table Added footnote 12 related to $t_{ACE}$
*C	901800	See ECN	VKN	Added footnote 9 related to $I_{SB2}$ and $I_{CCDR}$ Made footnote 13 applicable to AC parameters from $t_{ACE}$
*D	1371124	See ECN	VKN/AESA	Converted Automotive information from preliminary to final Changed $I_{IX}$ min spec from -1 $\mu A$ to -4 $\mu A$ and $I_{IX}$ max spec from +1 $\mu A$ to +4 $\mu A$ Changed $I_{OZ}$ min spec from -1 $\mu A$ to -4 $\mu A$ and $I_{OZ}$ max spec from +1 $\mu A$ to +4 $\mu A$ Changed $t_{DBE}$ spec from 55 ns to 25 ns for automotive part
*E	2594937	10/22/08	NXR/PYRS	Added Automotive-A information Changed $t_{LZBE}$ from 10 ns to 5 ns for -55.
*F	2675375	03/17/2009	VKN/PYRS	Corrected typo on page 2 (Corrected $I_{SB2}$ unit to $\mu A$ from mA)

## Sales, Solutions, and Legal Information

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LCD Drive	<a href="http://psoc.cypress.com/lcd-drive">psoc.cypress.com/lcd-drive</a>
CAN 2.0b	<a href="http://psoc.cypress.com/can">psoc.cypress.com/can</a>
USB	<a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>

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