

# M66312P/FP

## 8-Bit LED Driver with Shift Register and Latched 3-State Outputs

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### Description

M66312 is a LED array driver having a 8-bit serial input and parallel output shiftregister function with 3-state output latch.

This product guarantees the output electric current of 16 mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

### Features

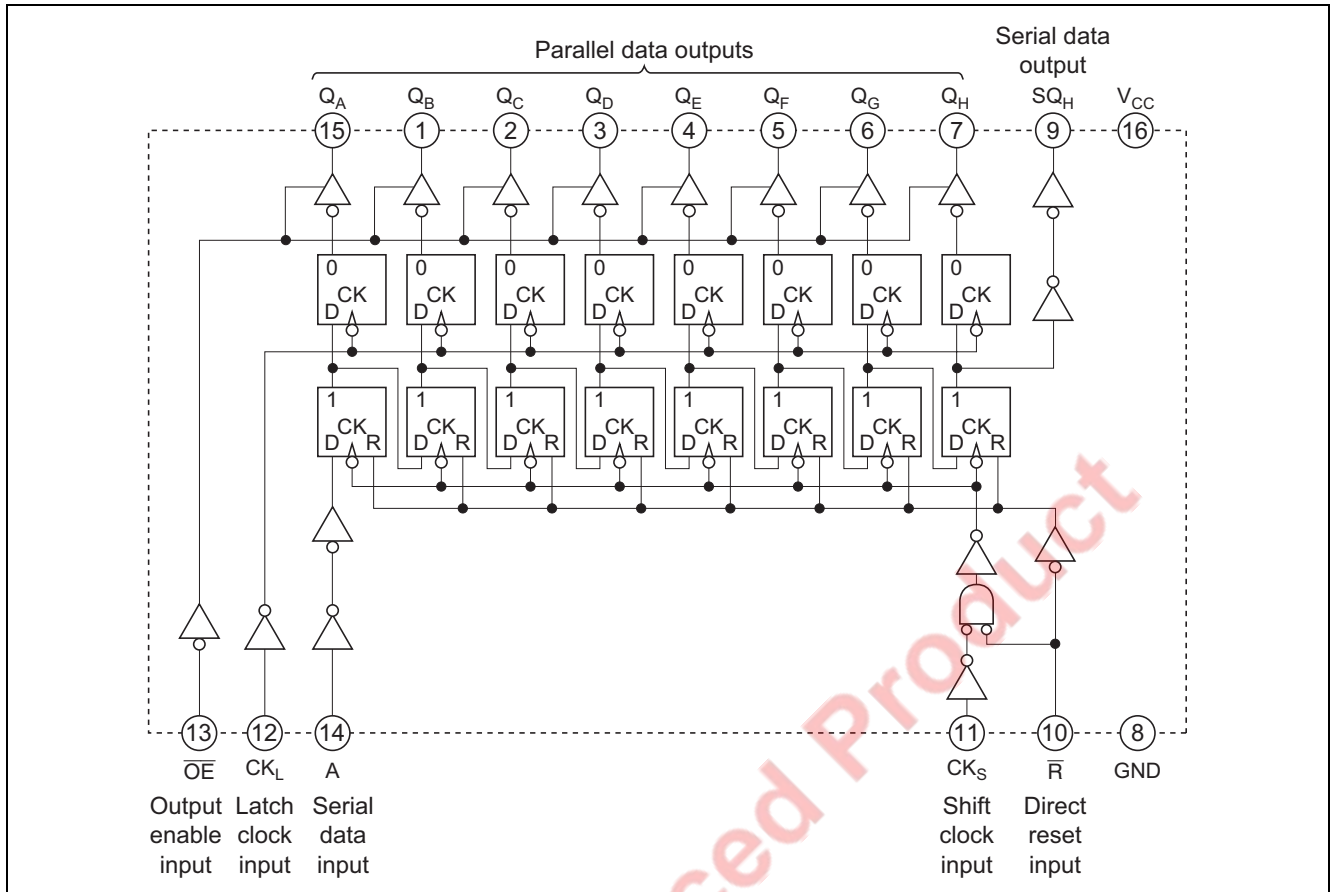
- High output current  $I_{OL} = 16 \text{ mA}$ ,  $I_{OH} = -16 \text{ mA}$
- High speed (clock frequency): 30 MHz (typ)  
( $C_L = 50 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ )
- Low power dissipation: 20  $\mu\text{W}$ /package (max)  
( $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range:  $T_a = -40$  to  $+85^\circ\text{C}$

### Application

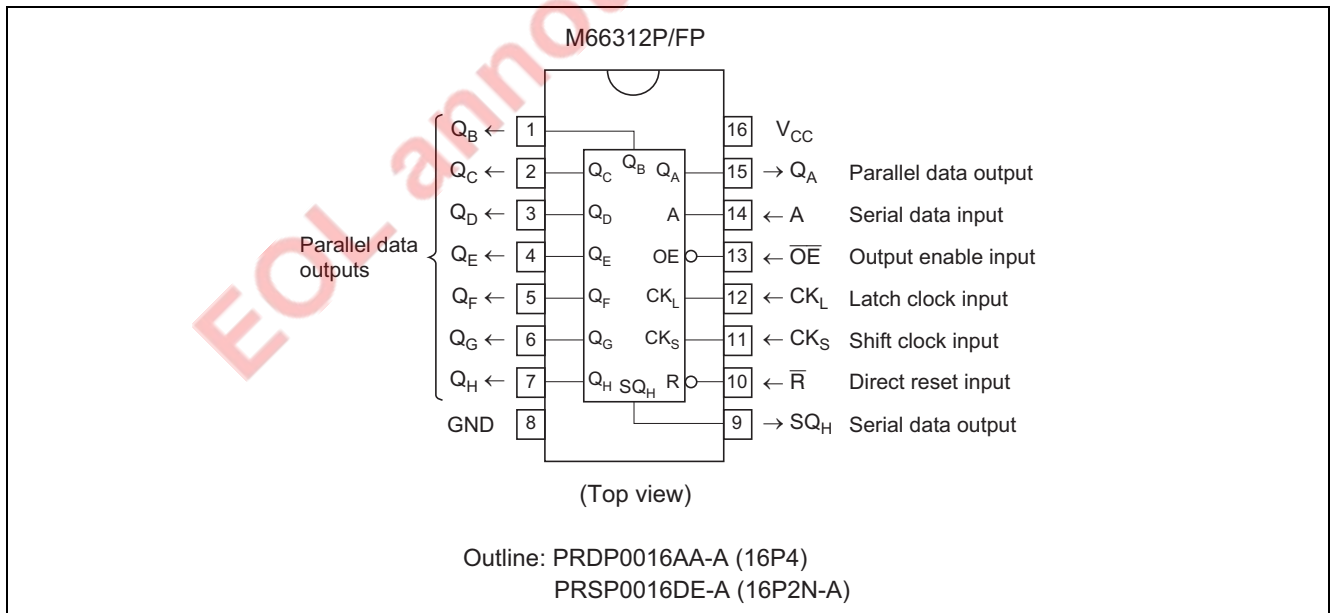
LED array drive of PRINTER

LED array drive of BUTTON TELEPHONE

## Block Diagram



## Pin Arrangement



## Functional Description

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input  $CK_S$  and latch clock input  $CK_L$  are independent from each other, shift and latch operations being made when “L” changes to “H”.

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to  $CK_S$ . When A is “H”, the signal of “H” shifts. When A is “L”, the signal of “L” shifts.

When the pulse is impressed to  $CK_L$ , the contents of the shifting register at that time are stored in a latching register, and they appear in the output from  $Q_A$  through  $Q_H$  are 3-state outputs.

To extend the number of bits, serial data output  $SQ_H$  is used to output the 8-bit of the shift register.

By connecting  $CK_S$  and  $CK_L$ , the shift register state delayed by 1 clock cycle is output at  $Q_A$  through  $Q_H$ .

When reset input  $\bar{R}$  is low, shift register and  $SQ_H$  will be reset. To reset  $Q_A$  through  $Q_H$  to low-level,  $CK_L$  must be changed from low-level to high-level after the shift register is reset by  $\bar{R}$ .

When output-enable input  $\overline{OE}$  is high,  $Q_A$  through  $Q_H$  will become high impedance state, but  $SQ_H$  is not changed.

Even if  $\overline{OE}$  is changed, shift operation is not affected.

**Function Table** (Note)

Operation Mode		Input					Parallel Data Output								Serial Data Output SQ <sub>H</sub>
		R̄	CK <sub>S</sub>	CK <sub>L</sub>	A	OĒ	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	
Reset	Shift t1	L	X	X	X	L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	Q <sub>C</sub> <sup>0</sup>	Q <sub>D</sub> <sup>0</sup>	Q <sub>E</sub> <sup>0</sup>	Q <sub>F</sub> <sup>0</sup>	Q <sub>G</sub> <sup>0</sup>	Q <sub>H</sub> <sup>0</sup>	L
	Latch t2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift latch operation	Shift t1	H	↑	X	H	L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	Q <sub>C</sub> <sup>0</sup>	Q <sub>D</sub> <sup>0</sup>	Q <sub>E</sub> <sup>0</sup>	Q <sub>F</sub> <sup>0</sup>	Q <sub>G</sub> <sup>0</sup>	Q <sub>H</sub> <sup>0</sup>	q <sub>G</sub> <sup>0</sup>
	Latch t2	H	X	↑	X	L	H	q <sub>A</sub> <sup>0</sup>	q <sub>B</sub> <sup>0</sup>	q <sub>C</sub> <sup>0</sup>	q <sub>D</sub> <sup>0</sup>	q <sub>E</sub> <sup>0</sup>	q <sub>F</sub> <sup>0</sup>	q <sub>G</sub> <sup>0</sup>	q <sub>G</sub> <sup>0</sup>
	Shift t1	H	↑	X	L	L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	Q <sub>C</sub> <sup>0</sup>	Q <sub>D</sub> <sup>0</sup>	Q <sub>E</sub> <sup>0</sup>	Q <sub>F</sub> <sup>0</sup>	Q <sub>G</sub> <sup>0</sup>	Q <sub>H</sub> <sup>0</sup>	q <sub>G</sub> <sup>0</sup>
	Latch t2	H	X	↑	X	L	L	q <sub>A</sub> <sup>0</sup>	q <sub>B</sub> <sup>0</sup>	q <sub>C</sub> <sup>0</sup>	q <sub>D</sub> <sup>0</sup>	q <sub>E</sub> <sup>0</sup>	q <sub>F</sub> <sup>0</sup>	q <sub>G</sub> <sup>0</sup>	q <sub>G</sub> <sup>0</sup>
3 state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	q <sub>H</sub>

Note  $\uparrow$ : Change from low-level to high-level  
 $Q^0$ : Output state Q before  $CK_L$  changed  
 X: Irrelevant  
 $q^0$ : Contents of shift register before  $CK_S$  changed  
 q: Contents of shift register  
 t1, t2: t2 is set after t1 is set  
 Z: High impedance

## Absolute Maximum Ratings

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	-0.5 to +7.0	V	
Input voltage	V <sub>I</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Output voltage	V <sub>O</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Input protection diode current	I <sub>IK</sub>	-20	mA	V <sub>I</sub> < 0 V
		20		V <sub>I</sub> > V <sub>CC</sub>
Output parasitic diode current	I <sub>OK</sub>	-20	mA	V <sub>O</sub> < 0 V
		20		V <sub>O</sub> > V <sub>CC</sub>
Output current per output pin	$\overline{Q}_A$ to $\overline{Q}_H$	±35	mA	
	SQ <sub>H</sub>	±25		
Supply/GND current	I <sub>CC</sub>	±132	mA	V <sub>CC</sub> , GND
Power dissipation	P <sub>d</sub>	500	mW	(Note)
Storage temperature range	T <sub>stg</sub>	-65 to +150	°C	

Note: M66312FP; Ta = -40 to +70°C, Ta = 70 to 85°C are derated at -6 mW/°C.

## Recommended Operating Conditions

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V <sub>CC</sub>	4.5	5	5.5	V
Input voltage	V <sub>I</sub>	0	—	V <sub>CC</sub>	V
Output voltage	V <sub>O</sub>	0	—	V <sub>CC</sub>	V
Operating temperature range	Topr	-40	—	+85	°C
Input rising and falling time	V <sub>CC</sub> = 4.5 V	tr, tf	0	500	ns
	V <sub>CC</sub> = 5.5 V		0	400	

## Electrical Characteristics

(V<sub>CC</sub> = 4.5 to 5.5V, unless otherwise noted)

Item	Sym bol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = −40 to +85°C				
		Min	Typ	Max	Min	Max			
High-level input voltage	V <sub>IH</sub>	0.70× V <sub>CC</sub>	—	—	0.70×V <sub>CC</sub>	—	V	V <sub>O</sub> = 0.1 V, V <sub>CC</sub> −0.1 V  I <sub>O</sub>   = 20 μA	
Low-level Input voltage	V <sub>IL</sub>	—	—	0.30×V <sub>CC</sub>	—	0.30×V <sub>CC</sub>	V	V <sub>O</sub> = 0.1 V, V <sub>CC</sub> −0.1 V  I <sub>O</sub>   = 20 μA	
High-level output voltage Q <sub>A</sub> to Q <sub>H</sub>	V <sub>OH</sub>	V <sub>CC</sub> −0.1	—	—	V <sub>CC</sub> −0.1	—	V	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −20 μA
		3.70 <sup>(note)</sup>	—	—	3.55 <sup>(note)</sup>	—		I <sub>OH</sub> = −16 mA	
High-level output voltage S <sub>Q<sub>H</sub></sub>	V <sub>OH</sub>	V <sub>CC</sub> −0.1	—	—	V <sub>CC</sub> −0.1	—	V	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −20 μA
		4.0	—	—	3.9	—		I <sub>OH</sub> = −4 mA	
Low-level output voltage Q <sub>A</sub> to Q <sub>H</sub>	V <sub>OL</sub>	—	—	0.1	—	0.1	V	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 μA
		—	—	0.7 <sup>(note)</sup>	—	0.85 <sup>(note)</sup>		I <sub>OL</sub> = 16 mA	
Low-level output voltage S <sub>Q<sub>H</sub></sub>	V <sub>OL</sub>	—	—	0.1	—	0.1	V	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 μA
		—	—	0.4	—	0.5		I <sub>OL</sub> = 4 mA	
High-level input current	I <sub>IH</sub>	—	—	0.1	—	1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , V <sub>CC</sub> = 5.5 V	
Low-level input current	I <sub>IL</sub>	—	—	−0.1	—	−1.0	μA	V <sub>I</sub> = GND, V <sub>CC</sub> = 5.5 V	
Off state high-level output current Q <sub>A</sub> to Q <sub>H</sub>	I <sub>OZH</sub>	—	—	1.0	—	10.0	μA	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> V <sub>CC</sub> = 5.5 V	V <sub>O</sub> = V <sub>CC</sub>
Off state low-level output current Q <sub>A</sub> to Q <sub>H</sub>	I <sub>OZL</sub>	—	—	−1.0	—	−10.0	μA		V <sub>O</sub> = GND
Quiescent supply current	I <sub>CC</sub>	—	—	4.0	—	40.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND, V <sub>CC</sub> = 5.5 V	

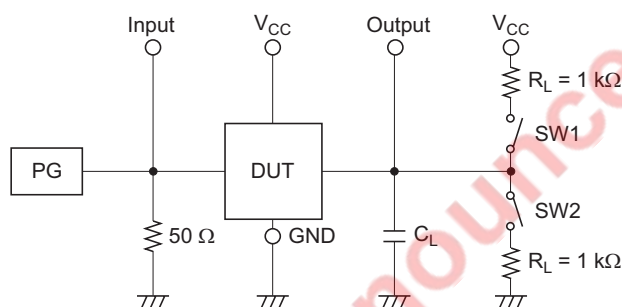
Note: Limits of single PIN operating state

## Switching Characteristics

(V<sub>CC</sub> = 5 V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = −40 to +85°C			
		Min	Typ	Max	Min	Max		
Maximum clock frequency	f <sub>max</sub>	15	—	—	12	—	MHz	C <sub>L</sub> = 50 pF
Low-level to high-level and high-level to low-level output propagation time CK <sub>S</sub> -SQ <sub>H</sub>	t <sub>PLH</sub>	—	—	70	—	88	ns	C <sub>L</sub> = 15 pF (Note)
	t <sub>PHL</sub>	—	—	70	—	88	ns	
High-level to low-level output propagation time $\bar{R}$ -SQ <sub>H</sub>	t <sub>PHL</sub>	—	—	60	—	76	ns	
Low-level to high-level and high-level to low-level output propagation time CK <sub>L</sub> -Q <sub>A</sub> to Q <sub>H</sub>	t <sub>PLH</sub>	—	—	60	—	76	ns	C <sub>L</sub> = 50 pF (Note)
	t <sub>PHL</sub>	—	—	60	—	76	ns	
Output disable time from low-level and high-level $\overline{OE}$ -Q <sub>A</sub> to Q <sub>H</sub>	t <sub>PLZ</sub>	—	—	50	—	64	ns	C <sub>L</sub> = 5 pF (Note)
	t <sub>PHZ</sub>	—	—	50	—	64	ns	
Output enable time to low-level and high-level $\overline{OE}$ -Q <sub>A</sub> to Q <sub>H</sub>	t <sub>PZL</sub>	—	—	56	—	70	ns	C <sub>L</sub> = 50 pF (Note)
	t <sub>PZH</sub>	—	—	56	—	70	ns	

Note: Test Circuit



Item	SW1	SW2
t <sub>PLH</sub> , t <sub>PHL</sub>	Open	Open
t <sub>PLZ</sub>	Close	Open
t <sub>PHZ</sub>	Open	Close
t <sub>PZL</sub>	Close	Open
t <sub>PZH</sub>	Open	Close

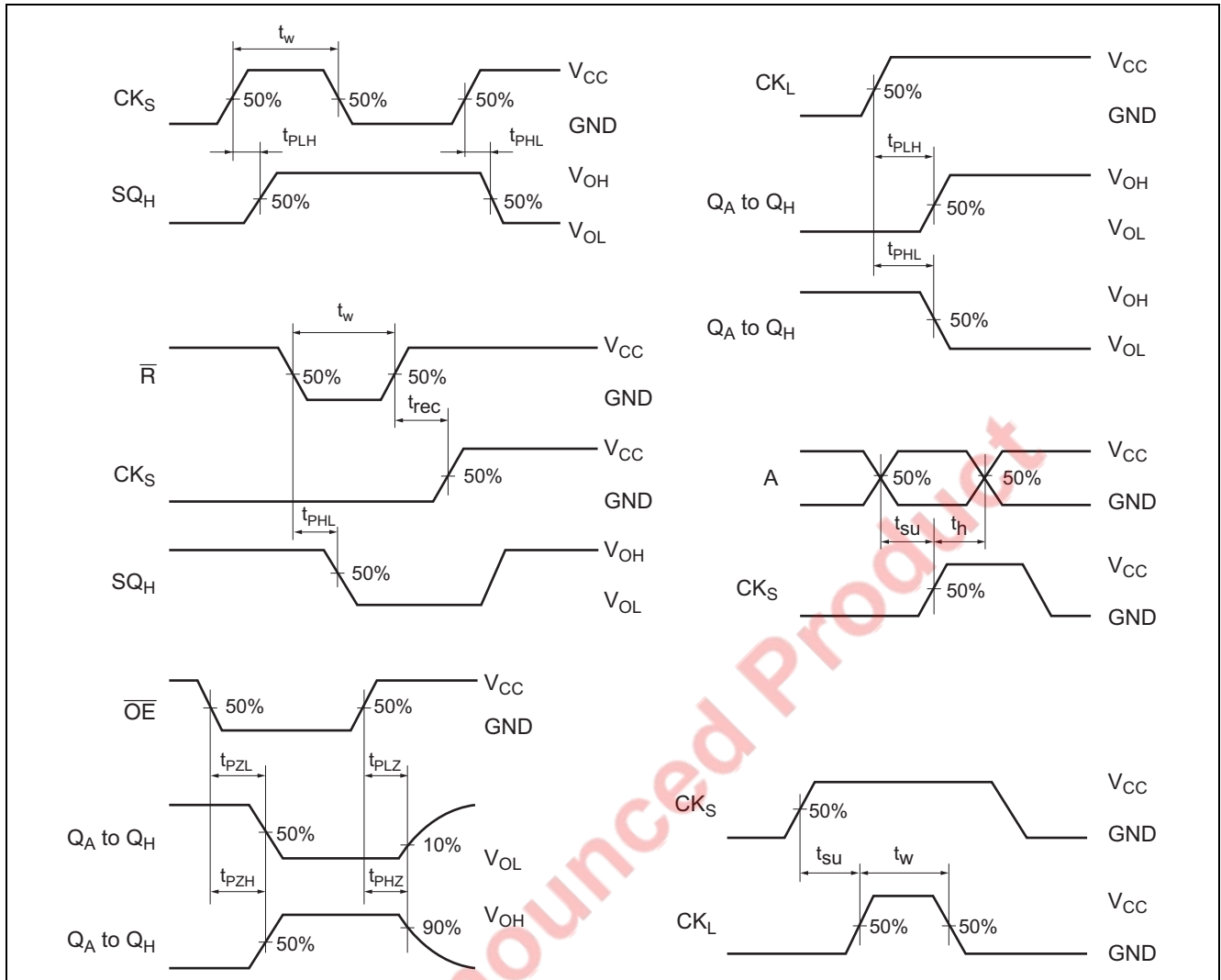
- (1) The pulse generator (PG) has the following characteristics (10% to 90%): tr = 6 ns, tf = 6 ns  
 (2) The capacitance C<sub>L</sub> includes stray wiring capacitance and the probe input capacitance.

## Timing Requirements

(V<sub>CC</sub> = 5 V)

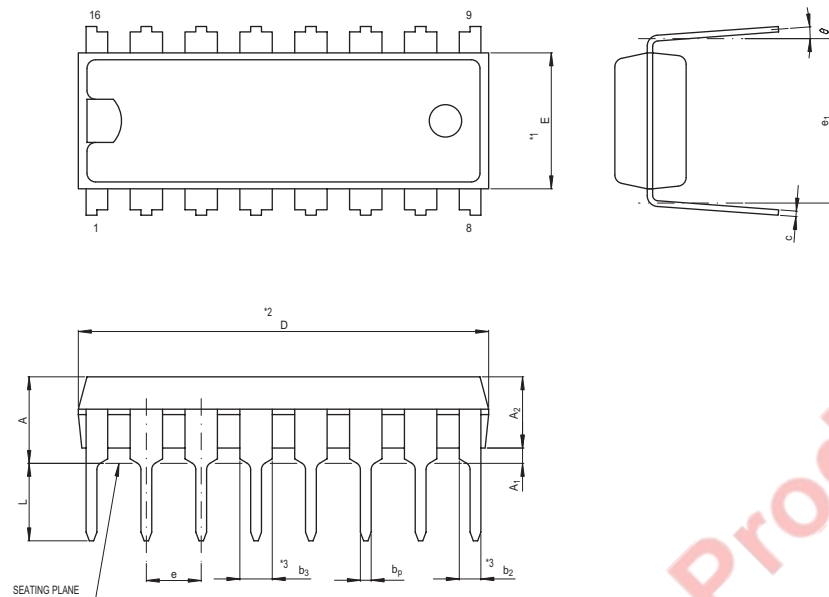
Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = −40 to +85°C			
		Min	Typ	Max	Min	Max		
CK <sub>S</sub> , CK <sub>L</sub> , $\overline{R}$ pulse width	t <sub>w</sub>	32	—	—	40	—	ns	
A setup time with respect to CK <sub>S</sub>	t <sub>su</sub>	40	—	—	50	—	ns	
CK <sub>S</sub> setup time with respect to CK <sub>L</sub>	t <sub>su</sub>	40	—	—	50	—	ns	
A hold time with respect to CK <sub>S</sub>	t <sub>h</sub>	10	—	—	10	—	ns	
$\overline{R}$ recovery time with respect to CK <sub>S</sub>	t <sub>rec</sub>	20	—	—	26	—	ns	

## Timing Chart



## Package Dimensions

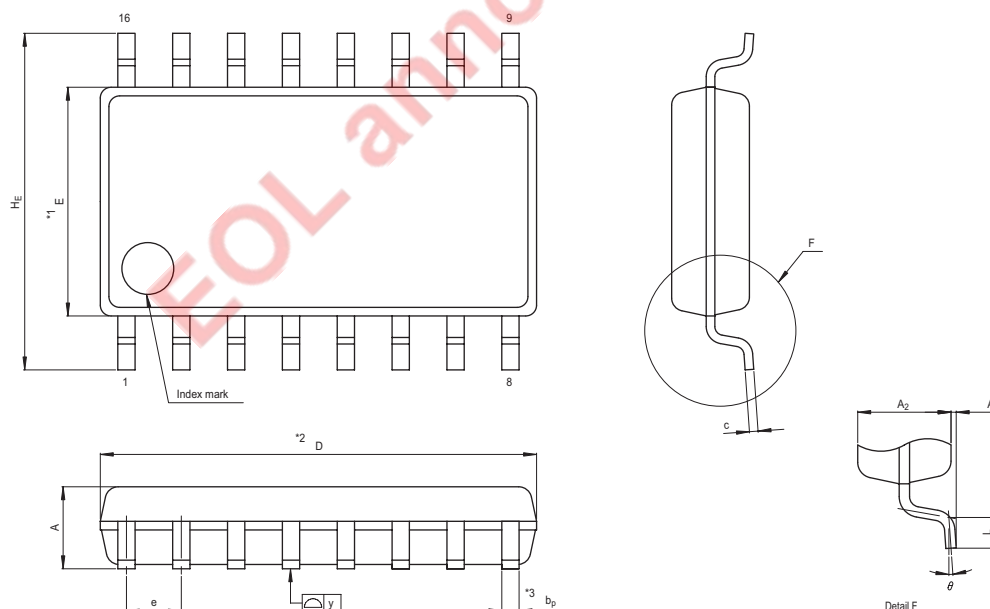
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19-2.54	PRDP0016AA-A	16P4	1.0g



NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Min	Nom	Max
e <sub>1</sub>	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A <sub>1</sub>	0.51	—	—
A <sub>2</sub>	—	3.3	—
b <sub>p</sub>	0.4	0.5	0.6
b <sub>2</sub>	0.9	1.0	1.3
b <sub>3</sub>	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.3x10.1-1.27	PRSP0016DE-A	16P2N-A	0.2g



NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A <sub>2</sub>	—	1.8	—
A <sub>1</sub>	0	0.1	0.2
A	—	—	2.1
b <sub>p</sub>	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H <sub>E</sub>	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8



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