MIC59P50

8-Bit Parallel-Input Protected Latched Driver

General Description

The MIC59P50 parallel-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, undervoltage lockout (UVLO), and overcurrent shutdown.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC59P50 has open-collector outputs capable of sinking 500mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V above V_{EE} (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC59P50 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors.

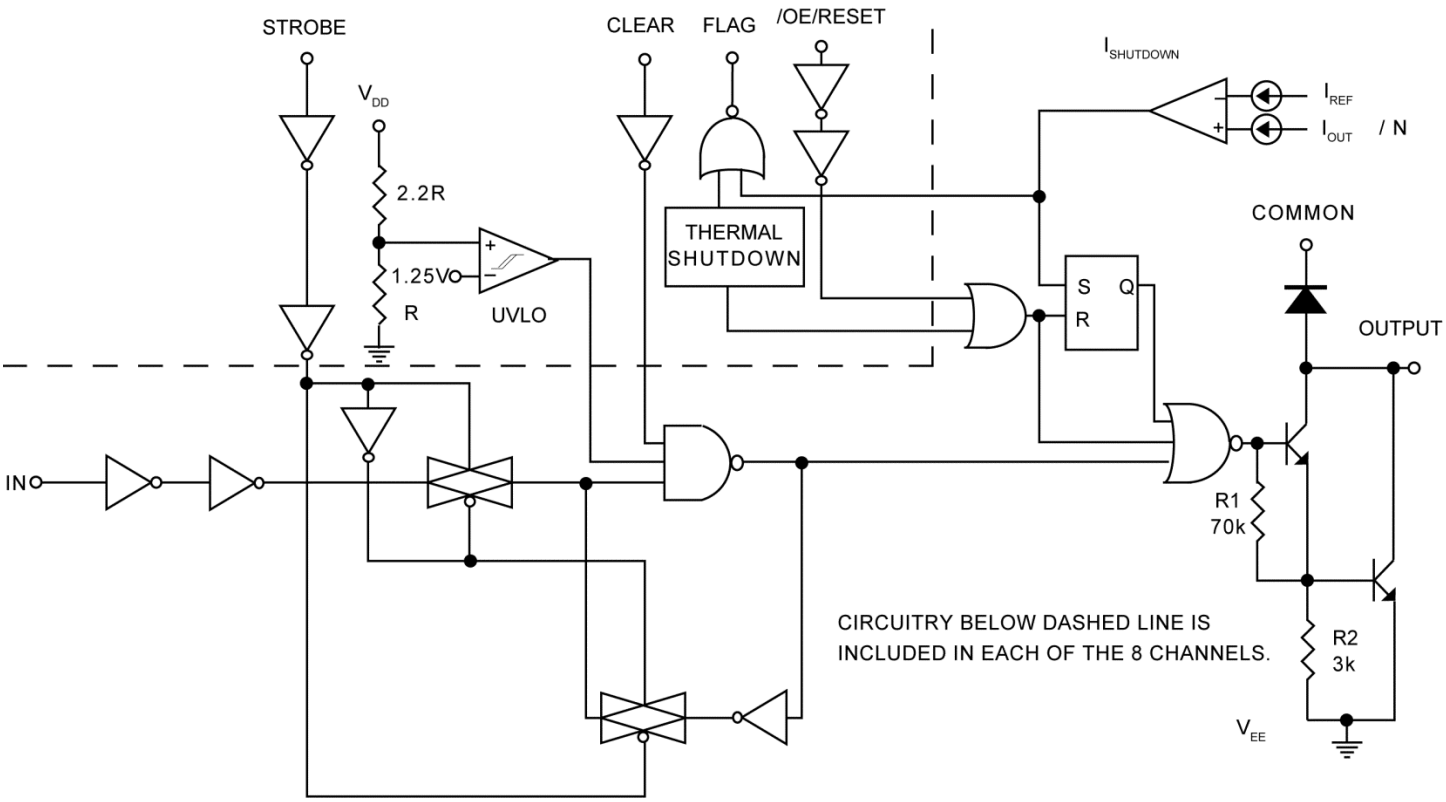
Each of these eight outputs has an independent overcurrent shutdown at 500mA. Upon current shutdown, the affected channel will turn OFF and the flag will go low until V_{DD} is cycled or the /ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate overcurrent shutdown. Temperatures above +165°C will shut down the device and activate the open-collector FLAG output at pin 1. The UVLO circuit disables the outputs at low V_{DD}; hysteresis of 0.5V is provided.

Datasheets and support documentation are available on Micrel's website at: www.micrel.com.

Features

- 4.4MHz minimum data input rate
- High-voltage, high-current outputs
- Per-output overcurrent shutdown (500mA typical)
- Undervoltage lockout
- Output fault flag
- Output transient protection diodes
- CMOS, PMOS, NMOS, and TTL-compatible inputs
- Internal pull-down resistors
- Low-power CMOS latches
- Single or split supply operation

Functional Diagram



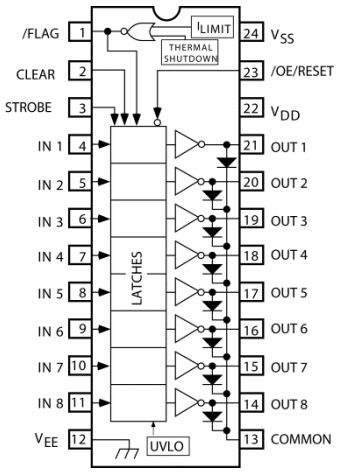
Ordering Information

Part Number	Temperature Range	Package	Pb-Free
MIC59P50YN	–40°C to +85°C	24-Pin Plastic DIP[1]	√
MIC59P50YV	–40°C to +85°C	28-Pin PLCC	√
MIC59P50YWM	–40°C to +85°C	24-Pin Wide SOIC	√

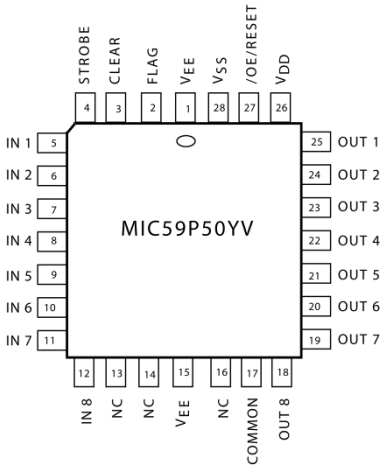
Note:

1. 300mm “Skinny DIP”

Pin Configuration



24-Pin PDIP (N)
24-Pin Wide SOIC (WM)
(Top View)



28-Pin PLCC (V)
(Top View)

Pin Description

Pin Number PDIP & SOIC	Pin Number PLCC	Pin Name	Pin Name
1	2	/FLAG	Error flag. Open-collector output is low upon overcurrent fault or overtemperature fault. /OE/RESET must be pulled high to reset the flag and fault condition.
2	3	CLEAR	Sets all latches to OFF (open).
3	4	STROBE	Input strobe pin. Loads output latches when high.
4-11	5-12	IN_n	Parallel inputs, 1 through 8.
12	15	VEE	Output ground (substrate). Most negative voltage in the system connects here.
13	17	COMMON	Transient suppression diodes cathode common pin.
14-21	18-25	OUT_n	Parallel outputs, 8 through 1.
22	26	VDD	Logic positive supply voltage.
23	27	/OE/RESET	Output enable reset. When low, outputs are active. When high, outputs are inactive and the flag and outputs are reset from a fault condition. An undervoltage condition emulates a high /OE input.
24	28	VSS	Logic reference (ground) pin.

Absolute Maximum Ratings[2]

Input Voltage (V_{CE}) ..... +80V
Supply Voltage
(V_{DD}) 15V
(V_{DD} – V_{EE}) 25V
Continuous Collector Current (I_C) 500mA
Protected Current[4] 1.5A
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature (Ts) ..... –65°C to +150°C
ESD Rating[5] ..... ESD Sensitive

Operating Ratings[3]

Input Voltage (V_{IN}) ..... –0.3V to V_{DD}+0.3V
Operating Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... +150°C
Power Dissipation (P_D)
Plastic DIP (N) 2.4W
Derate above T_A = +25°C ..... 24mW/°C
PLCC (V) 1.6W
Derate above T_A = +25°C ..... 16mW/°C
Wide SOIC (WM) 1.4W
Derate above T_A = +25°C ..... 14mW/°C

Electrical Characteristics[6]

V_{DD} = 5V; T_A = 25°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CEX}	Output Leakage Current	V_{CE} = 80V, T_A = +25°C			50	µA
		V_{CE} = 80V, T_A = +70°C			100	µA
$V_{CE(SAT)}$	Collector-Emitter	I_C = 100mA		0.9	1.1	V
	Saturation Voltage	I_C = 200mA		1.1	1.3	V
		I_C = 350mA		1.3	1.6	V
$V_{IN(0)}$	Input Voltage				1.0	V
$V_{IN(1)}$		V_{DD} = 12V	10.5			V
		V_{DD} = 10V	8.5			V
		V_{DD} = 5V, Note 7	3.5			V
R_{IN}	Input Resistance	V_{DD} = 12V	50	200		kΩ
		V_{DD} = 10V	50	300		kΩ
		V_{DD} = 5V	50	600		kΩ
I_{OL}	/Flag Output Current	V_{OL} = 0.4V		15		mA
I_{OH}	/Flag Output Leakage	V_{OH} = 12V		50		nA

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.
4. Each channel VEE connection must be designed to minimize inductance and resistance.
5. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
6. Specification for packaged product only.
7. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic “1”.

Electrical Characteristics[6] (Continued)

V_{DD} = 5V; T_A = 25°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DD(ON)1}$	Supply Current One Output Active	V_{DD} = 12V, outputs open		3.3	4.5	mA
		V_{DD} = 10V, outputs open		3.1	4.5	mA
		V_{DD} = 5V, outputs open		2.4	3.6	mA
$I_{DD(ON)\ All}$	Supply Current All Outputs Active	V_{DD} = 12V, outputs open		6.4	10.0	mA
		V_{DD} = 10V, outputs open		6.0	9.0	mA
		V_{DD} = 5V, outputs open		4.7	7.5	mA
$I_{DD(OFF)}$	Supply Current OFF	V_{DD} = 12V, outputs open, inputs = 0V		3.0	4.5	mA
		V_{DD} = 5V, outputs open, inputs = 0V		2.2	3.6	mA
I_R	Clamp Diode Leakage Current	V_R = 80V, T_A = +25°C			50	µA
		V_R = 80V, T_A = +70°C			100	µA
I_{LIM}	Overcurrent Threshold	Each output		500		mA
V_{SU}	Start-up Voltage	Note 8	3.5	4.0	4.5	V
$V_{DD\ MIN}$	Minimum Operating V_{DD}		3.0	3.5	4.0	V
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2.0	V
	Thermal Shutdown			165		°C
	Thermal Shutdown Hysteresis			10		

Notes:

8. Undervoltage lockout is guaranteed to release device at no more than 4.5V and disable the device at no less than 3.0V input logic voltage.

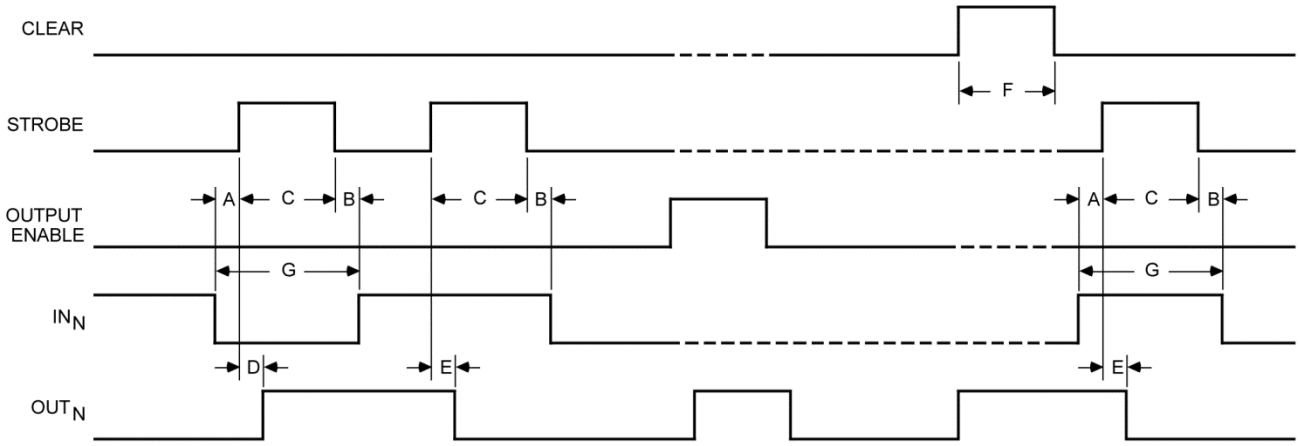
Truth Table

IN_n	Strobe	Clear	Output Enable	OUT_n	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

Note:
X = Irrelevant
t-1 = Previous output state
t = Present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation and reset the FLAG. Overtemperature faults are not latched and require no reset pulse.

Timing Diagram



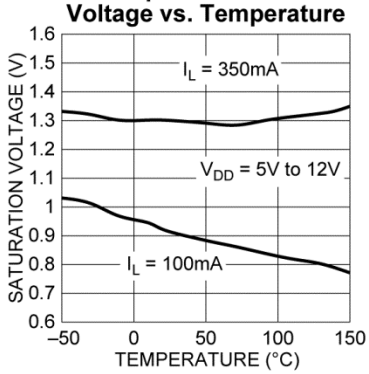
Timing Conditions

T_A = +25°C; Logic levels are V_{DD} and V_{SS}; V_{DD} = 5V.

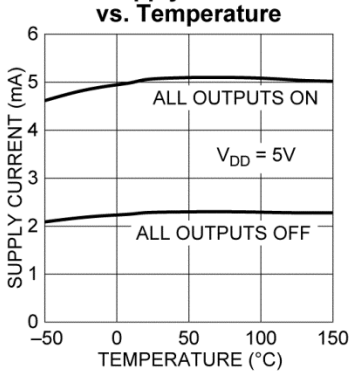
A.	Minimum data active time before strobe enabled (data set-up time)	50ns
B.	Minimum data active time after strobe disabled (data hold time)	50ns
C.	Minimum strobe pulse width	125ns
D.	Typical time between strobe activation and output on-to-off transition	500ns
E.	Typical time between strobe activation and output off-to-on transition	500ns
F.	Minimum clear pulse width	300ns
G.	Minimum data pulse width	225ns

Typical Characteristics

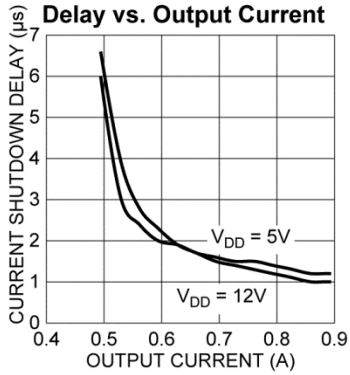
Output Saturation Voltage vs. Temperature



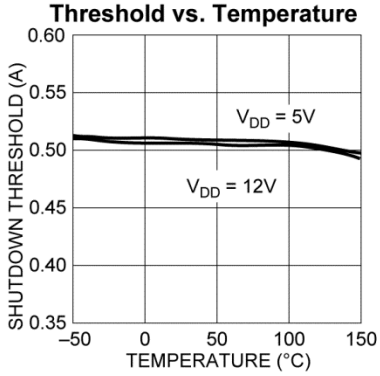
Supply Current vs. Temperature



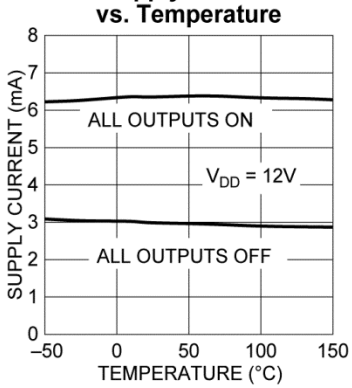
Current Shutdown Delay vs. Output Current



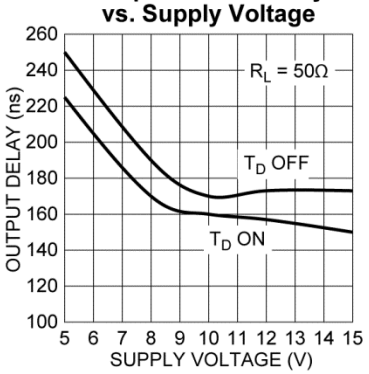
Current Shutdown Threshold vs. Temperature



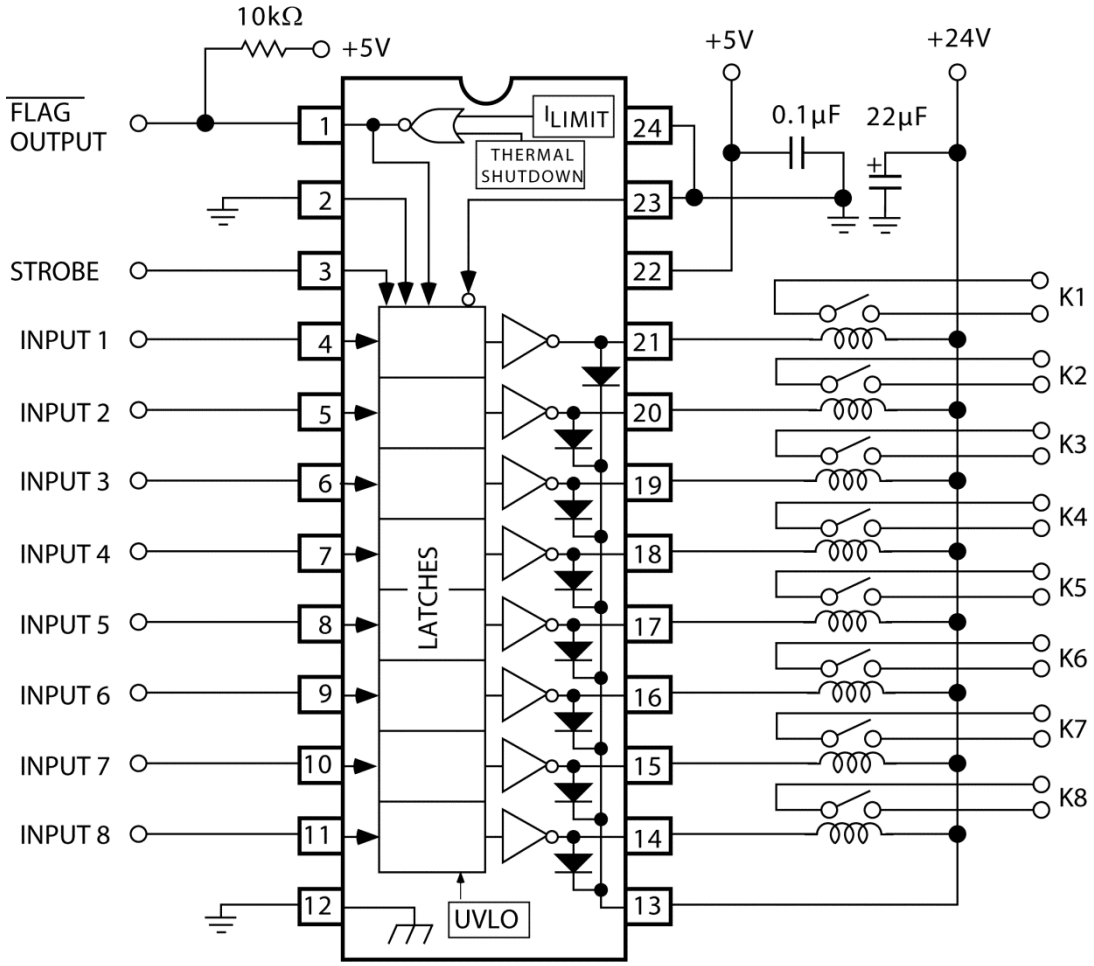
Supply Current vs. Temperature



Output Enable Delay vs. Supply Voltage

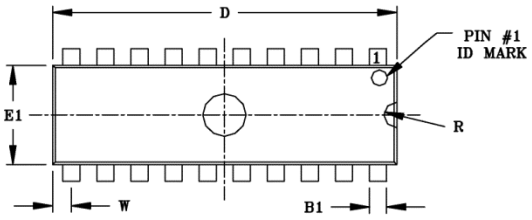


Typical Application

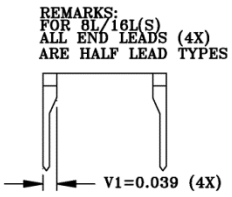


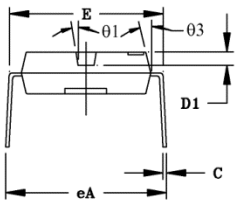
MIC59P50 Protected Relay Driver

Package Information and Recommended Land Pattern[9]

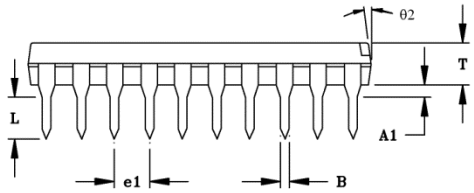


TOP VIEW





END VIEW



SIDE VIEW

NOTE:

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF TIN PLATING OR SOLDER PLATING/ DIPPING THICKNESS.
2. PACKAGE OUTLINE EXCLUSIVE OF ANY MOLD FLASHES.
3. PACKAGE OUTLINE EXCLUSIVE OF BURR DIMENSION.
4. * – REFERENCE DIMENSION.
5. PACKAGE AND FINISHING : TOP, BOTTOM & ALL SIDE: MATTE VDI #24~27.

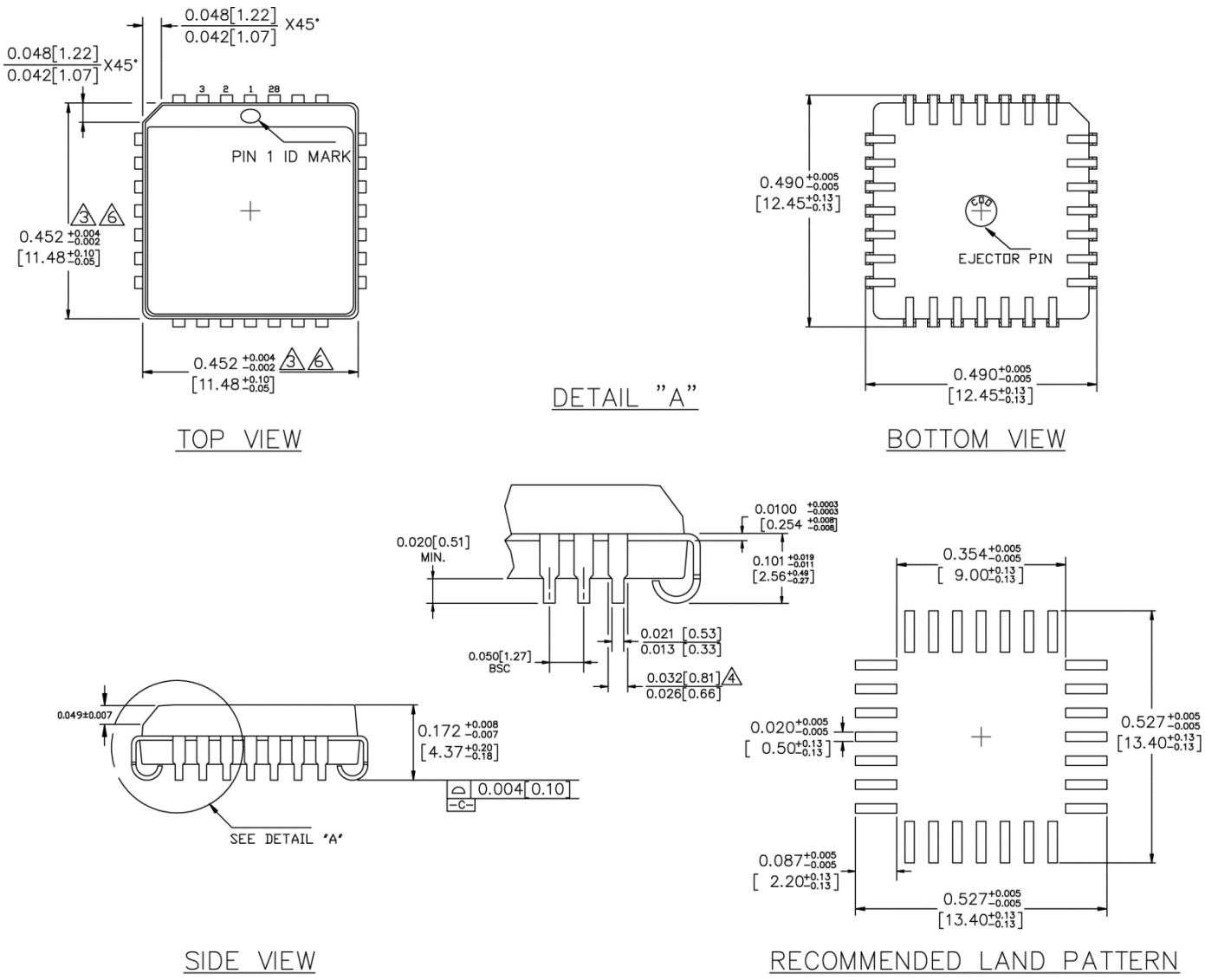
LEAD TYPE		8LD	14/16LD	18LD	20LD	24LD
STAND-OFF	A1	0.015 MIN	0.015 MIN	0.015 MIN	0.015 MIN	0.015 MIN
LEAD WIDTH *	B	0.018	0.018	0.018	0.018	0.018
SPADE WIDTH *	B1	0.060	0.060	0.060	0.060	0.060
LEAD THICKNESS *	C	0.010	0.010	0.010	0.010	0.012
LENGTH TOL ±0.004	D	0.375	0.750	0.890	1.020	1.250
IDENT DEPTH	D1	0.030 ~ 0.060	0.030 ~ 0.060	0.030 ~ 0.060	0.030 ~ 0.060	0.030 ~ 0.060
SHOULDER WIDTH OUTER TO OUTER	E	0.300 ~ 0.325	0.300 ~ 0.325	0.300 ~ 0.325	0.300 ~ 0.325	0.300 ~ 0.325
WIDTH TOL ±0.004	E1	0.250	0.250	0.250	0.250	0.250
LEAD SPREAD OUTER TO OUTER	eA	0.320 ~ 0.370	0.320 ~ 0.370	0.320 ~ 0.370	0.320 ~ 0.370	0.320 ~ 0.370
LEAD PITCH *	e1	0.100	0.100	0.100	0.100	0.100
LEAD LENGTH TOL ±0.004	L	0.125	0.125	0.125	0.125	0.125
IDENT RADIUS	R	0.030	0.030	0.030	0.030	0.030
TOTAL THICKNESS TOL ±0.004	T	0.130	0.130	0.130	0.130	0.130
LEAD TO END PACKAGE	W	0.025 REF	0.075REF14LD 0.025REF16LD	0.045REF	0.060REF	0.075REF
IDENT DRAFT TOL ±3°	θ1	7°	7°	7°	7°	7°
END ANGLE (4x) TOL ±3°	θ2	7°	7°	7°	7°	7°
SIDE ANGLE (4x) TOL ±3°	θ3	7°	7°	7°	7°	7°

24-Pin PDIP (N)

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

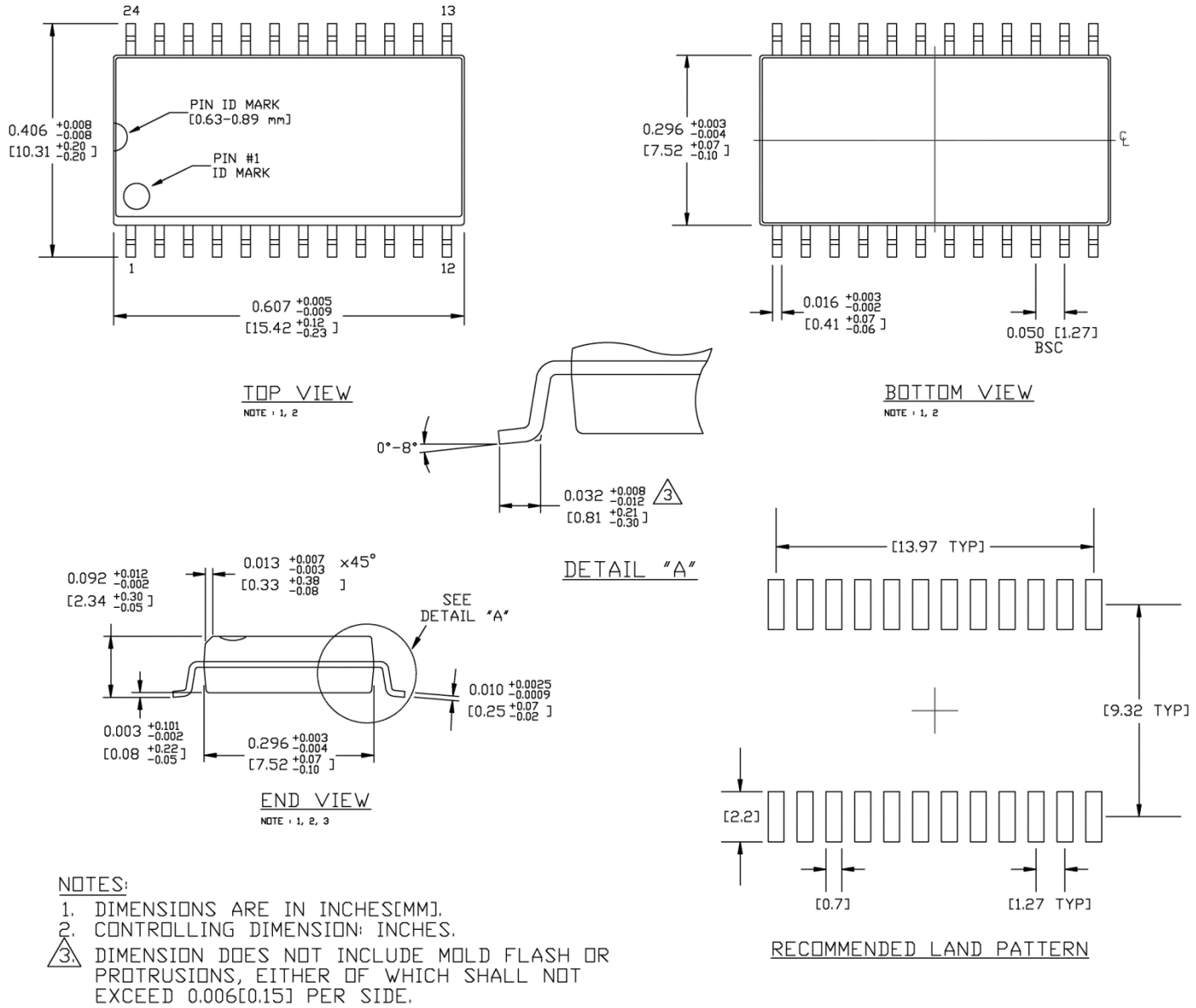
Package Information and Recommended Land Pattern[9]



NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS : MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

28-Pin PLCC (V)

Package Information and Recommended Land Pattern[9]



24-Pin Wide SOIC (WM)

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