ISL6185

Dual USB Port Power Supply Controller

FN6937
Rev 3.00
March 8, 2012

The ISL6185 USB power controller family provides fully independent overcurrent (OC) fault protection for two or more USB ports.

This product family consists of sixteen individual functional product variants and three package options. It is operation rated for a nominal +2.5V to +5V range and is specified over the full commercial and industrial temperature ranges.

Each ISL6185 type incorporates in a single package two 71mΩ P-channel MOSFET power switches for power control. Each features internal current monitoring, accurate current limiting, and current limited delay to turn-off, for system supply protection along with control and communication I/O.

The ISL6185 family offers product variants with specified continuous output current levels of 0.6A, 1.1A, 1.5A or 1.8A; enable active high or low inputs; and latch off or automatic retry after overcurrent turn-off, making these devices well suited for many low-power applications.

This family of ICs is offered in an industry-standard SOIC pinout and also in the 70% smaller 3x3 DFN packages providing similar or enhanced performance in the smallest possible package.

Features

- 2.5V to 5V Operating Range
- 71mΩ Integrated Power P-channel MOSFET Switches
- Continuous Current Options for 0.6A, 1.1A, 1.5A and 1.8A
- Thermally Insensitive 12ms of Current Limiting Prior to Turn-Off
- Output Discharges with Reverse Current Blocking When Disabled
- Latch-off or Auto Restart Options
- 1µA Off-State Supply Current
- Enable Polarity Options
- Industry-standard Pin for Pin SOIC, and Smaller DFN Packages Available
- UL Recognized, File Number: E333469

Applications

- USB 1, 2, 3 Port Power Management
- Low Power (18W) Electronic Circuit Limiting and Breaker

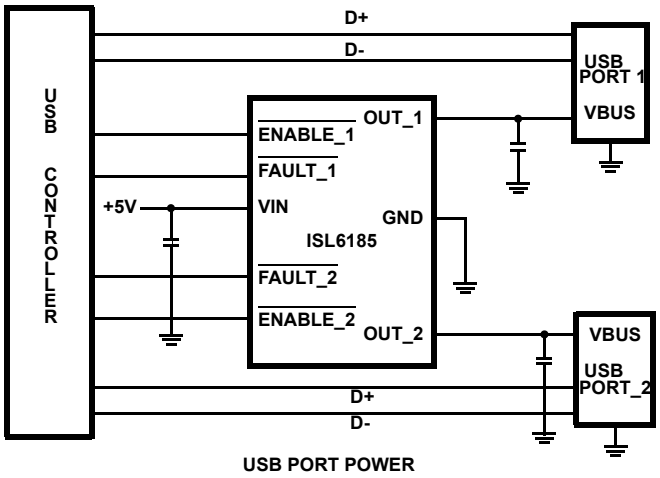


FIGURE 1. TYPICAL APPLICATION

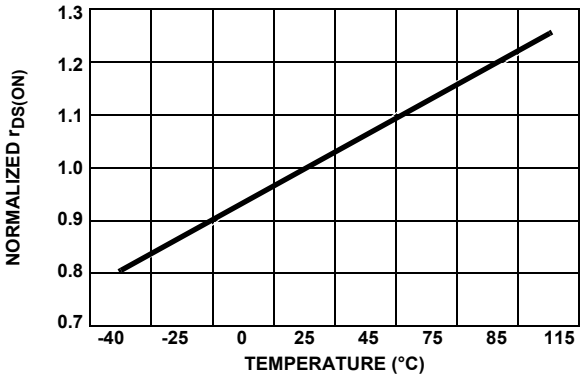
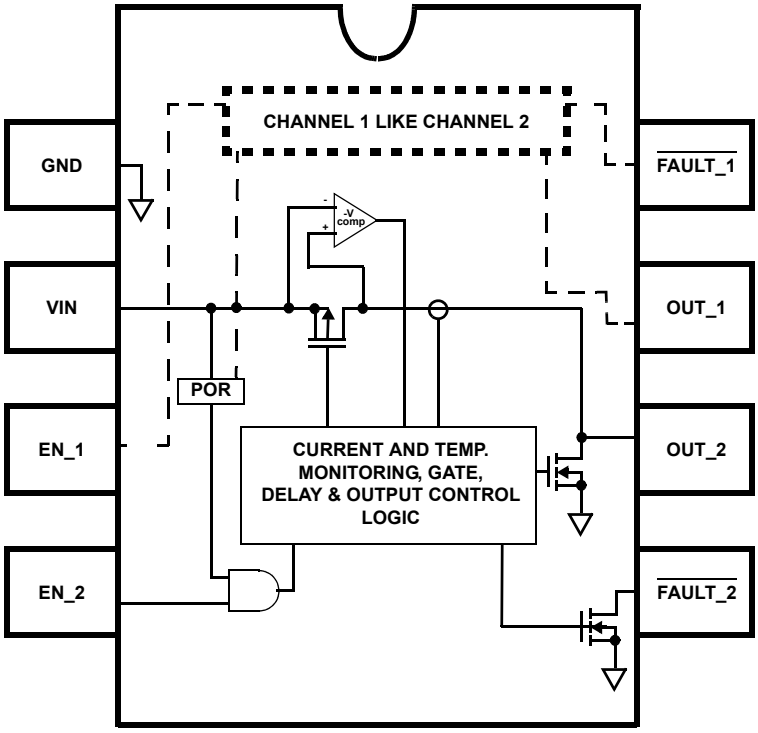


FIGURE 2. NORMALIZED $r_{DS(ON)}$ TEMPERATURE CHARACTERISTIC CURVE

Simplified Block Diagram



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	EN/$\overline{EN}$ INPUT	V_{IN} = 5V MAXIMUM CONTINUOUS IOUT (A)	LATCH/AUTO RETRY	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL61851ACBZ	61851A CBZ	EN	0.6	LATCH	0 to +70	8 Lead SOIC	M8.15
ISL61851BCBZ	61851B CBZ	EN	0.6	RETRY	0 to +70	8 Lead SOIC	M8.15
ISL61851CCBZ	61851C CBZ	EN	1.1	LATCH	0 to +70	8 Lead SOIC	M8.15
ISL61851DCBZ	61851D CBZ	EN	1.1	RETRY	0 to +70	8 Lead SOIC	M8.15
ISL61851ECBZ	61851E CBZ	$\overline{EN}$	0.6	LATCH	0 to +70	8 Lead SOIC	M8.15
ISL61851FCBZ	61851F CBZ	$\overline{EN}$	0.6	RETRY	0 to +70	8 Lead SOIC	M8.15
ISL61851GCBZ	61851G CBZ	$\overline{EN}$	1.1	LATCH	0 to +70	8 Lead SOIC	M8.15
ISL61851HCBZ	61851H CBZ	$\overline{EN}$	1.1	RETRY	0 to +70	8 Lead SOIC	M8.15
ISL61851ICBZ	61851I CBZ	EN	1.5	LATCH	0 to +70	8 Lead SOIC	M8.15
ISL61851JCBZ	61851J CBZ	EN	1.5	RETRY	0 to +70	8 Lead SOIC	M8.15
ISL61851KCBZ	61851K CBZ	$\overline{EN}$	1.5	LATCH	0 to +70	8 Lead SOIC	M8.15
ISL61851LCBZ	61851L CBZ	$\overline{EN}$	1.5	RETRY	0 to +70	8 Lead SOIC	M8.15
ISL61852ACRZ	52AC	EN	0.6	LATCH	0 to +70	8 Lead DFN	L8.3x3J
ISL61852BCRZ	52BC	EN	0.6	RETRY	0 to +70	8 Lead DFN	L8.3x3J
ISL61852CCRZ	52CC	EN	1.1	LATCH	0 to +70	8 Lead DFN	L8.3x3J
ISL61852DCRZ	52DC	EN	1.1	RETRY	0 to +70	8 Lead DFN	L8.3x3J
ISL61852ECRZ	52EC	$\overline{EN}$	0.6	LATCH	0 to +70	8 Lead DFN	L8.3x3J

Ordering Information (Continued)

PART NUMBER (Notes 1, 2, 3)	PART MARKING	EN/$\overline{EN}$ INPUT	V_{IN} = 5V MAXIMUM CONTINUOUS IOUT (A)	LATCH/AUTO RETRY	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL61852FCRZ	52FC	$\overline{EN}$	0.6	RETRY	0 to +70	8 Lead DFN	L8.3x3J
ISL61852GCRZ	52GC	$\overline{EN}$	1.1	LATCH	0 to +70	8 Lead DFN	L8.3x3J
ISL61852HCRZ	52HC	$\overline{EN}$	1.1	RETRY	0 to +70	8 Lead DFN	L8.3x3J
ISL61852ICRZ	52IC	EN	1.5	LATCH	0 to +70	8 Lead DFN	L8.3x3J
ISL61852JCRZ	52JC	EN	1.5	RETRY	0 to +70	8 Lead DFN	L8.3x3J
ISL61852KCRZ	52KC	$\overline{EN}$	1.5	LATCH	0 to +70	8 Lead DFN	L8.3x3J
ISL61852LCRZ	52LC	$\overline{EN}$	1.5	RETRY	0 to +70	8 Lead DFN	L8.3x3J
ISL61853ACRZ	53AC	EN	0.6	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853BCRZ	53BC	EN	0.6	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853CCRZ	53CC	EN	1.1	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853DCRZ	53DC	EN	1.1	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853ECRZ	53EC	$\overline{EN}$	0.6	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853FCRZ	53FC	$\overline{EN}$	0.6	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853GCRZ	53GC	$\overline{EN}$	1.1	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853HCRZ	53HC	$\overline{EN}$	1.1	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853ICRZ	53IC	EN	1.5	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853JCRZ	53JC	EN	1.5	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853KCRZ	53KC	$\overline{EN}$	1.5	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853LCRZ	53LC	$\overline{EN}$	1.5	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853MCRZ	53MC	EN	1.8	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853NCRZ	53NC	EN	1.8	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61853OCRZ	53OC	$\overline{EN}$	1.8	LATCH	0 to +70	10 Lead DFN	L10.3x3
ISL61853PCRZ	53PC	$\overline{EN}$	1.8	RETRY	0 to +70	10 Lead DFN	L10.3x3
ISL61851AIBZ	61851A IBZ	EN	0.6	LATCH	-40 to +85	8 Lead SOIC	M8.15
ISL61851BIBZ	61851B IBZ	EN	0.6	RETRY	-40 to +85	8 Lead SOIC	M8.15
ISL61851CIBZ	61851C IBZ	EN	1.1	LATCH	-40 to +85	8 Lead SOIC	M8.15
ISL61851DIBZ	61851D IBZ	EN	1.1	RETRY	-40 to +85	8 Lead SOIC	M8.15
ISL61851EIBZ	61851E IBZ	$\overline{EN}$	0.6	LATCH	-40 to +85	8 Lead SOIC	M8.15
ISL61851FIBZ	61851F IBZ	$\overline{EN}$	0.6	RETRY	-40 to +85	8 Lead SOIC	M8.15
ISL61851GIBZ	61851G IBZ	$\overline{EN}$	1.1	LATCH	-40 to +85	8 Lead SOIC	M8.15
ISL61851HIBZ	61851H IBZ	$\overline{EN}$	1.1	RETRY	-40 to +85	8 Lead SOIC	M8.15
ISL61851IIBZ	61851I IBZ	EN	1.5	LATCH	-40 to +85	8 Lead SOIC	M8.15
ISL61851JIBZ	61851J IBZ	EN	1.5	RETRY	-40 to +85	8 Lead SOIC	M8.15
ISL61851KIBZ	61851K IBZ	$\overline{EN}$	1.5	LATCH	-40 to +85	8 Lead SOIC	M8.15
ISL61851LIBZ	61851L IBZ	$\overline{EN}$	1.5	RETRY	-40 to +85	8 Lead SOIC	M8.15
ISL61852AIRZ	52AI	EN	0.6	LATCH	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852BIRZ	52BI	EN	0.6	RETRY	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852CIRZ	52CI	EN	1.1	LATCH	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852DIRZ	52DI	EN	1.1	RETRY	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852EIRZ	52EI	$\overline{EN}$	0.6	LATCH	-40 to +85	8 Lead DFN	L8.3x3J

Ordering Information (Continued)

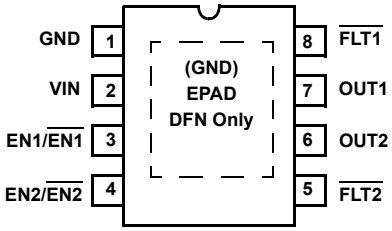
PART NUMBER (Notes 1, 2, 3)	PART MARKING	EN/$\overline{EN}$ INPUT	V_{IN} = 5V MAXIMUM CONTINUOUS IOUT (A)	LATCH/AUTO RETRY	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL61852FIRZ	52FI	$\overline{EN}$	0.6	RETRY	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852GIRZ	52GI	$\overline{EN}$	1.1	LATCH	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852HIRZ	52HI	$\overline{EN}$	1.1	RETRY	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852IIRZ	52II	EN	1.5	LATCH	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852JIRZ	52JI	EN	1.5	RETRY	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852KIRZ	52KI	$\overline{EN}$	1.5	LATCH	-40 to +85	8 Lead DFN	L8.3x3J
ISL61852LIRZ	52LI	$\overline{EN}$	1.5	RETRY	-40 to +85	8 Lead DFN	L8.3x3J
ISL61853AIRZ	53AI	EN	0.6	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853BIRZ	53BI	EN	0.6	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853CIRZ	53CI	EN	1.1	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853DIRZ	53DI	EN	1.1	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853EIRZ	53EI	$\overline{EN}$	0.6	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853FIRZ	53FI	$\overline{EN}$	0.6	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853GIRZ	53GI	$\overline{EN}$	1.1	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853HIRZ	53HI	$\overline{EN}$	1.1	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853IIRZ	53II	EN	1.5	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853JIRZ	53JI	EN	1.5	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853KIRZ	53KI	$\overline{EN}$	1.5	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853LIRZ	53LI	$\overline{EN}$	1.5	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853MIRZ	53MI	EN	1.8	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853NIRZ	53NI	EN	1.8	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61853OIRZ	53OI	$\overline{EN}$	1.8	LATCH	-40 to +85	10 Lead DFN	L10.3x3
ISL61853PIRZ	53PI	$\overline{EN}$	1.8	RETRY	-40 to +85	10 Lead DFN	L10.3x3
ISL61851EVAL1Z	8 Lead SOIC Evaluation Platform with ISL61851A installed						
ISL61852EVAL1Z	8 Lead DFN Evaluation Platform with ISL61852H installed						
ISL61853EVAL1Z	10 Lead DFN Evaluation Platform with ISL61853I installed						

NOTES:

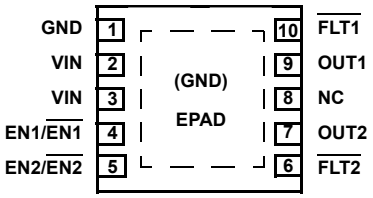
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information pages for ISL6185XXC (commercial version) and ISL6185XXI (industrial version). For more information on MSL please see techbrief TB363.

Pin Configurations

ISL6185
(8 LD SOIC/DFN)
TOP VIEW



ISL6185
(10 LD DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER		SYMBOL	DESCRIPTION
8 Ld SOIC/DFN	10 Ld DFN		
1	1	GND	IC ground reference.
2	2, 3	VIN	Chip bias, Controlled Voltage Input, Undervoltage Lock Out (UVLO). VIN provides chip bias voltage. At VIN < 1.7V chip functionality is disabled, $\overline{FLT}$ is active and floating, and OUT is held low. Range 0V to 5.5V.
3, 4	4, 5	EN1, $\overline{EN1}$/ EN2, $\overline{EN2}$	Enable/Disable inputs, Active high (EN) and active low ($\overline{EN}$) options enable the power switch. These inputs have internal 1MΩ pull-off resistors. Range 0V to VIN.
5, 8	6, 10	$\overline{FLT2}$ $\overline{FLT1}$	Overcurrent Fault Indicator. $\overline{FLT}$ floats and is disabled until VIN >V_{UVLO}. This output is pulled low after the current limit time-out period has expired. Fault is not signaled due to over-temperature shut down. Range 0V to VIN.
6, 7	7, 9	OUT2, OUT1	Controlled Supply Output. Upon an OC condition, I_{OUT} is current limited. Current limit response time is within 200µs. This output remains in current limit for a nominal 12ms before being turned off either for the latch or auto retry versions. Range 0V to VIN.
-	8	NC	This pin is not electrically connected internally.
PD (DFN only)	PD	EPAD	Thermal Dissipation Exposed PAD Range: Connect to GND.

Absolute Maximum Ratings

Supply Voltage (VIN to GND, Note 7) 6.5V
EN, FAULT. . . . . VIN
OUT. . . . . GND - 0.3V to VIN 0.3V
Output Current . . . . . Short Circuit Protected Current Limit of 2.5A
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). 3kV
Machine Model (Per MIL-STD-883 Method 3015.7) 300V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead SOIC Package (Note 4)	120	N/A
8 Lead 3x3 DFN Package (Notes 5, 6)	48	6
10 Lead 3x3 DFN Package (Notes 5, 6)	53	6

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Commercial Temperature Range . . . . . 0°C to +70°C
Industrial Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range (Typical). . . . . 2.3V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{IN} = 5V, T_A = T_J, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER SWITCH						
$r_{DS(ON)_50}$	ON-Resistance at 5.0V (Pulse Tested)	V_{IN} = 5V, I_{OUT} = 0.1A, T_A = T_J = +25°C	-	71	87	mΩ
		T_A = T_J = +85°C	-		**110**	mΩ
$r_{DS(ON)_33}$	ON-Resistance at 3.3V (Pulse Tested)	V_{IN} = 3.3V, I_{OUT} = 0.1A, T_A = T_J = +25°C	-	90	105	mΩ
		T_A = T_J = +85°C	-		**130**	mΩ
$r_{DS(ON)_25}$	On Resistance at 2.5V (Pulse Tested)	V_{IN} = 2.5V, I_{OUT} = 0.1A, T_A = T_J = +25°C	-	114	127	mΩ
		T_A = T_J = +85°C	-		**150**	mΩ
V_{OUT_DIS}	Disabled Output Voltage	V_{IN} = 5V, Switch Disabled, 50µA Load	-	50	**70**	mV
R_{OUT_PU}	Output Pull-Down Resistor	V_{IN} = 5V, Switch Disabled	**8**	9.6	**12**	kΩ
t_R	V_{OUT} Rise Time	R_L = 10Ω, C_L = 10µF, 10% to 90%	-	100	-	µs
t_F	Slow V_{OUT} Turn-off Fall Time	R_L = 10Ω, C_L = 10µF, 90% to 10%	-	200	-	µs
t_{F_fast}	Fast V_{OUT} Turn-off Fall Time	R_L = 1Ω, C_L = 10µF, 80% to 20%	-	23	-	µs
CURRENT CONTROL						
$I_{OUT_CONT_5}$	Maximum Continuous Current, V_{IN} = 5V. Guaranteed by Itrip minimum specification.	ISL6185xA,B,E,F	-		**0.6**	A
$I_{OUT_CONT_5}$		ISL6185xC,D,G,H	-		**1.1**	A
$I_{OUT_CONT_5}$		ISL6185xI,J,K,L	-		**1.5**	A
$I_{OUT_CONT_5}$		ISL61853M,N,O,P (10 Ld DFN)	-		**1.8**	A
$I_{OUT_CONT_3}$	Maximum Continuous Current, V_{IN} = 3.3V. Guaranteed by Itrip minimum specification.	ISL6185xA,B,E,F	-		**0.6**	A
$I_{OUT_CONT_3}$		ISL6185xC,D,G,H	-		**0.9**	A
$I_{OUT_CONT_3}$		ISL61851I,J,K,L (SOIC)	-		**1.3**	A
$I_{OUT_CONT_3}$		ISL61852, ISL61853 (DFN)	-		**1.5**	A

Electrical Specifications V_{IN} = 5V, T_A = T_J, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
$I_{OUT_CONT_2}$	Maximum Continuous Current, V_{IN} = 2.5V	ISL6185xA,B,E,F	-	0.6	-	A
$I_{OUT_CONT_2}$		ISL61851C,D,G,H,I,J,K,L (SOIC)	-	0.9	-	A
$I_{OUT_CONT_2}$		ISL61852, ISL61853 C,D,G,H (DFN)	-	1	-	A
$I_{OUT_CONT_2}$		ISL61853I,J,K,L (10 Ld DFN)	-	1	-	A
$I_{OUT_CONT_2}$		ISL61853M,N,O,P (10 Ld DFN)	-	1	-	A
I_{TRIP_5}	Trip Current, V_{IN} = 5V	ISL6185xA,B,E,F	**0.70**	1.02	**1.52**	A
I_{TRIP_5}		ISL6185xC,D,G,H	**1.15**	1.45	**1.95**	A
I_{TRIP_5}		ISL6185xI,J,K,L	**1.55**	1.82	**2.25**	A
I_{TRIP_5}		ISL61853M.N,O,P	**1.85**	1.99	**2.45**	A
I_{TRIP_3}	Trip Current, V_{IN} = 3.3V	ISL6185xA,B,E,F	**0.65**	0.86	**1.20**	A
I_{TRIP_3}		ISL6185xC,D,G,H	**0.95**	1.25	**1.60**	A
I_{TRIP_3}		ISL6185xI,J,K,L	**1.35**	1.60	**1.85**	A
I_{TRIP_3}		ISL61853M.N,O,P	**1.55**	1.89	**2.25**	A
I_{TRIP_2}	Trip Current, V_{IN} = 2.5V	ISL6185xA,B,E,F	**-**	0.65	-	A
I_{TRIP_2}		ISL6185xC,D,G,H	**-**	1	-	A
I_{TRIP_2}		ISL6185xI,J,K,L	**-**	1.2	-	A
I_{TRIP_2}		ISL61853M.N,O,P	**-**	1.6	**-**	A
I_{LIM_5}	Current Limit, V_{IN} = 5V	ISL6185xA,B,E,F, V_{IN} - V_{OUT} = 1V	**0.50**	0.65	**0.78**	A
I_{LIM_5}		ISL6185xC,D,G,H, V_{IN} - V_{OUT} = 1V	**0.98**	1.14	**1.28**	A
I_{LIM_5}		ISL6185xI,J,K,L, V_{IN} - V_{OUT} = 1V	**1.30**	1.55	**1.72**	A
I_{LIM_5}		ISL61853M,N,O,P, V_{IN} - V_{OUT} = 1V	**1.52**	1.83	**2.20**	A
I_{LIM_3}	Current Limit, V_{IN} = 3.3V	ISL6185xA,B,E,F, V_{IN} - V_{OUT} = 1V	**0.45**	0.63	**0.75**	A
I_{LIM_3}		ISL6185xC,D,G,H, V_{IN} - V_{OUT} = 1V	**0.90**	1.10	**1.26**	A
I_{LIM_3}		ISL6185xI,J,K,L, V_{IN} - V_{OUT} = 1V	**1.25**	1.50	**1.68**	A
I_{LIM_3}		ISL61853M,N,O,P, V_{IN} - V_{OUT} = 1V	**1.48**	1.78	**2.05**	A
I_{LIM_2}	Current Limit, V_{IN} = 2.5V	ISL6185xA,B,E,F, V_{IN} - V_{OUT} = 1V	**0.47**	0.61	**0.74**	A
I_{LIM_2}		ISL6185xC,D,G,H, V_{IN} - V_{OUT} = 1V	**0.90**	1.05	**1.17**	A
I_{LIM_2}		ISL6185xI,J,K,L, V_{IN} - V_{OUT} = 1V	**1.15**	1.37	**1.58**	A
I_{LIM_2}		ISL61853M,N,O,P, V_{IN} - V_{OUT} = 1V	**1.3**	1.63	**1.90**	A
I_{sc_5}	Short Circuit Current, V_{IN} = 5V	ISL6185xA,B,E,F, V_{OUT} = 0V	**0.60**	0.80	**1.00**	A
I_{sc_5}		ISL6185xC,D,G,H, V_{OUT} = 0V	**1.00**	1.27	**1.55**	A
I_{sc_5}		ISL6185xI,J,K,L, V_{OUT} = 0V	**1.15**	1.61	**1.85**	A
I_{sc_5}		ISL61853M,N,O,P, V_{OUT} = 0V	**1.20**	1.70	**2.5**	A
I_{sc_3}	Short Circuit Current, V_{IN} = 3.3V	ISL6185XA,B,E,F, V_{OUT} = 0V	**0.35**	0.48	**0.60**	A
I_{sc_3}		ISL6185XC,D,G,H, V_{OUT} = 0V	**0.65**	0.80	**0.95**	A
I_{sc_3}		ISL6185xI,J,K,L, V_{OUT} = 0V	**0.70**	1.06	**1.25**	A
I_{sc_3}		ISL61853M,N,O,P, V_{OUT} = 0V	**0.90**	1.24	**1.50**	A

Electrical Specifications V_{IN} = 5V, T_A = T_J, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
I_{sc_2}	Short Circuit Current, V_{IN} = 2.5V	ISL6185xA,B,E,F, V_{OUT} = 0V	-	0.61		A
I_{sc_2}		ISL6185xC,D,G,H, V_{OUT} = 0V	-	1.06	-	A
I_{sc_2}		ISL6185xI,J,K,L, V_{OUT} = 0V	-	1.30	-	A
I_{sc_2}		ISL61853M,N,O,P, V_{OUT} = 0V	-	1.39	-	A
$I_{sc_5.5}$	Short Circuit Current, V_{IN} = 5.5V	All ISL6185X Variants	-	-	2.5	A
$tsett_{Ilim}$	OC to Limit Settling Time	$V_{IN}/R_L = 2I_{LIM}$, C_L = 10µF to within 10% of I_{LIM}	-	200	-	µs
$tsett_{Ilim_sev}$	Severe OC to Limit Settling Time	$V_{IN}/R_L = 4I_{LIM}$, C_L = 10µF to within 10% of I_{LIM}	-	30	-	µs
t_{CL}	Current Limit Duration	$I_{OUT} = I_{LIM}$	9.2	12	15	ms
t_{RTY}	Automatic Retry Period		0.80	1	1.35	s
I/O PARAMETERS						
Vfault_lo	Fault Output Voltage	Fault I_{OUT} = 10mA	-	-	0.4	V
Ifault	Fault Leakage		-	5	-	µA
Venr_5	EN / $\overline{EN}$ Rising Threshold	V_{IN} = 5V	1.5	1.8	2	V
Hys_Venr_5	EN / $\overline{EN}$ Rising Threshold Hysteresis	V_{IN} = 5V	80	140	175	mV
Venr_3	EN / $\overline{EN}$ Rising Threshold	V_{IN} = 3.3V	1.0	1.3	1.6	V
Hys_Venr_3	EN / $\overline{EN}$ Rising Threshold Hysteresis	V_{IN} = 3.3V	58	80	120	mV
Venr_2	EN / $\overline{EN}$ Rising Threshold	V_{IN} = 2.5V	0.95	1.1	1.3	V
Hys_Venr_2	EN / $\overline{EN}$ Rising Threshold Hysteresis	V_{IN} = 2.5V	30	70	110	mV
Ren_h	ENABLE Pull-Down Resistor	Enable asserted high options	0.6	1	1.55	MΩ
Ren_l	$\overline{ENABLE}$ Pull-Up Resistor	Enable asserted low options	0.6	1	1.55	MΩ
t_{ON}	Enable to Output Turn-on Time	R_L = 10Ω, C_L = 10µF, Enable 50% to Output 90%	-	0.1	-	ms
t_{OFF}	Enable to Output Turn-off Time	R_L = 10Ω, C_L = 10µF, Enable 50% to Output 10%	-	0.25	-	ms
BIAS PARAMETERS						
I_{VDD}	Enabled V_{IN} Current	Switches Closed, OUTPUT = OPEN		50	75	µA
I_{VDD}	Disabled V_{IN} Current	Switches Open, OUTPUT = OPEN	-	2	5	µA
V_{UVLO}	Rising POR Threshold	V_{IN} Rising to functional operation	1.7	2.1	2.3	V
I_{VR}	Reverse Blocking Leakage Current	V_{IN} = 0V, V_{OUT} = 5V	-		2	µA
Temp_dis	Over-Temperature Disable		-	150	-	°C
Temp_hys	Over-Temperature Hysteresis		-	20	-	°C

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Introduction

The ISL6185 is a dual channel fully independent overcurrent (OC) fault protection IC for the +2.5V to +5V environment. Each ISL6185 incorporates in a single package two 85mΩ P-channel MOSFET power switches for power control. Independent enabling inputs and fault reporting outputs compatible with 2.5V to 5V logic allow for external control and reporting. This device features integrated power switches with current monitoring, accurate current limiting, reverse bias protection and current limited timed delay to turn-off for system reliability. See Figures 13 through 28 for typical operational waveforms including both under-current and over-current situations.

The ISL6185 offers current sense and limiting, with V_{IN} = 5V guaranteed continuous current product variants of 0.6A, 1.1A, 1.5A and 1.8A, making these devices well suited for a myriad of USB and other low power (9W max) port power management applications and configurations.

The ISL6185 also provides thermally insensitive timed OC turn-off and fault notification. This isolates and protects the voltage bus in the event of a peripheral OC event or short circuit event, independent of the adjoining switch's electrical or the ambient thermal condition.

The ISL6185 undervoltage lockout feature prevents turn-on of the outputs unless the correct ENABLE state and $V_{IN} > V_{UVLO}$ are present. During initial turn-on, the ISL6185 prevents fault reporting by blanking the fault signal.

During operation, once an OC condition is detected, the output is current limited for t_{CL} to allow transient OC conditions to pass. If still in current limit after the current limit period has elapsed, the output is turned off, and the fault is reported by pulling the corresponding $\overline{FAULT}$ output low. On the latch-off options, after turn-off, both the output and the $\overline{FAULT}$ signal are latched low until reset by the enable signal being de-asserted or until a POR occurs. At this time, the $\overline{FAULT}$ signal clears, and the switch is ready to be turned back on. On the auto restart options, the ISL6185 attempts to periodically turn on the output, as long as the enable is asserted.

When disabled, the ISL6185 has a low quiescent supply current and an output-to-input reverse current flow blocking capability.

The ISL6185 family is provided with enable polarity options and an industry-standard 8 lead SOIC pinout, along with two versions in the 70% smaller 3x3 DFN. The 8 Ld DFN package offers the same performance as the 8 Ld SOIC, whereas the 10 Ld DFN offers higher current capability in the smallest possible package because of lower package electrical and thermal resistance.

Functional Description

Power On Preset (POR)

The ISL6185 POR feature inhibits device functionality when VIN < V_{UVLO}.

Reverse Polarity Protection

In any event in which the power switch is disabled and $V_{OUT} > V_{IN,}$ there will be no output-to-input current flow, nor will the output voltage appear on the input.

Soft-Start

Upon enable, the switch passes a constant current to the load. The voltage on the VOUT pin ramps up according the equation, I_{LIM}/C_{OUT} (V/s). Resistive or active load slows the V_{OUT} ramp-up toward the top of its curve.

Fault Blanking On Start-Up

During initial turn-on, the ISL6185 prevents nuisance faults from being reported to the system controller by blanking the fault signal until the internal FET is fully enhanced.

Current Trip and Limiting Levels

The ISL6185 provides integrated current sensing in the MOSFET that allows for rapid control of OC events. Once an OC condition is detected, the ISL6185 goes into its current limiting (CL) control mode. The ISL6185 is variant specified to allow a continuous current (I_{CONT}) operation of 0.6A, 1.1A, 1.5A or 1.8A. As the current increases past its continuous current rating, it will reach a level that causes the device to enter its current limit mode; that is, the current trip level. The current trip level is in all cases adequately above the I_{CONT} rating so as not to cause unintended false faults. The current limit is specified at $V_{OUT} = V_{IN}$ - 1V to test a known representative condition and is featured at a nominal value slightly higher than the continuous current rating. The speed of this current limiting control is inversely related to the magnitude of the OC fault. Thus, a hard overcurrent is more quickly pulled to its limiting value than a marginal OC condition.

Over-Temperature Shutdown

Although the ISL6185 has an over-temperature shutdown and lockout feature, because of the 12ms timed shutdown, the thermal shutdown is likely to be invoked only in extremely high ambient temperatures.

The over-temperature protection invokes and disables the switch turn-on operation once the die temperature is ~+140°C. It turns off an already on switch at ~+150°C and releases the part to operation once the die temperature falls to ~+120°C.

Turn-off Time Delay

During operation, once an OC condition is detected, the output is current limited for ~12ms to allow transient OC conditions to pass. If still in current limit and after the current limit period has elapsed, the output is turned off, and the fault is reported by pulling the corresponding $\overline{\text{FAULT}}$ low. The internal 12ms timer starts upon current limiting and is independent of ambient or IC thermal conditions, thus providing more consistent operation over the entire temperature range.

Latch-off Restart/Auto-Restart Start

After turn-off, with the latch-off options, both the output and the $\overline{\text{FAULT}}$ signal are latched low until they are reset by the enable signal being de-asserted. At this time, the $\overline{\text{FAULT}}$ signal clears, and the IC is ready for enable to assert. On the auto restart options, the ISL6185 attempts to periodically turn-on the output at approximately 1s intervals, as long as the enable is asserted. If the OC condition remains indefinitely, the fault indication and the restart attempts also continue until the thermal protection feature is invoked, thus increasing the restart period.

Active Output Pull-down

Another ISL6185 feature is the 10kΩ active pull-down on the outputs to <60mV above GND when the device is disabled, thus ensuring discharge of the load.

Typical Performance Curves

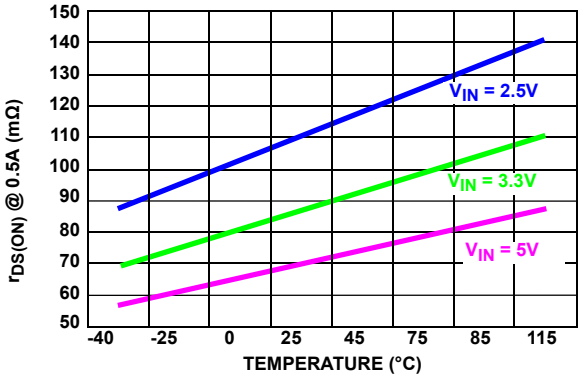


FIGURE 3. SWITCH ON-RESISTANCE AT 0.5A

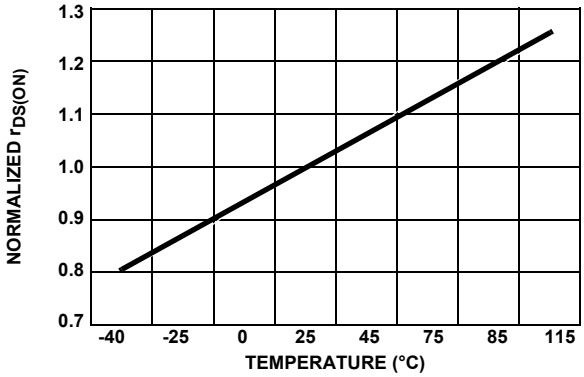


FIGURE 4. NORMALIZED SWITCH RESISTANCE

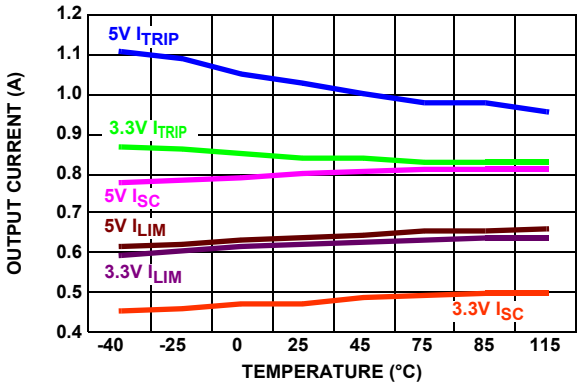


FIGURE 5. 0.6A CONTINUOUS CURRENT CHARACTERISTICS

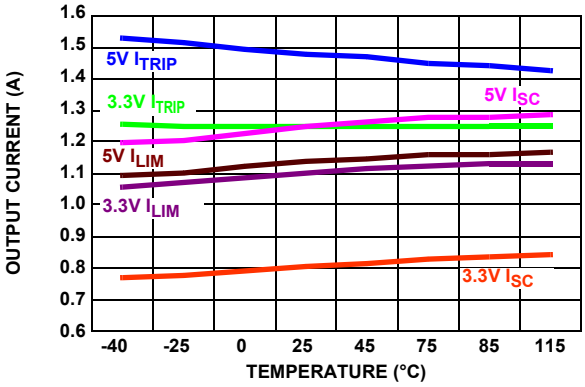


FIGURE 6. 1.1A CONTINUOUS CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

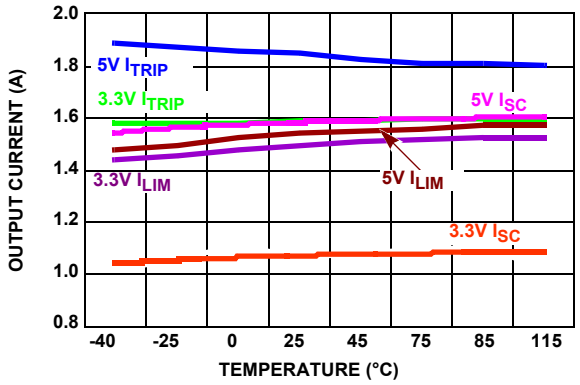


FIGURE 7. 1.5A CONTINUOUS CURRENT CHARACTERISTICS

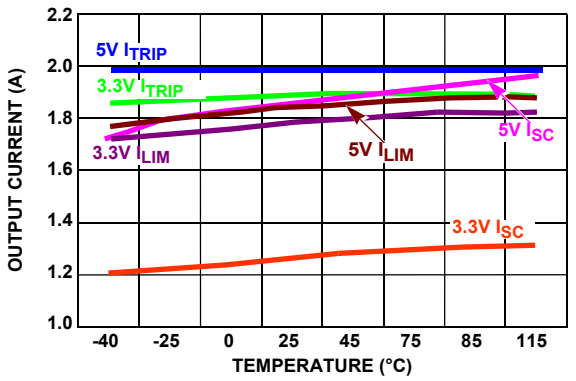


FIGURE 8. 1.8A CONTINUOUS CURRENT CHARACTERISTICS

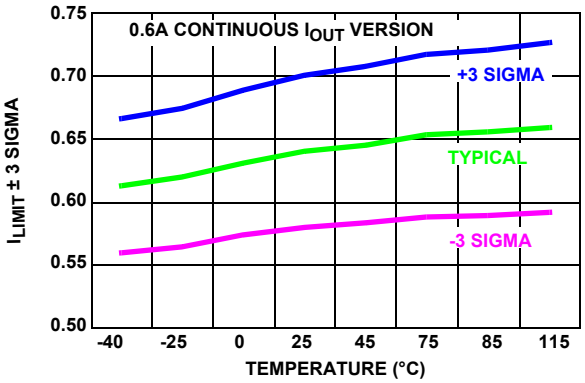


FIGURE 9. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V

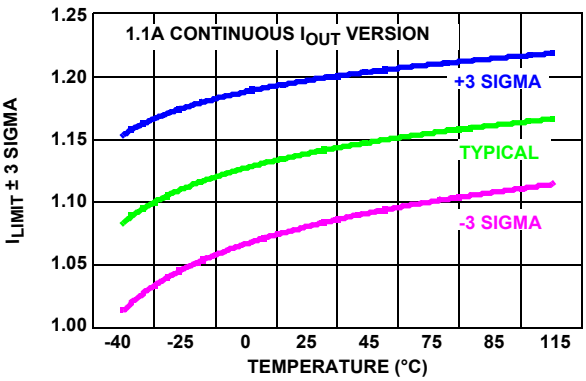


FIGURE 10. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V

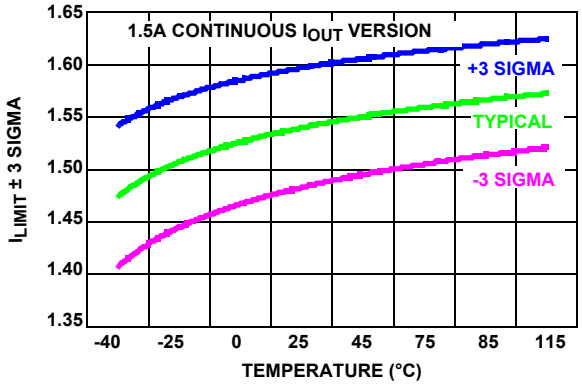


FIGURE 11. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V

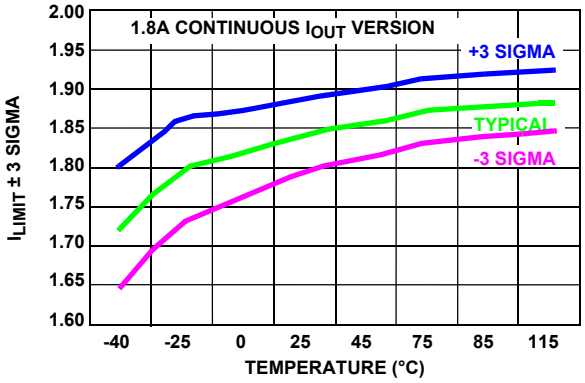


FIGURE 12. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V

Typical Performance Curves (Continued)

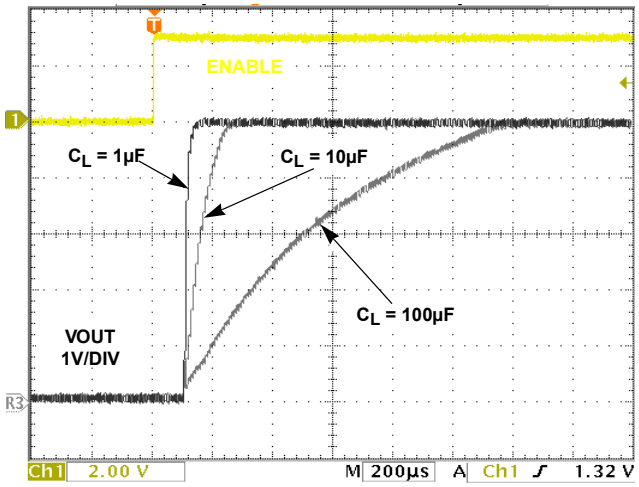


FIGURE 13. V_{OUT} TURN-ON/RISE TIME vs C_{LOAD}. V_{IN} = 5V, R_L = 10Ω

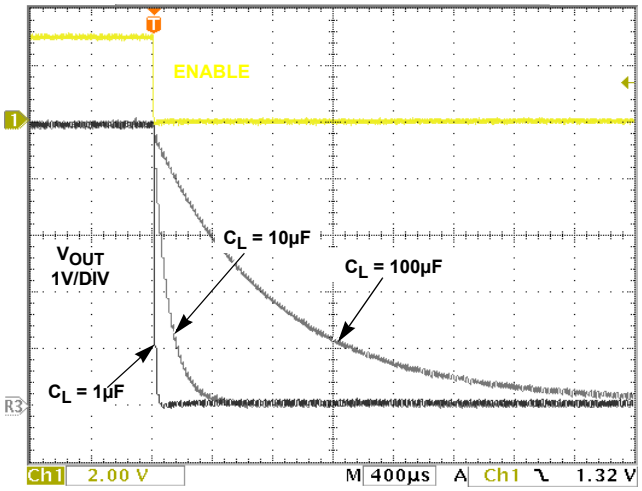


FIGURE 14. V_{OUT} TURN-OFF/FALL TIME vs C_{LOAD}. V_{IN} = 5V, R_L = 10Ω

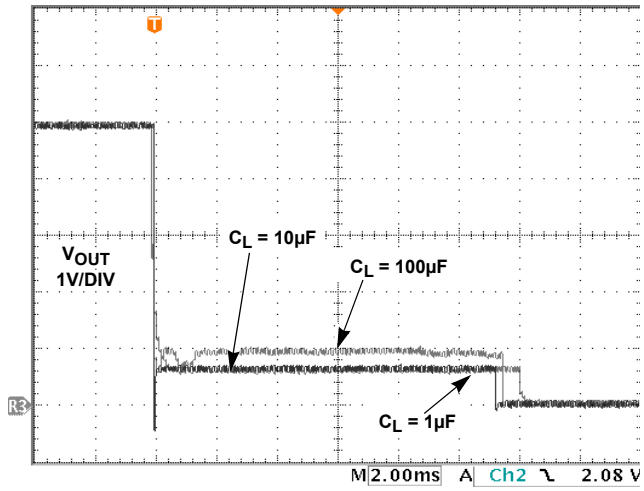


FIGURE 15. LATCH-OFF vs C_{LOAD}

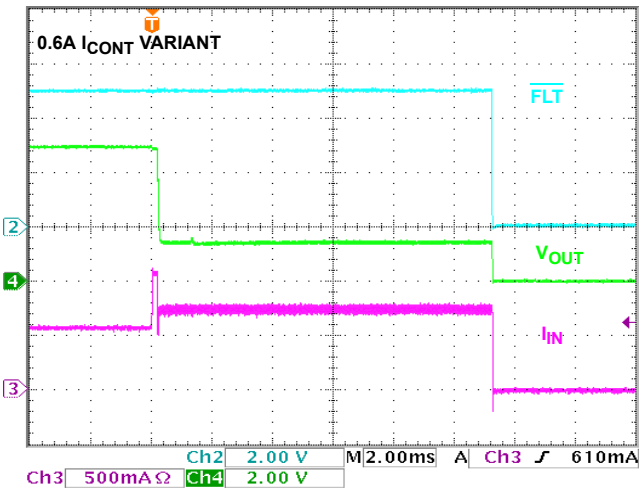


FIGURE 16. I_{LIM} WAVEFORM

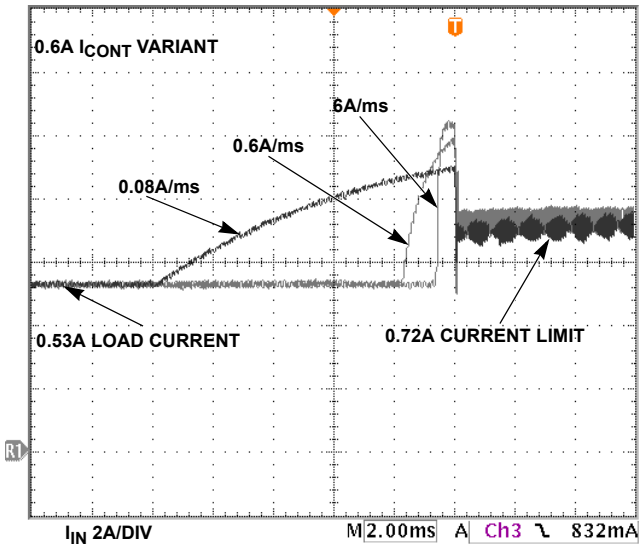


FIGURE 17. OC RAMP RATE I_{LIM} WAVEFORMS

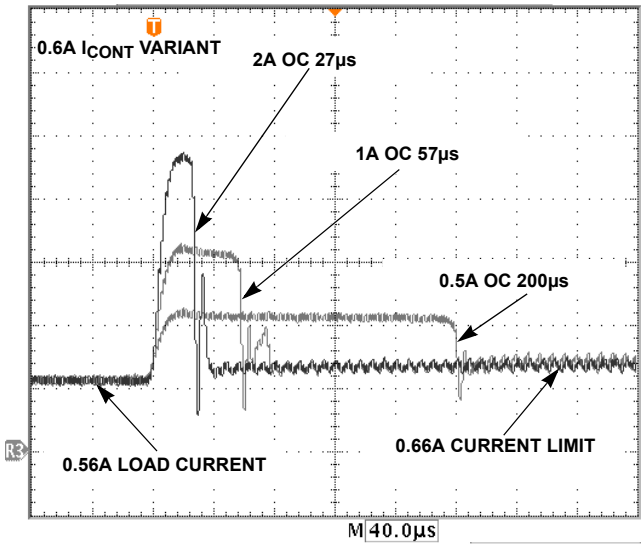


FIGURE 18. PEAK CURRENT SETTLING TIMES

Typical Performance Curves (Continued)

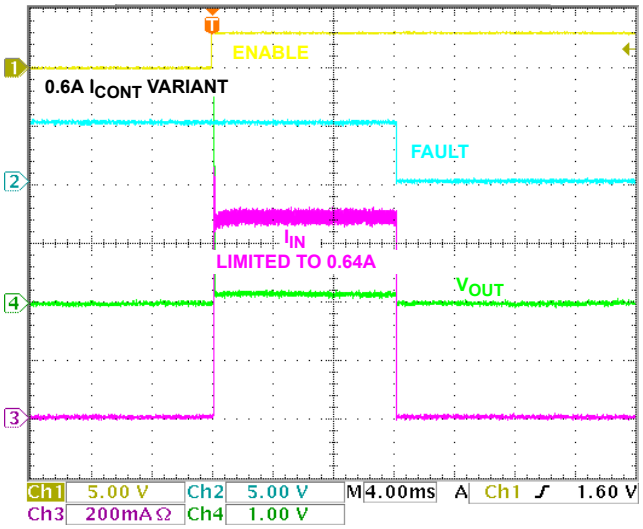


FIGURE 19. TURN-ON INTO A SHORT

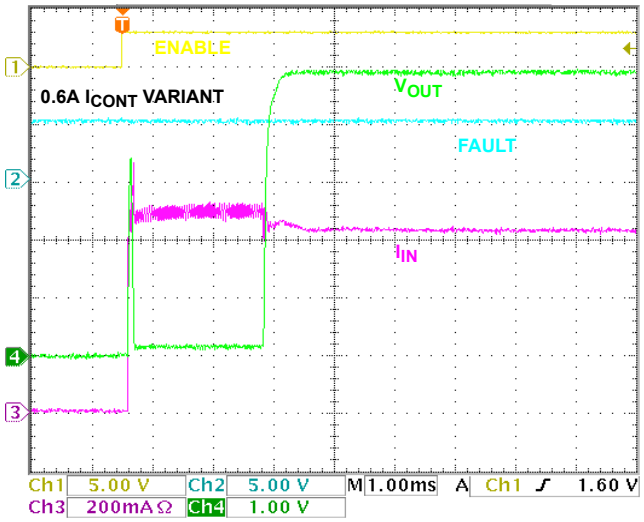


FIGURE 20. TURN-ON INTO MOMENTARY OC

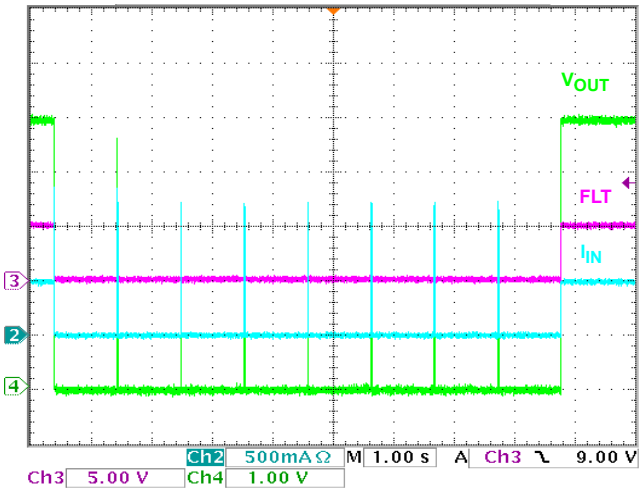


FIGURE 21. ISL6185 RETRY FUNCTION

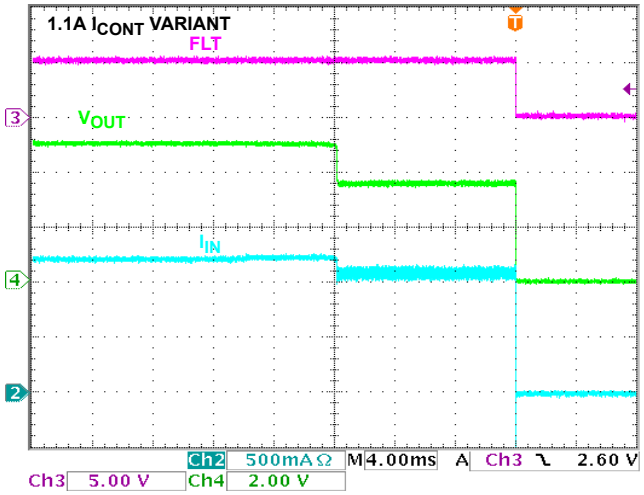


FIGURE 22. I_{LIM} WAVEFORM

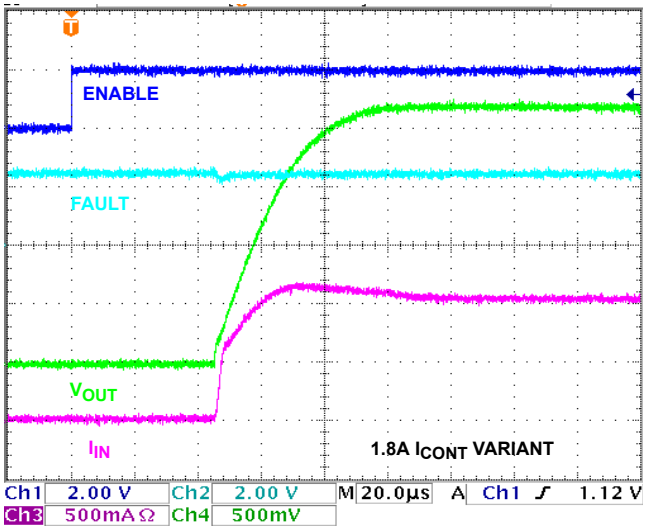


FIGURE 23. V_{IN} = 2.5V TURN-ON INTO 2.2Ω

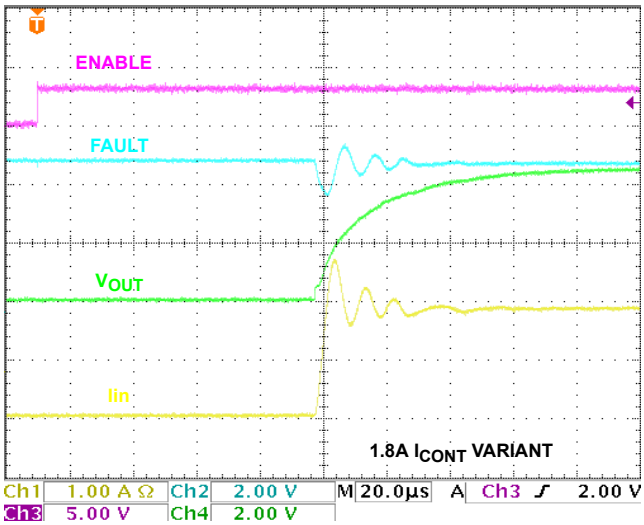


FIGURE 24. V_{IN} = 5V TURN-ON INTO 2.7Ω

Typical Performance Curves (Continued)

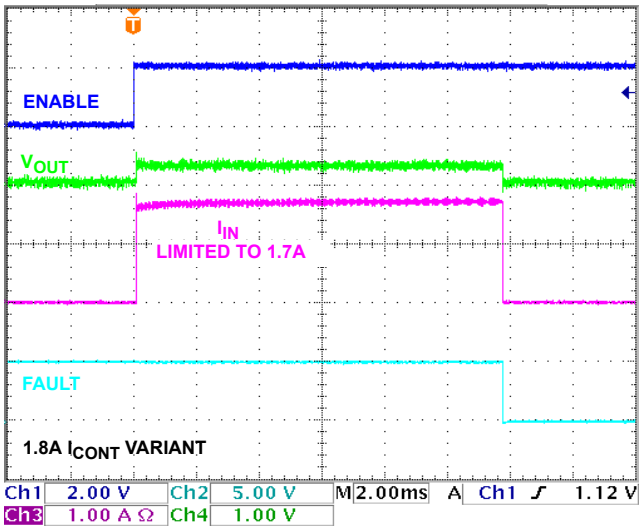


FIGURE 25. TURN-ON INTO A SHORT

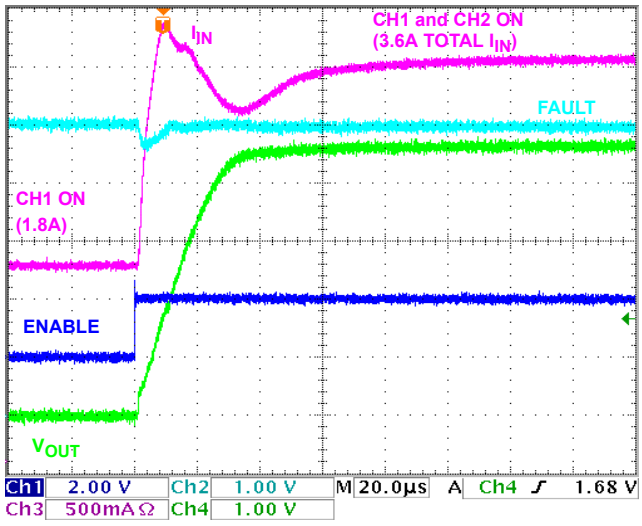


FIGURE 26. TURN-ON 2ND OUTPUT TO FULL LOAD

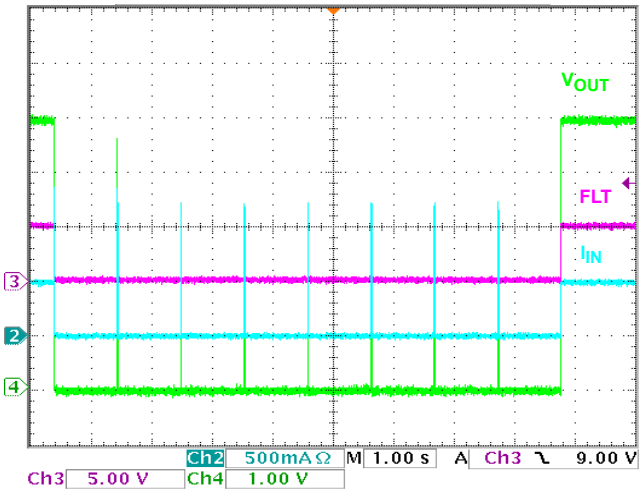


FIGURE 27. ISL6185 RETRY FUNCTION

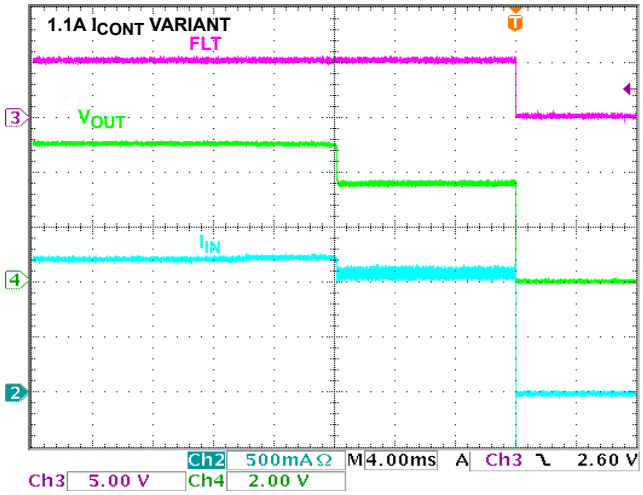
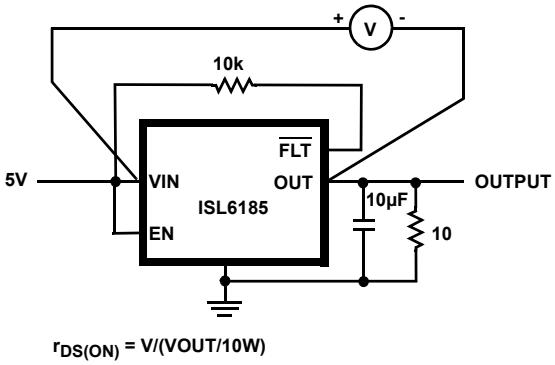


FIGURE 28. ILIM WAVEFORM

FIGURE 28. PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Test Circuits



$r_{DS(ON)} = V/(VOUT/10W)$

FIGURE 29A. $r_{DS(ON)}$

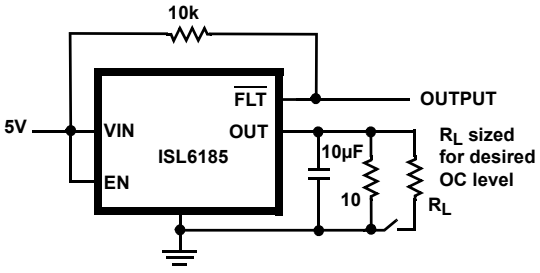


FIGURE 29B. CURRENT LIMITING

FIGURE 29. DC TEST CIRCUIT

Test Circuits (Continued)

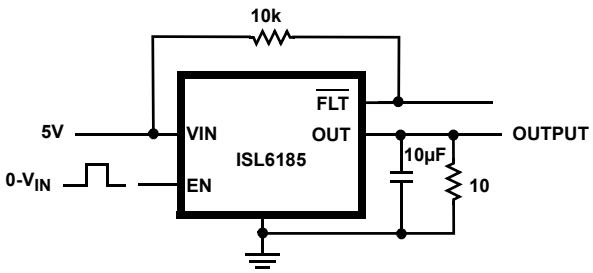


FIGURE 30. TRANSIENT TEST CIRCUIT

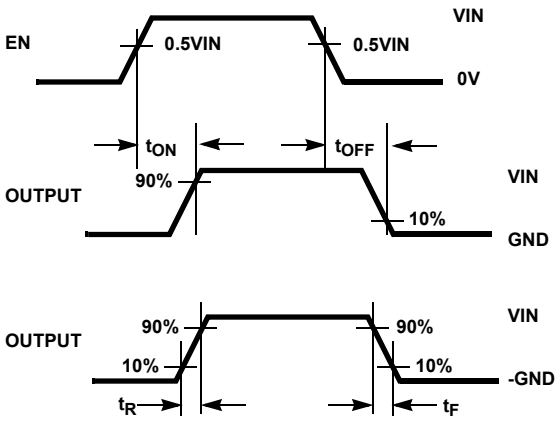
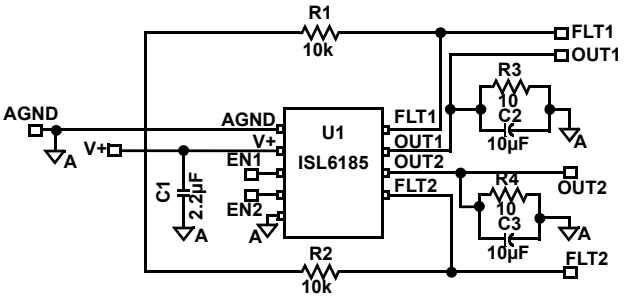


FIGURE 31. TRANSIENT WAVEFORM MEASUREMENT POINTS

ISL6185xEVAL1Z Schematic and Photo



NOTE: EXPOSED PAD on DFN packages only

FIGURE 32A. ISL6185xEVAL SCHEMATIC

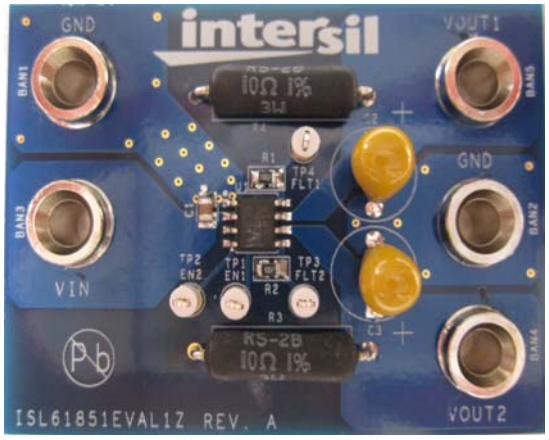


FIGURE 32B. ISL61851EVAL1Z BOARD PHOTO

FIGURE 32. ISL6185xEVAL1Z SCHEMATIC and ISL61851EVAL1Z PHOTOGRAPH

Application Information

Using the ISL6185xEVAL1Z Platform General and Biasing Information

There are three evaluation platforms for the ISL6185 family. There is one platform for each package style, each with a different continuous output current level and a mix of enable polarity and output retry or latch options. See page 4, at the end of the “Ordering Information” table, for information on the standard available evaluation board options. Figure 32A shows the common schematic for all three evaluation boards. See “Pin Configurations” on page 5 for details and differences.

The evaluation platform is biased and monitored through numerous labeled test points. See Table 1 for test point assignments and descriptions.

TABLE 1. ISL61851EVAL1Z TEST POINT ASSIGNMENTS

TP NAME	DESCRIPTION
GND	Eval Board and IC Gnd
V+	Eval Board and IC Bias
EN1	Enable Switch 1
EN2	Enable Switch 2
FLT2	Switch 2 Fault
OUT2	Switch Out 2
OUT1	Switch Out 1
FLT1	Switch 1 Fault

Upon proper bias of the evaluation platform and correct enabling of the IC, the ISL6185 will have a nominal $V_{IN}/10\Omega$ load current that is lower than the continuous current rating passing through each enabled switch. See Figures 13 and 14 for typical ISL6185 turn-on and turn-off waveforms.

External current loading in excess of the trip current level for the particular part being evaluated will result in the ISL6185 entering the current limiting mode. Figure 16 illustrates the current limiting mode for the ISL6185 product variants with 0.6A of continuous load current rating. The scope shot shows current limiting for ~12ms before it is turned off and the fault signal is asserted.

Application Considerations

The application considerations for the ISL6185 family are widely accepted best industry practices. Good decoupling practices on the VIN pin must be followed: placement close to the IC, with at least 2.2µF recommended. It is recommended to reduce the input and output inductance to the ISL6185 with good PCB layout practices.

When designing with the 1.5A and 1.8A versions in an implementation in which the output may be unloaded (open) while the ISL6185 is turned on, a minimum of 4.7µF of capacitive output load is recommended to prevent high dv/dt from unnecessarily activating the surge/ESD control circuit.

The ISL6185 provides several continuous current rated devices specified at V_{IN} = 5V; these are 0.6A, 1.1A, 1.5A and 1.8A options that are capable over the entire temperature extreme. At V_{IN} = 3.3V, the current capability is degraded, and the ISL6185 is specified at 0.6A, 1.1A, 1.3A and 1.5A, respectively. At V_{IN} = 2.5V, there are no minimum specifications, but a typical value is provided for +25°C operation (see “Electrical Specifications” on page 6). This degraded capability is due to the higher $r_{DS(ON)}$ of the FET switch at the lower bias voltage.

The enhanced thermal characteristics and increased number of bond wires allow the 10 Ld DFN to have a higher current capability than either the 8 Ld SOIC or the DFN.

TABLE 2. ISL6185XEVAL1Z BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6185	Intersil, ISL6185
R3 - R4	Output Load Resistors	10Ω, 5%, 3W
R1 - R2	FLT Output Pull-up Resistor	10kΩ, 0805
C1	Decoupling Capacitor	2.2µF, 0805
C2 - C3	Load Capacitor	10µF 16V Electrolytic, Radial Lead

© Copyright Intersil Americas LLC 2010-2012. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 1, 2012	FN6937.3	In “Features” on page 1 changed from: UL Recognized, File Number: E333469 (Applies to DFN Packages, SOIC Package to be Qualified Shortly) to: UL Recognized, File Number : E333469 In “Absolute Maximum Ratings” on page 6: Changed from: Output Current . . . . . Short Circuit Protected to: Output Current . . . . . .Short Circuit Protected Current Limit of 2.5A Updated “Package Outline Drawing” on page 20. Changed Note 1 "1982" to "1994".
December 2, 2011	FN6937.2	Page 1: Added "UL Recognized, File Number: E333469 (Applies to DFN packages, SOIC pkg to be qualified shortly)" to "Features" Page 8: Added Isc_5.5, Short Circuit Current with max of 2.5A to “Electrical Specifications” Page 19: Updated package outline drawing to most updated revision. Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly.
June 14, 2011	FN6937.1	Page 2: “Ordering Information”: added part numbers of parts installed on evaluation boards to Description column. Page 7: “Electrical Specifications” table: - For “Maximum Continuous Current, VIN = 2.5V,” changed “ISL61851C,D,G,H (SOIC)” to “ISL61851C,D,G,H,I,J,K,L (SOIC)” - For “Trip Current, V_{IN} = 5V”, changed “ISL61853I,J,K,L” to “ISL6185xI,J,K,L”. For “ISL61853M.N,O,P” changed MAX from “2.15” to “2.45”. - For “Trip Current, VIN = 3.3V” and “Trip Current, VIN = 2.5V” changed “ISL61853I,J,K,L“ to “ISL6185xI,J,K,L“. - For “Current Limit, VIN = 5V”, “Current Limit, VIN = 3.3V”, and “Current Limit, VIN = 2.5V”, changed “ISL61853I,J,K,L, VIN - VOUT = 1V” to “ISL6185xI,J,K,L, VIN - VOUT = 1V” - For “Short Circuit Current, VIN = 5V”, “Short Circuit Current, VIN = 3.3V” and “Short Circuit Current, VIN = 2.5V” changed “ISL61853I,J,K,L, VOUT = 0V” to “ISL6185xI,J,K,L, VOUT = 0V” Page 8: “Electrical Specifications” table: For the I/O Parameters Venr_5, Hys_Venr_5, Venr_3, Hys_Venr_3, Venr_2, and Hys_Venr_2: changed "ENABLE Rising Threshold" and "ENABLE Rising Threshold Hysteresis" to "EN / $\overline{EN}$ Rising Threshold" and "EN / $\overline{EN}$ Rising Threshold Hysteresis," for clarity. Page 8: Electrical Specifications table: Removed UV_{HYS}, POR Hysteresis specification. Page 20: Replaced Rev. 1 of M8.15 package outline drawing, dated 6/05, with Rev 2 (latest version), dated 11/10. Applied current Intersil datasheet template to document.
October 22, 2010	FN6937.0	Initial release.

Products

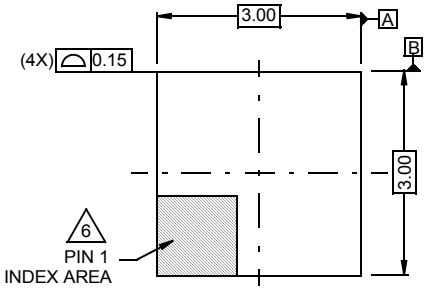
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information pages on intersil.com for ISL6185XXC (commercial version) and ISL6185XXI (industrial version).

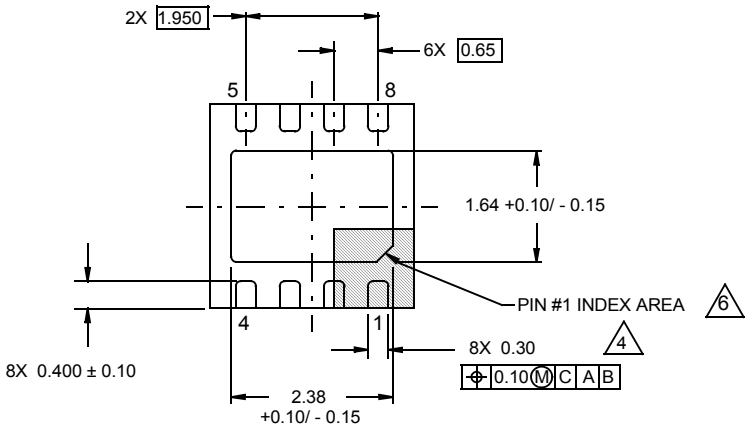
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/sear

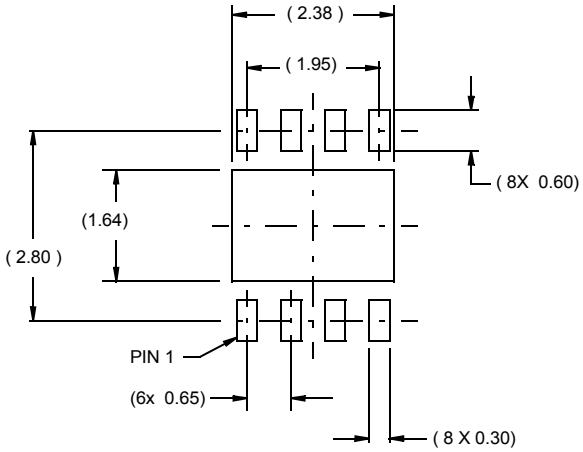
Package Outline Drawing
L8.3x3J
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 0 9/09



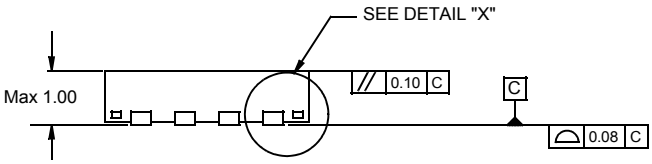
TOP VIEW



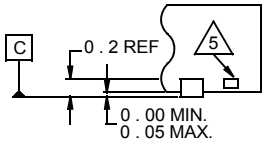
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

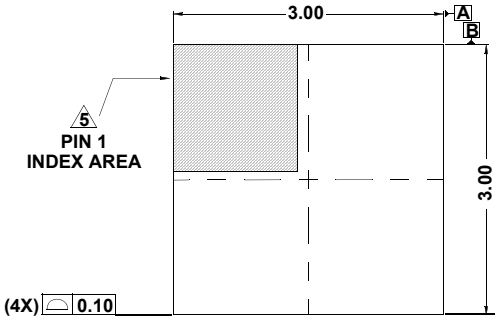
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

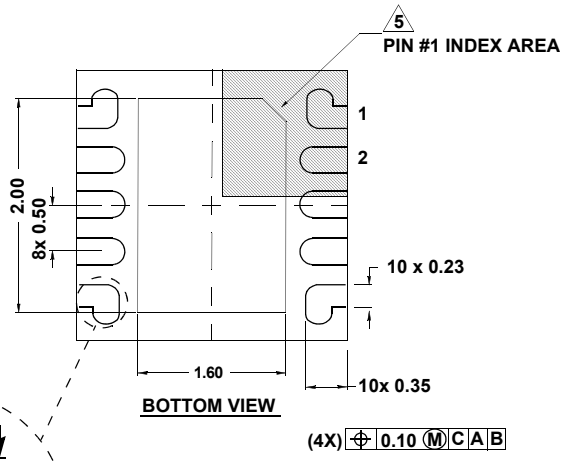
L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

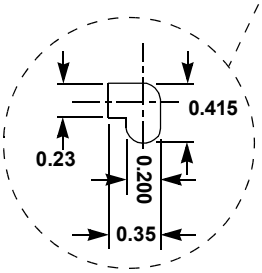
Rev 7, 10/11

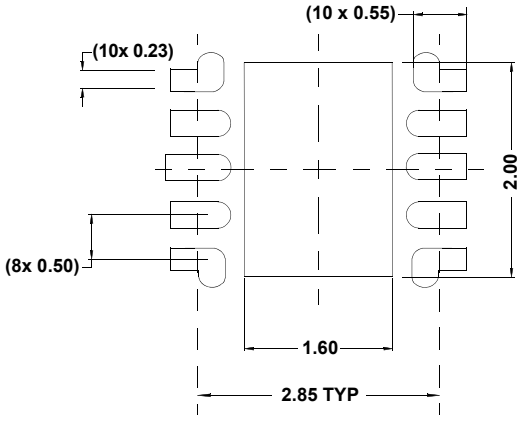


TOP VIEW

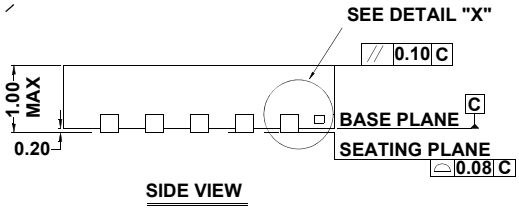


BOTTOM VIEW

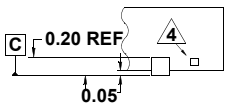




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

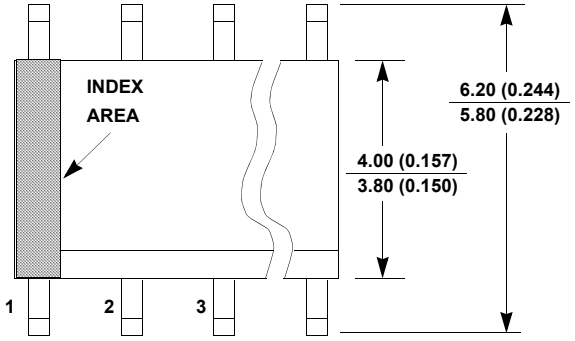
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

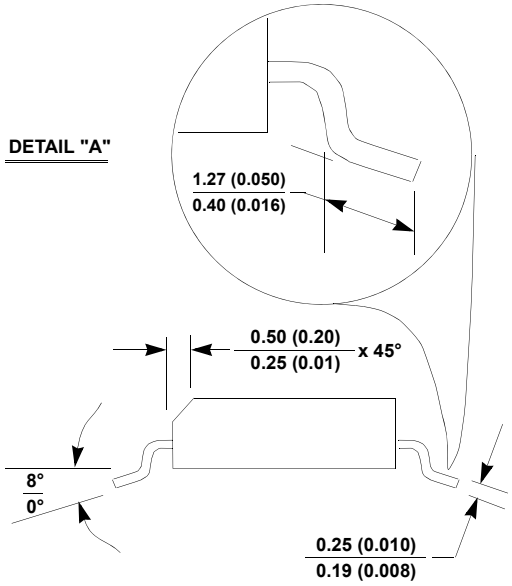
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

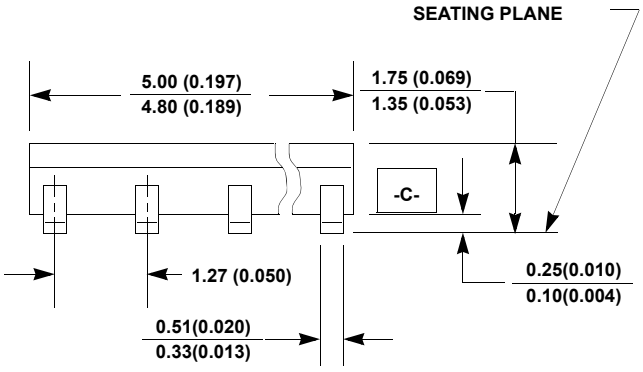
Rev 4, 1/12



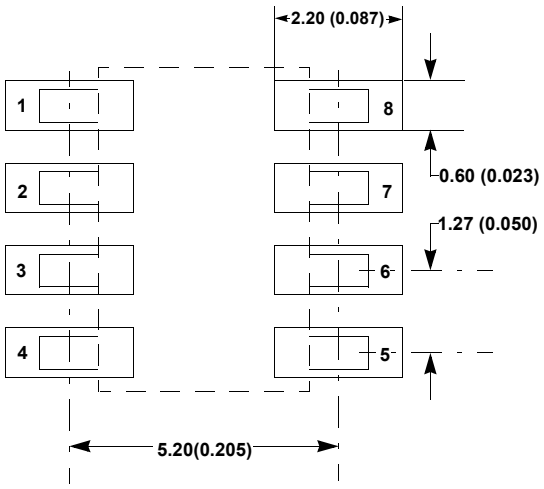
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.