

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200 \text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

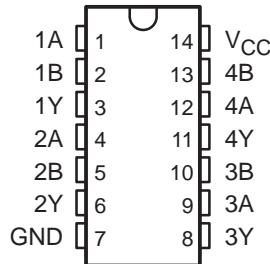
description

The 'AHC86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

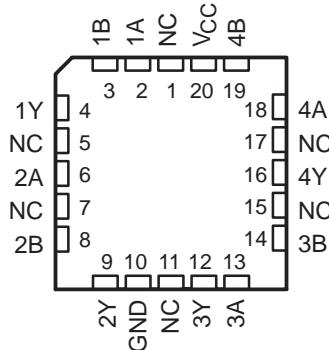
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54AHC86 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC86 is characterized for operation from -40°C to 85°C .

SN54AHC86 . . . J OR W PACKAGE
SN74AHC86 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



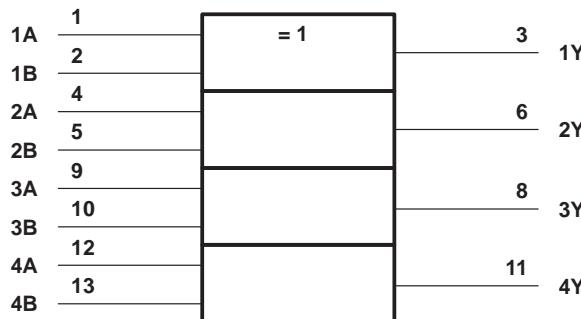
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54AHC86, SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249F – OCTOBER 1995 – REVISED JANUARY 2000

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



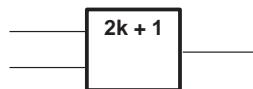
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V	
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V	
Output voltage range, V_O (see Note 1)	-0.5 V to V_{CC} + 0.5 V	
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA	
Continuous current through V_{CC} or GND	±50 mA	
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W	
DB package	96°C/W	
DGV package	127°C/W	
N package	80°C/W	
PW package	113°C/W	
Storage temperature range, T_{stg}	-65°C to 150°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54AHC86		SN74AHC86		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5	1.5	V
		$V_{CC} = 3$ V	2.1	2.1	2.1	
		$V_{CC} = 5.5$ V	3.85	3.85	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	0.5	0.5	V
		$V_{CC} = 3$ V	0.9	0.9	0.9	
		$V_{CC} = 5.5$ V	1.65	1.65	1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	-50	-50	-50	μ A
		$V_{CC} = 3.3$ V ± 0.3 V	-4	-4	-4	mA
		$V_{CC} = 5$ V ± 0.5 V	-8	-8	-8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	50	50	μ A
		$V_{CC} = 3.3$ V ± 0.3 V	4	4	4	mA
		$V_{CC} = 5$ V ± 0.5 V	8	8	8	
$\Delta t/\Delta V$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	100	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	20	20	
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHC86, SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249F – OCTOBER 1995 – REVISED JANUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC86	SN74AHC86	UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9	1.9	V
		3 V	2.9	3		2.9	2.9	
		4.5 V	4.4	4.5		4.4	4.4	
	I _{OH} = -4 mA	3 V	2.58			2.48	2.48	
		4.5 V	3.94			3.8	3.8	
	I _{OL} = 50 µA	2 V		0.1		0.1	0.1	
		3 V		0.1		0.1	0.1	
V _{OL}	I _{OL} = 4 mA	4.5 V		0.1		0.1	0.1	V
		3 V		0.36		0.5	0.44	
		4.5 V		0.36		0.5	0.44	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V		±0.1		±1*	±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		2		20	20	µA
C _i	V _I = V _{CC} or GND	5 V	4	10			10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC86	SN74AHC86	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t _{PLH}	A or B	Y	C _L = 15 pF	7**	11**		1**	13**	1	13
t _{PHL}				7**	11**		1**	13**	1	13
t _{PLH}	A or B	Y	C _L = 50 pF	9.5	14.5		1	16.5	1	16.5
t _{PHL}				9.5	14.5		1	16.5	1	16.5

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC86	SN74AHC86	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t _{PLH}	A or B	Y	C _L = 15 pF	4.8**	6.8**		1**	8**	1	8
t _{PHL}				4.8**	6.8**		1**	8**	1	8
t _{PLH}	A or B	Y	C _L = 50 pF	6.3	8.8		1	10	1	10
t _{PHL}				6.3	8.8		1	10	1	10

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

SN54AHC86, SN74AHC86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249F – OCTOBER 1995 – REVISED JANUARY 2000

noise characteristics, $V_{CC} = 5$ V, $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC86			UNIT	
	MIN	TYP	MAX		
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.4		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

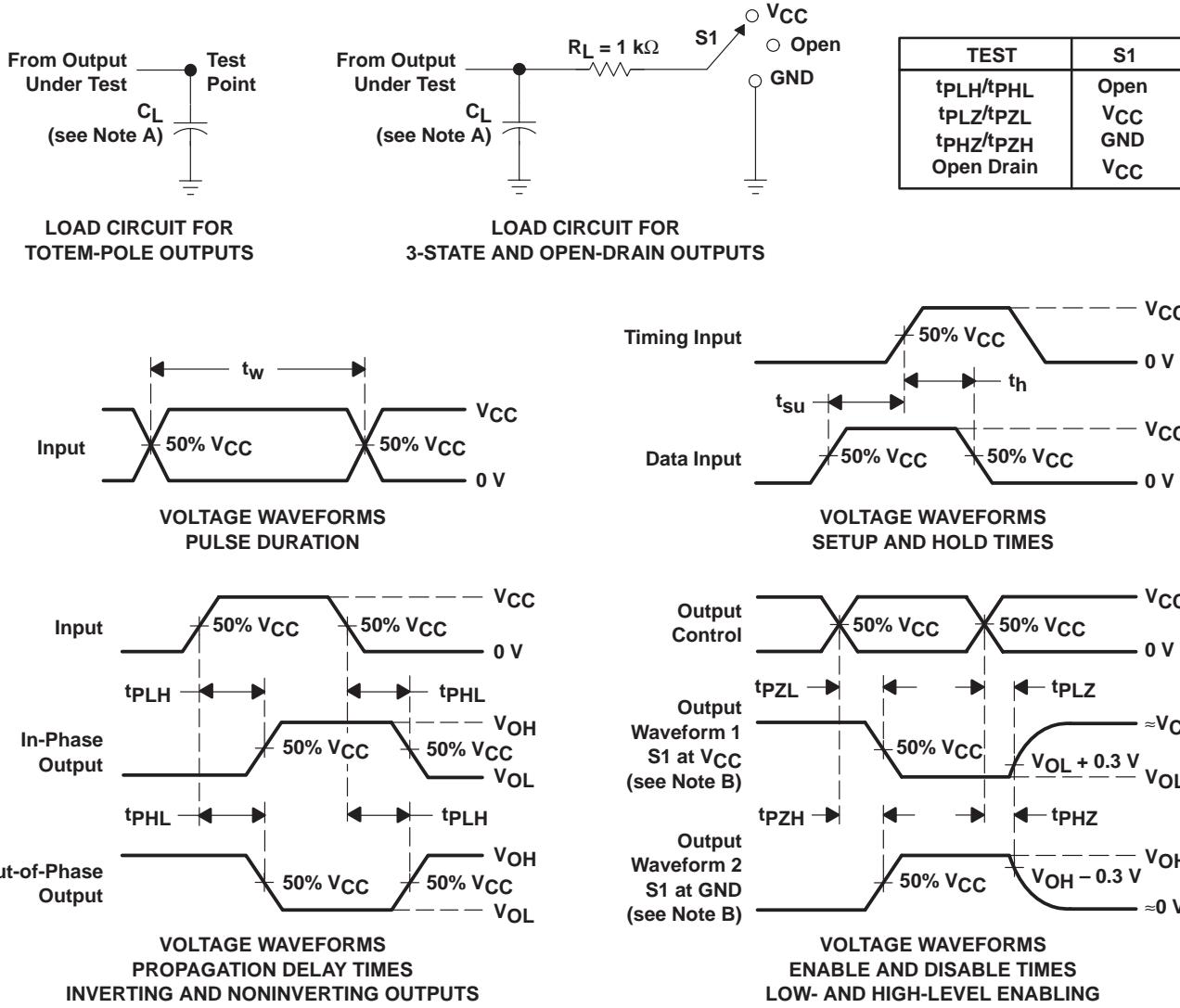
operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1$ MHz	18	pF

SN54AHC86, SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249F – OCTOBER 1995 – REVISED JANUARY 2000

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated