

1Mx16

16Mb DRAM WITH EDO PAGE MODE

PRELIMINARY INFORMATION
MARCH 2016

FEATURES

- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval:
 - Auto refresh Mode: 1,024 cycles /16 ms
 - $\overline{\text{RAS}}$ -Only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR), and Hidden
 - Self refresh Mode: 1,024 cycles /128 ms
- JEDEC standard pinout
- Single power supply:
 $3.3V \pm 10\%$
- Byte Write and Byte Read operation via two $\overline{\text{CAS}}$
- Industrial Temperature Range: -40°C to +85°C

DESCRIPTION

The ISSI IS41LV16100D is a 1,048,576 x 16-bit high-performance CMOS Dynamic Random Access Memories. These devices offer a cycle access called Extended Data Out (EDO) Page Mode. EDO Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 30 ns per 16-bit word. It is asynchronous, as it does not require a clock signal input to synchronize commands and I/O.

These features make the IS41LV16100D ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications that run without a clock to synchronize with the DRAM.

The IS41LV16100D is packaged in a 42-pin 400-mil SOJ and 400-mil 50/44 pin TSOP (Type II).

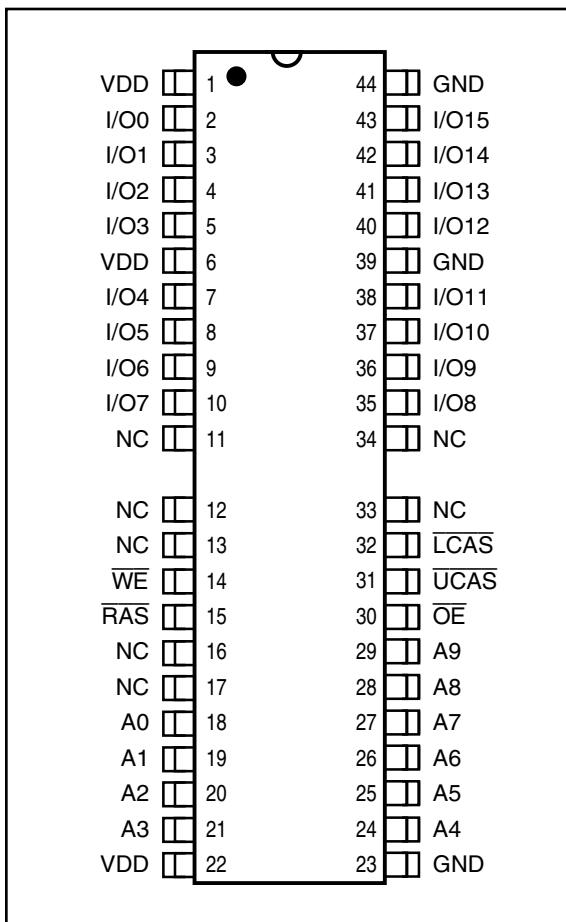
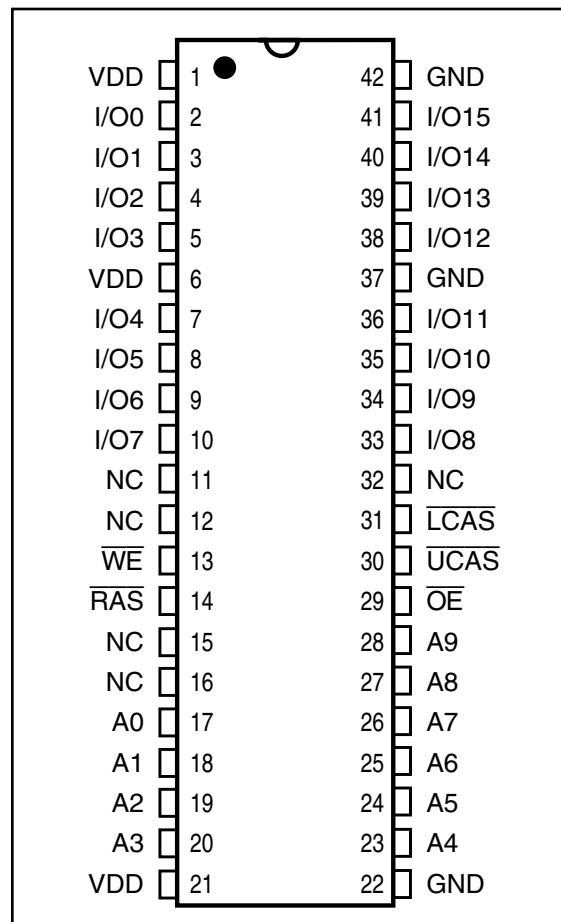
KEY TIMING PARAMETERS

Parameter	-50	Unit
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	50	ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	14	ns
Max. Column Address Access Time (t_{CAA})	25	ns
Min. EDO Page Mode Cycle Time (t_{PC})	30	ns
Min. Read/Write Cycle Time (t_{RC})	85	ns

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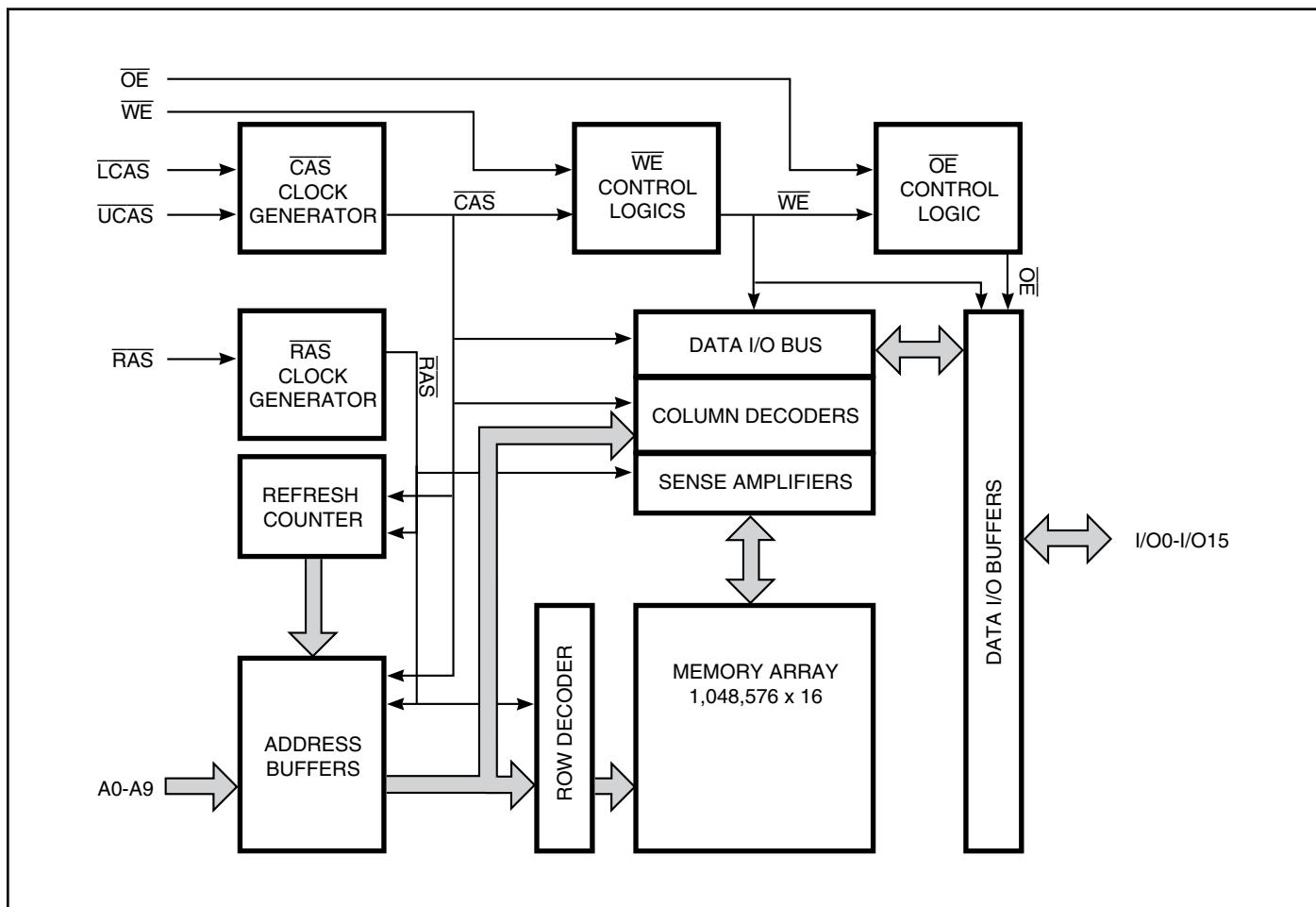
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

IS41LV16100D**PIN CONFIGURATIONS****50(44)-Pin TSOP (Type II)****42-Pin SOJ****PIN DESCRIPTIONS**

A0-A9	Address Inputs
I/O0-15	Data Inputs/Outputs
WE	Write Enable
OE	Output Enable
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
VDD	Power
GND	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE⁽⁵⁾

Function	RAS	LCAS	UCAS	WE	OE	Address tr/tc	I/O
Standby	H	X	X	X	X	X	High-Z
Read: Word	L	L	L	H	L	ROW/COL	DOUT
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, DOUT Upper Byte, High-Z
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, DOUT
Write: Word (Early Write)	L	L	L	L	X	ROW/COL	DIN
Write: Lower Byte (Early Write)	L	L	H	L	X	ROW/COL	Lower Byte, DIN Upper Byte, High-Z
Write: Upper Byte (Early Write)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, DIN
Read-Write ^(1,2)	L	L	L	H→L	L→H	ROW/COL	DOUT, DIN
EDO Page-Mode Read ⁽²⁾	L	H→L	H→L	H	L	ROW/COL	DOUT
1st Cycle:	L	H→L	H→L	H	L	NA/COL	DOUT
2nd Cycle:	L	L→H	L→H	H	L	NA/NA	DOUT
Any Cycle:	L	L→H	L→H	H	L	NA/NA	DOUT
EDO Page-Mode Write ⁽¹⁾	L	H→L	H→L	L	X	ROW/COL	DIN
1st Cycle:	L	H→L	H→L	L	X	NA/COL	DIN
2nd Cycle:	L	H→L	H→L	H→L	L→H	ROW/COL	DOUT, DIN
Read-Write	L	H→L	H→L	H→L	L→H	NA/COL	DOUT, DIN
Hidden Refresh	Read ⁽²⁾	L→H→L	L	H	L	ROW/COL	DOUT
	Write ^(1,3)	L→H→L	L	L	X	ROW/COL	DOUT
RAS-Only Refresh		L	H	H	X	ROW/NA	High-Z
CBR Refresh ⁽⁴⁾	H→L	L	L	H	X	X	High-Z

Notes:

1. These WRITE cycles may also be BYTE WRITE cycles (either LCAS or UCAS active).
2. These READ cycles may also be BYTE READ cycles (either LCAS or UCAS active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active (LCAS or UCAS).
5. Commands valid only after proper initialization.

IS41LV16100D

Functional Description

The IS41LV16100D is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits. These are entered ten bits (A0-A9) at time. The row address is latched by the Row Address Strobe (RAS). The column address is latched by the Column Address Strobe (CAS). RAS is used to latch the first nine bits and CAS is used to latch the latter nine bits.

The IS41LV16100D has two CAS controls, LCAS and UCAS. The LCAS and UCAS inputs internally generates a CAS signal functioning in an identical manner to the single CAS input on the other 1M x 16 DRAMs. The key difference is that each CAS controls its corresponding I/O tristate logic (in conjunction with OE and WE and RAS). LCAS controls I/O0 through I/O7 and UCAS controls I/O8 through I/O15.

The IS41LV16100D CAS function is determined by the first CAS (LCAS or UCAS) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the IS41LV16100D BYTE READ and BYTE WRITE cycle capabilities.

Memory Cycle

A memory cycle is initiated by bring RAS LOW and it is terminated by returning both RAS and CAS HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum tRAS time has expired. A new cycle must not be initiated until the minimum precharge time tRP, tCP has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of CAS or OE, whichever occurs last, while holding WE HIGH. The column address must be held for a minimum time specified by tAR. Data Out becomes valid only when trAC, tAA, tcAC and toEA are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of CAS and WE, whichever occurs last. The input data must be valid at or before the falling edge of CAS or WE, whichever occurs first.

Auto Refresh Cycle

To retain data, 1,024 refresh cycles are required in each 16 ms period. There are two ways to refresh the memory.

1. By clocking each of the 1,024 row addresses (A0 through A9) with RAS at least once every tREF max. Any read, write, read-modify-write or RAS-only cycle refreshes the addressed row.
2. Using a CAS-before-RAS refresh cycle. CAS-before-RAS refresh is activated by the falling edge of RAS, while holding CAS LOW. In CAS-before-RAS refresh cycle,

an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

CAS-before-RAS is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Self Refresh Cycle

The Self Refresh allows the user a dynamic refresh, data retention mode at the extended refresh period of 128 ms. i.e., 125 μ s per row when using distributed CBR refreshes. The feature also allows the user the choice of a fully static, low power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding RAS LOW for the specified tRAS.

The Self Refresh mode is terminated by driving RAS HIGH for a minimum time of tRP. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh.

However, if the DRAM controller utilizes a RAS-only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

Extended Data Out Page Mode

EDO page mode operation permits all 1,024 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next CAS cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the CAS cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the CAS cycle time becomes shorter.

In EDO page mode, due to the extended data function, the CAS cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one RAS cycle, but the performance is equivalent to that of the fast page mode in that case.

Power-On

During Power-On, RAS, UCAS, LCAS, and WE must all track with VDD (HIGH) to avoid current surges, and allow initialization to continue. An initial pause of 200 μ s is required followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS signal).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameters	Rating	Unit
V _T	Voltage on Any Pin Relative to GND	-0.5 to +4.6	V
V _{DD}	Supply Voltage	-0.5 to +4.6	V
I _{OUT}	Output Current	50	mA
P _D	Power Dissipation	1	W
T _A	Industrial Temperature	-40 to +85	°C
T _{TG}	Storage Temperature	-55 to +125	°C

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		3.0	3.3	3.6	V
V _{IH}	Input High Voltage		2.0	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage		-0.3	—	0.8	V
I _{IL}	Input Leakage Current	Any input 0V ≤ V _{IN} ≤ V _{DD} Other inputs not under test = 0V	-5	5	5	µA
I _{IO}	Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ V _{OUT} ≤ V _{DD}	-5	5	5	µA
V _{OH}	Output High Voltage Level	I _{OH} = -2.0 mA	2.4	—	—	V
V _{OL}	Output Low Voltage Level	I _{OL} = 2.0 mA	—	—	0.4	V

CAPACITANCE^(1,2)

Symbol	Parameter	Max.	Unit
C _{IN1}	Input Capacitance: A0-A9	5	pF
C _{IN2}	Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	7	pF
C _{IO}	Data Input/Output Capacitance: I/O0-I/O15	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS⁽¹⁾ (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Max.	Unit
IDD1	Stand-by Current: TTL	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}} \geq V_{IH}$	2	mA
IDD2	Stand-by Current: CMOS	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}} \geq V_{DD} - 0.2V$	1	mA
IDD3	Operating Current: Random Read/Write ^(2,3,4)	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}},$ Address Cycling, $t_{RC} = t_{RC}$ (min.)	90	mA
	Average Power Supply Current			
IDD4	Operating Current: Fast Page Mode ^(2,3,4)	$\overline{\text{RAS}} = V_{IL}, \overline{\text{LCAS}}, \overline{\text{UCAS}},$ Cycling $t_{PC} = t_{PC}$ (min.)	30	mA
	Average Power Supply Current			
IDD5	Refresh Current: $\overline{\text{RAS}}$ -Only ^(2,3)	$\overline{\text{RAS}}$ Cycling, $\overline{\text{LCAS}}, \overline{\text{UCAS}} \geq V_{IH}$ $t_{RC} = t_{RC}$ (min.)	60	mA
	Average Power Supply Current			
IDD6	Refresh Current: CBR ^(2,3,5)	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}}$ Cycling $t_{RC} = t_{RC}$ (min.)	60	mA
	Average Power Supply Current			

Notes:

1. An initial pause of 200 μs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS^(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50		-60		Units
		Min.	Max.	Min.	Max.	
t _{RC}	Random READ or WRITE Cycle Time	85	—	110	—	ns
t _{TRAC}	Access Time from $\overline{\text{RAS}}^{(6, 7)}$	—	50	—	60	ns
t _{CAC}	Access Time from $\overline{\text{CAS}}^{(6, 8, 15)}$	—	14	—	15	ns
t _{AA}	Access Time from Column-Address ⁽⁶⁾	—	25	—	30	ns
t _{TRAS}	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	ns
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	30	—	40	—	ns
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width ⁽²⁶⁾	8	10K	10	10K	ns
t _{CP}	$\overline{\text{CAS}}$ Precharge Time ^(9, 25)	9	—	10	—	ns
t _{CSH}	$\overline{\text{CAS}}$ Hold Time ⁽²¹⁾	50	—	60	—	ns
t _{TRCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time ^(10, 20)	12	37	20	45	ns
t _{TASR}	Row-Address Setup Time	0	—	0	—	ns
t _{TRAH}	Row-Address Hold Time	8	—	10	—	ns
t _{TASC}	Column-Address Setup Time ⁽²⁰⁾	0	—	0	—	ns
t _{TCAH}	Column-Address Hold Time ⁽²⁰⁾	8	—	10	—	ns
t _{TAR}	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$)	30	—	40	—	ns
t _{TRAD}	$\overline{\text{RAS}}$ to Column-Address Delay Time ⁽¹¹⁾	14	25	15	30	ns
t _{TRAL}	Column-Address to $\overline{\text{RAS}}$ Lead Time	25	—	30	—	ns
t _{TRPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	—	5	—	ns
t _{TRSH}	$\overline{\text{RAS}}$ Hold Time ⁽²⁷⁾	14	—	15	—	ns
t _{TRHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	37	—	37	—	ns
t _{TCLZ}	$\overline{\text{CAS}}$ to Output in Low-Z ^(15, 29)	0	—	0	—	ns
t _{TCRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time ⁽²¹⁾	5	—	5	—	ns
t _{TOD}	Output Disable Time ^(19, 28, 29)	3	12	3	12	ns
t _{TOE/TOEA}	Output Enable Time ^(15, 16)	—	14	—	15	ns
t _{TOEHC}	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	15	—	15	—	ns
t _{TOEP}	$\overline{\text{OE}}$ HIGH Pulse Width	10	—	10	—	ns
t _{TOES}	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	ns
t _{TRCS}	Read Command Setup Time ^(17, 20)	0	—	0	—	ns
t _{TRRH}	Read Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹²⁾	0	—	0	—	ns
t _{TRCH}	Read Command Hold Time (referenced to $\overline{\text{CAS}}$) ^(12, 17, 21)	0	—	0	—	ns
t _{WCW}	Write Command Hold Time ^(17, 27)	8	—	10	—	ns
t _{WCW}	Write Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹⁷⁾	40	—	50	—	ns

AC CHARACTERISTICS (Continued)^(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50		-60		Units
		Min.	Max.	Min.	Max.	
tWP	Write Command Pulse Width ⁽¹⁷⁾	8	—	10	—	ns
tWPZ	WE Pulse Widths to Disable Outputs	10	—	10	—	ns
tRWL	Write Command to RAS Lead Time ⁽¹⁷⁾	13	—	15	—	ns
tcWL	Write Command to CAS Lead Time ^(17, 21)	8	—	15	—	ns
twCS	Write Command Setup Time ^(14, 17, 20)	0	—	0	—	ns
tdHR	Data-in Hold Time (referenced to RAS)	39	—	40	—	ns
tACH	Column-Address Setup Time to CAS precharge during WRITE cycle	15	—	15	—	ns
toEH	OE Hold Time from WE during READ-MODIFY-WRITE cycle ⁽¹⁸⁾	14	—	15	—	ns
tdS	Data-In Setup Time ^(15, 22)	0	—	0	—	ns
tdH	Data-In Hold Time ^(15, 22)	8	—	15	—	ns
trWC	READ-MODIFY-WRITE Cycle Time	110	—	155	—	ns
trWD	RAS to WE Delay Time during READ-MODIFY-WRITE Cycle ⁽¹⁴⁾	65	—	85	—	ns
tcWD	CAS to WE Delay Time ^(14, 20)	26	—	40	—	ns
tAWD	Column-Address to WE Delay Time ⁽¹⁴⁾	40	—	55	—	ns
tPC	EDO Page Mode READ or WRITE Cycle Time ⁽²⁴⁾	30	—	40	—	ns
trASP	RAS Pulse Width in EDO Page Mode	50	100K	60	100K	ns
tCPA	Access Time from CAS Precharge ⁽¹⁵⁾	—	30	—	35	ns
tPRWC	EDO Page Mode READ-WRITE Cycle Time ⁽²⁴⁾	56	—	56	—	ns
tCOH	Data Output Hold after CAS LOW	5	—	5	—	ns
toFF	Output Buffer Turn-Off Delay from CAS or RAS ^(13,15,19, 29)	3	12	3	15	ns
tWHz	Output Disable Delay from WE	3	10	3	15	ns
tCLCH	Last CAS going LOW to First CAS returning HIGH ⁽²³⁾	10	—	10	—	ns
tCSR	CAS Setup Time (CBR REFRESH) ^(30, 20)	5	—	5	—	ns
tCHR	CAS Hold Time (CBR REFRESH) ^(30, 21)	8	—	10	—	ns
tORD	OE Setup Time prior to RAS during HIDDEN REFRESH Cycle	0	—	0	—	ns
tWRP	WE Setup Time (CBR Refresh)	5	—	5	—	ns
tWRH	WE Hold Time (CBR Refresh)	8	—	10	—	ns
tREF	Auto Refresh Period (1,024 Cycles)	—	16	—	16	ms
tREF	Self Refresh Period (1,024 Cycles)	—	128	—	128	ms
tr	Transition Time (Rise or Fall) ^(2, 3)	1	50	1	50	ns

Note:

The -60 timing parameters are shown for reference only. The -50 speed option supports 50ns and 60ns timing specifications.

AC TEST CONDITIONS

Output load: One TTL Load and 50 pF

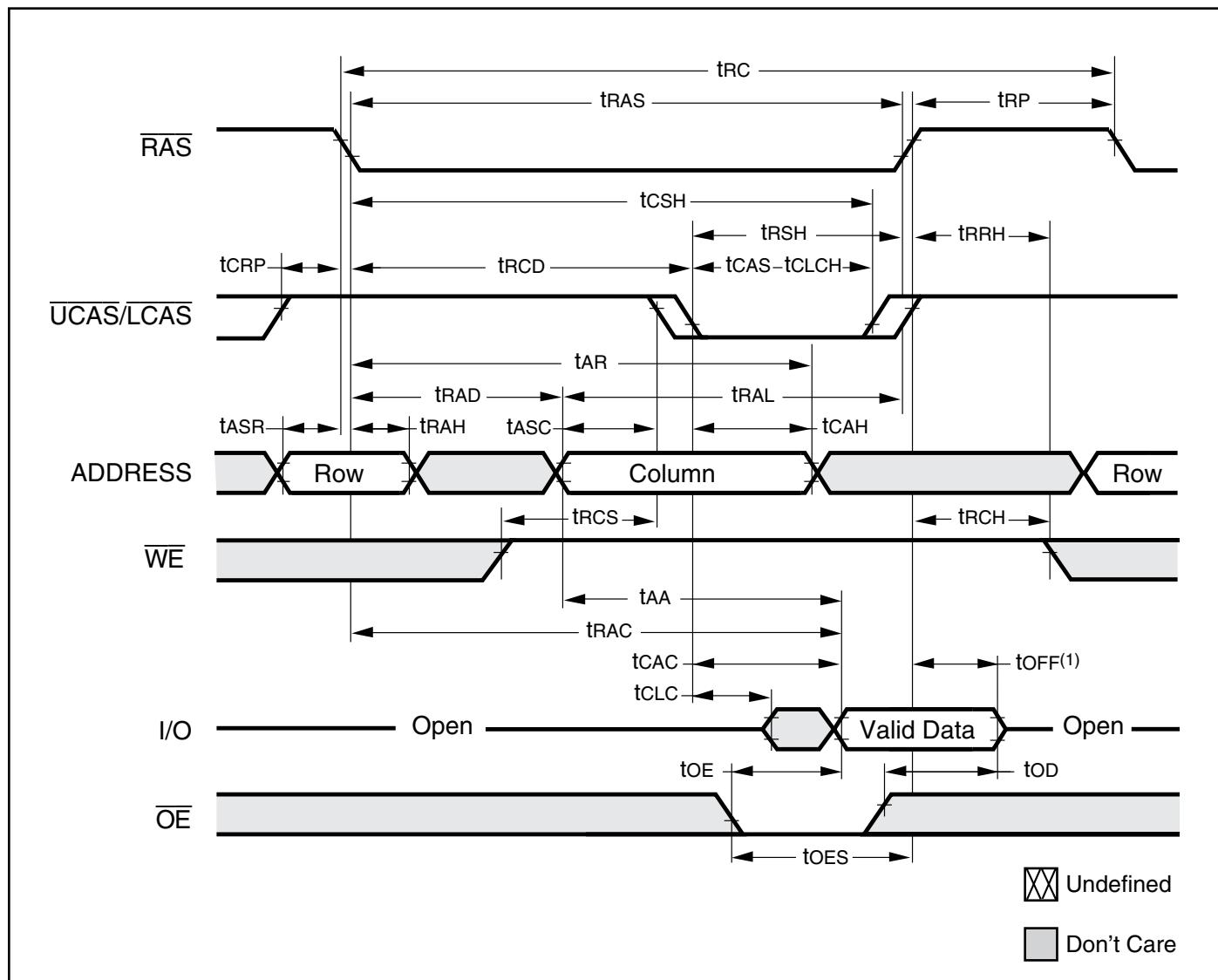
Input timing reference levels: $V_{IH} = 2.0V$, $V_{IL} = 0.8V$

Output timing reference levels: $V_{OH} = 2.4V$, $V_{OL} = 0.4V$

Notes:

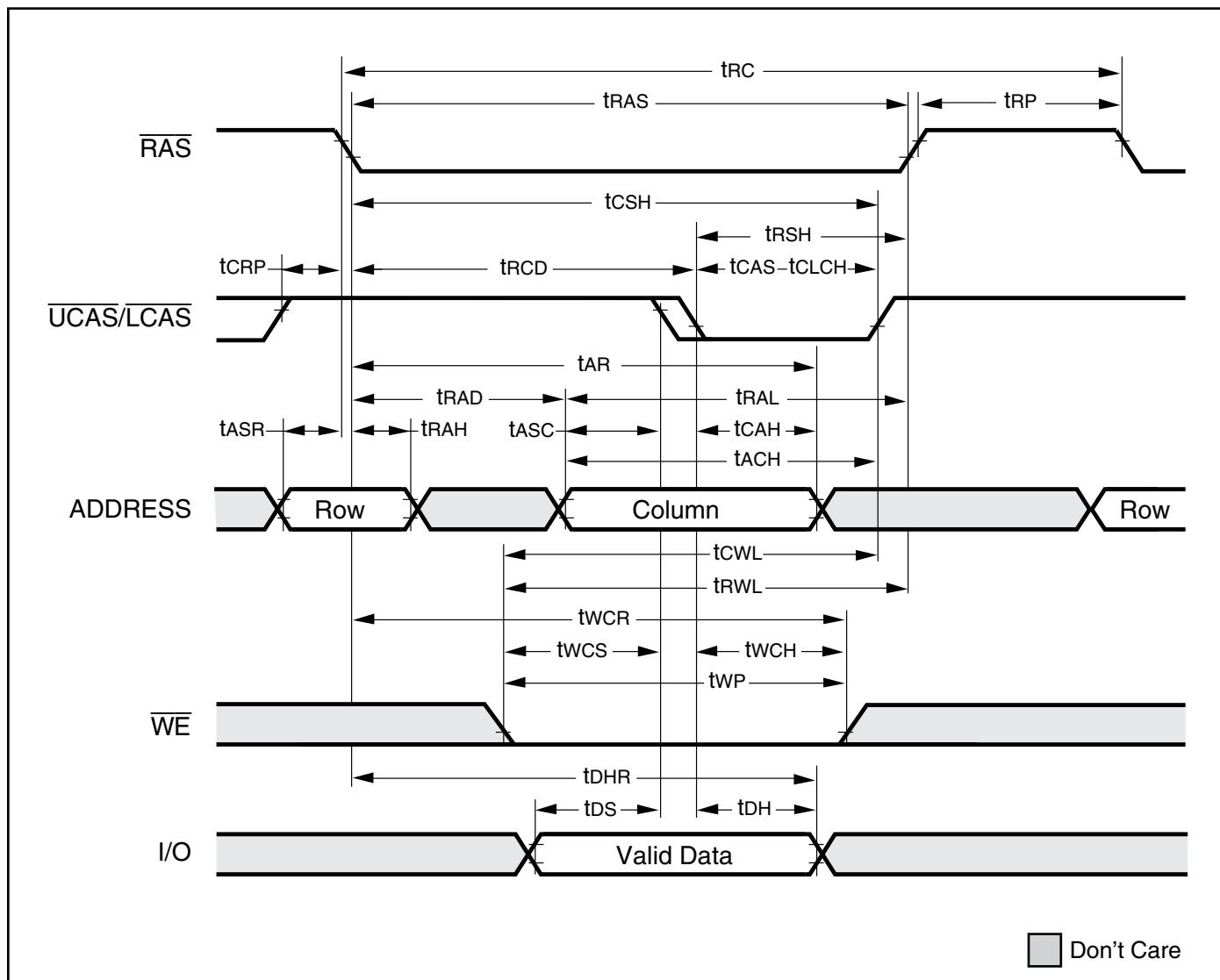
1. An initial pause of 200 μs is required after power-up followed by eight \overline{RAS} refresh cycle (\overline{RAS} -Only or CBR) before proper device operation is assured. The eight \overline{RAS} cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If \overline{CAS} and $\overline{RAS} = V_{IH}$, data output is High-Z.
5. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} \leq t_{RC} (MAX)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RC} \leq t_{RC} (MAX)$.
9. If CAS is LOW at the falling edge of \overline{RAS} , data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, CAS and RAS must be pulsed for t_{CP} .
10. Operation with the $t_{RC} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RC} (MAX)$ is specified as a reference point only; if t_{RC} is greater than the specified $t_{RC} (MAX)$ limit, access time is controlled exclusively by t_{CAC} .
11. Operation within the $t_{RAD} (MAX)$ limit ensures that $t_{RCD} (MAX)$ can be met. $t_{RAD} (MAX)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (MAX)$ limit, access time is controlled exclusively by t_{AA} .
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. $t_{OFF} (MAX)$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
14. t_{WCS} , t_{RWL} , t_{AWD} and t_{CWL} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \leq t_{WCS} (MIN)$, the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWL} \leq t_{RWL} (MIN)$, $t_{AWD} \leq t_{AWD} (MIN)$ and $t_{CWL} \leq t_{CWL} (MIN)$, the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until CAS and \overline{RAS} or \overline{OE} go back to V_{IH}) is indeterminate. \overline{OE} held HIGH and \overline{WE} taken LOW after \overline{CAS} goes LOW result in a LATE WRITE (\overline{OE} -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding \overline{CAS} input, I/O0-I/O7 by \overline{LCAS} and I/O8-I/O15 by \overline{UCAS} .
16. During a READ cycle, if \overline{OE} is LOW then taken HIGH before \overline{CAS} goes HIGH, I/O goes open. If \overline{OE} is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as \overline{WE} going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met (\overline{OE} HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if CAS remains LOW and \overline{OE} is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. The first χ_{CAS} edge to transition LOW.
21. The last χ_{CAS} edge to transition HIGH.
22. These parameters are referenced to \overline{CAS} leading edge in EARLY WRITE cycles and \overline{WE} leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling χ_{CAS} edge to first rising χ_{CAS} edge.
24. Last rising χ_{CAS} edge to next cycle's last rising χ_{CAS} edge.
25. Last rising χ_{CAS} edge to first falling χ_{CAS} edge.
26. Each χ_{CAS} must meet minimum pulse width.
27. Last χ_{CAS} to go LOW.
28. I/Os controlled, regardless \overline{UCAS} and \overline{LCAS} .
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

READ CYCLE

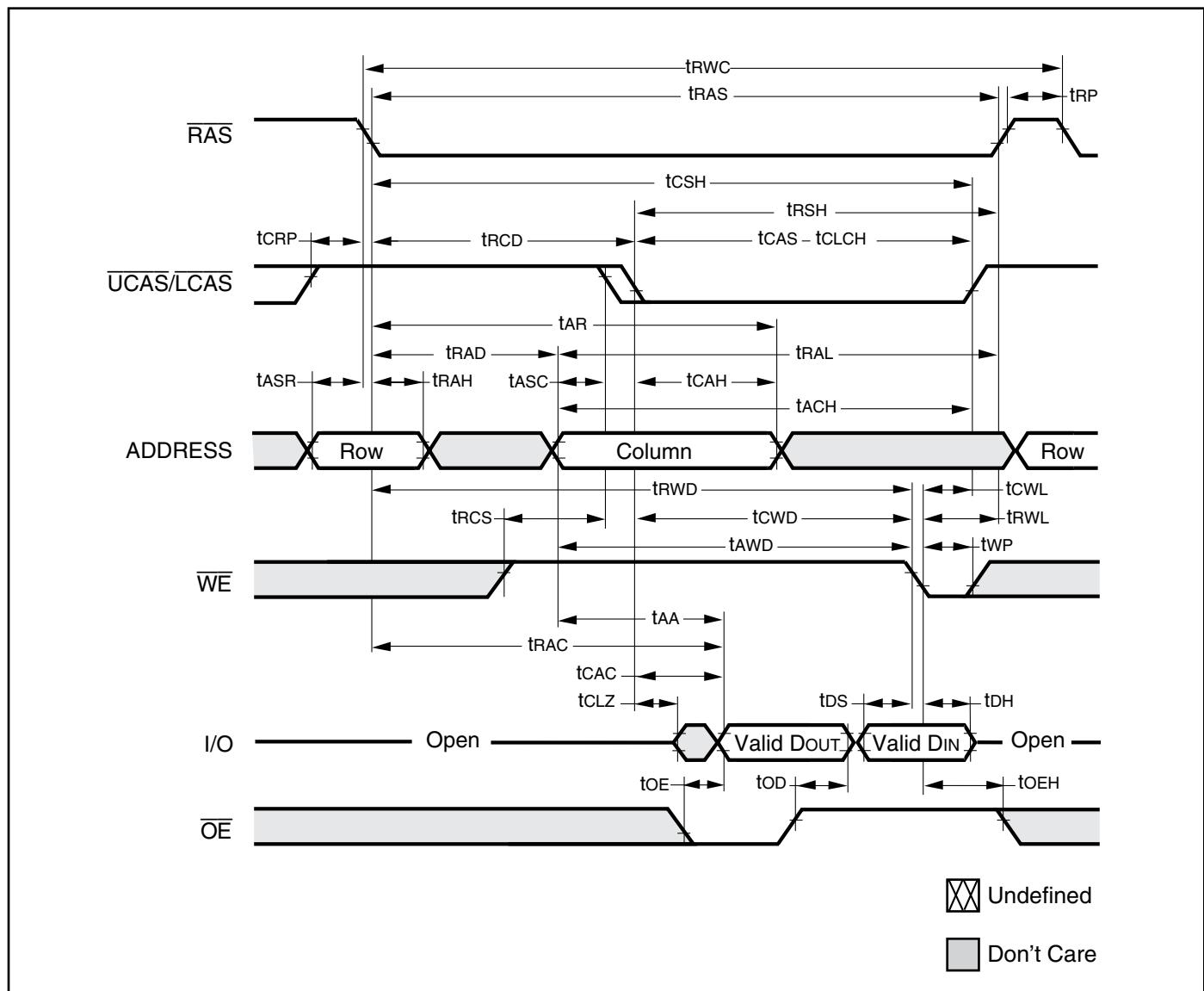


Note:

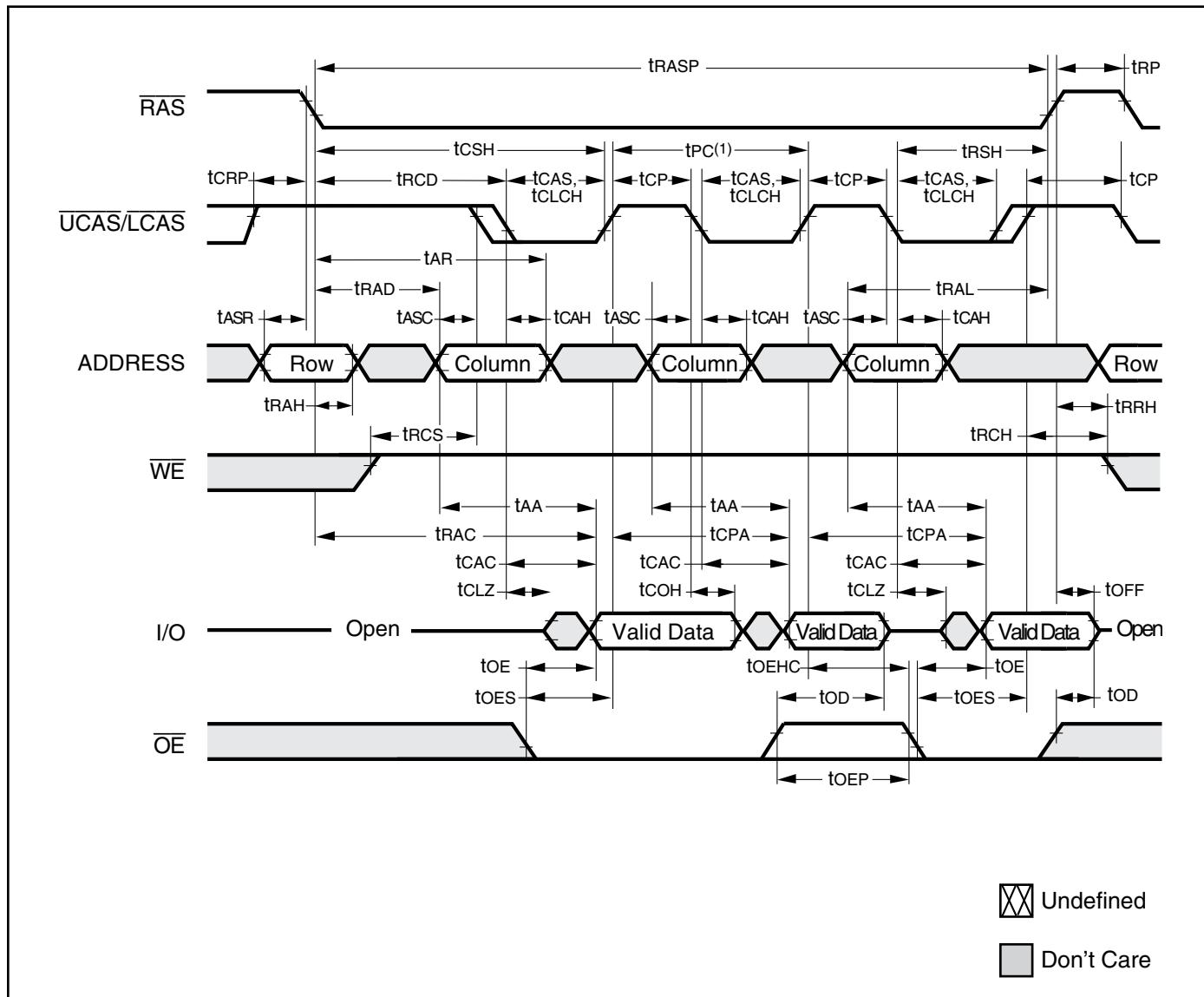
1. tOFF is referenced from rising edge of **RAS** or **CAS**, whichever occurs last.

EARLY WRITE CYCLE (\overline{OE} = DON'T CARE)

READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



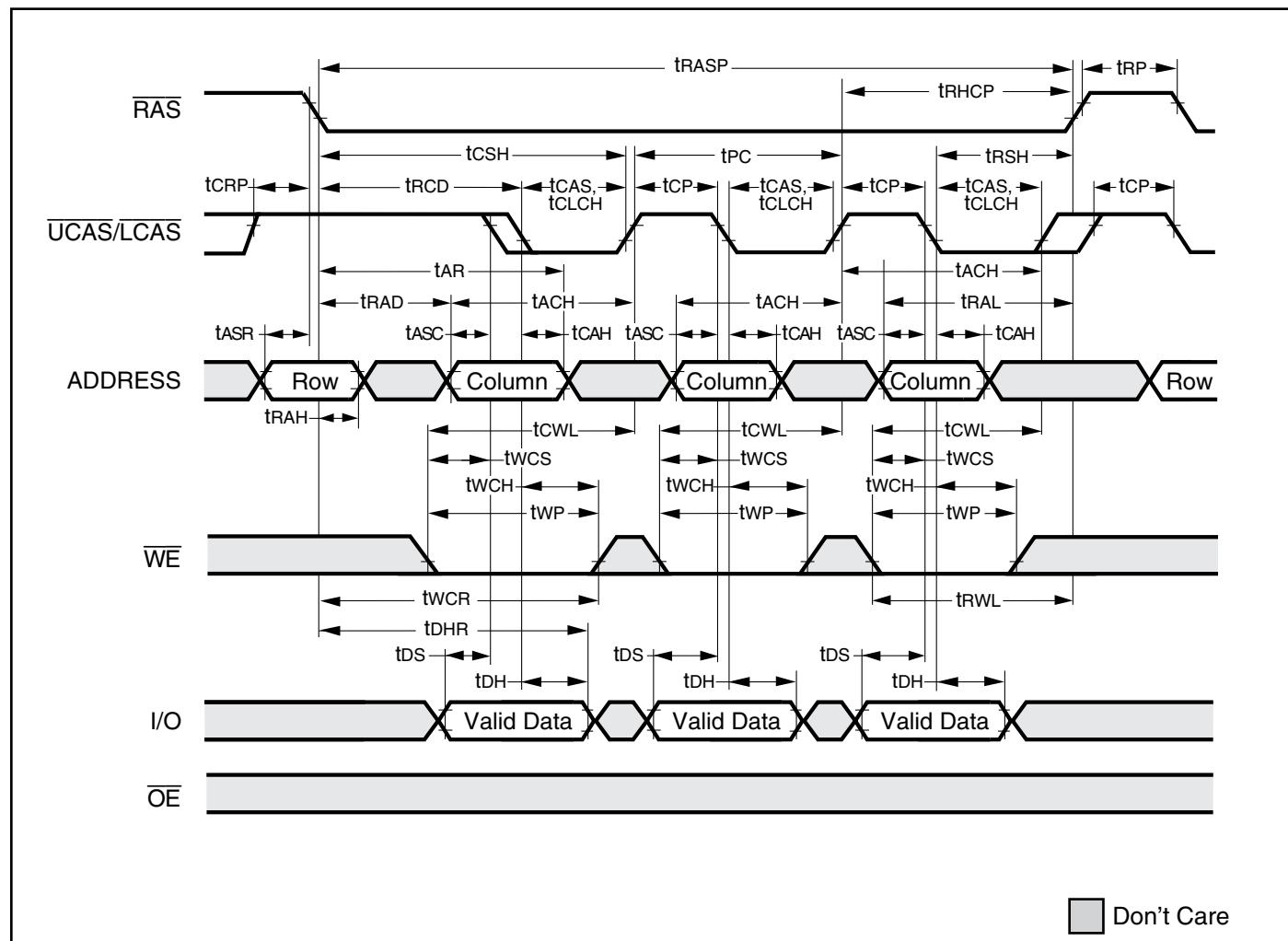
EDO-PAGE-MODE READ CYCLE

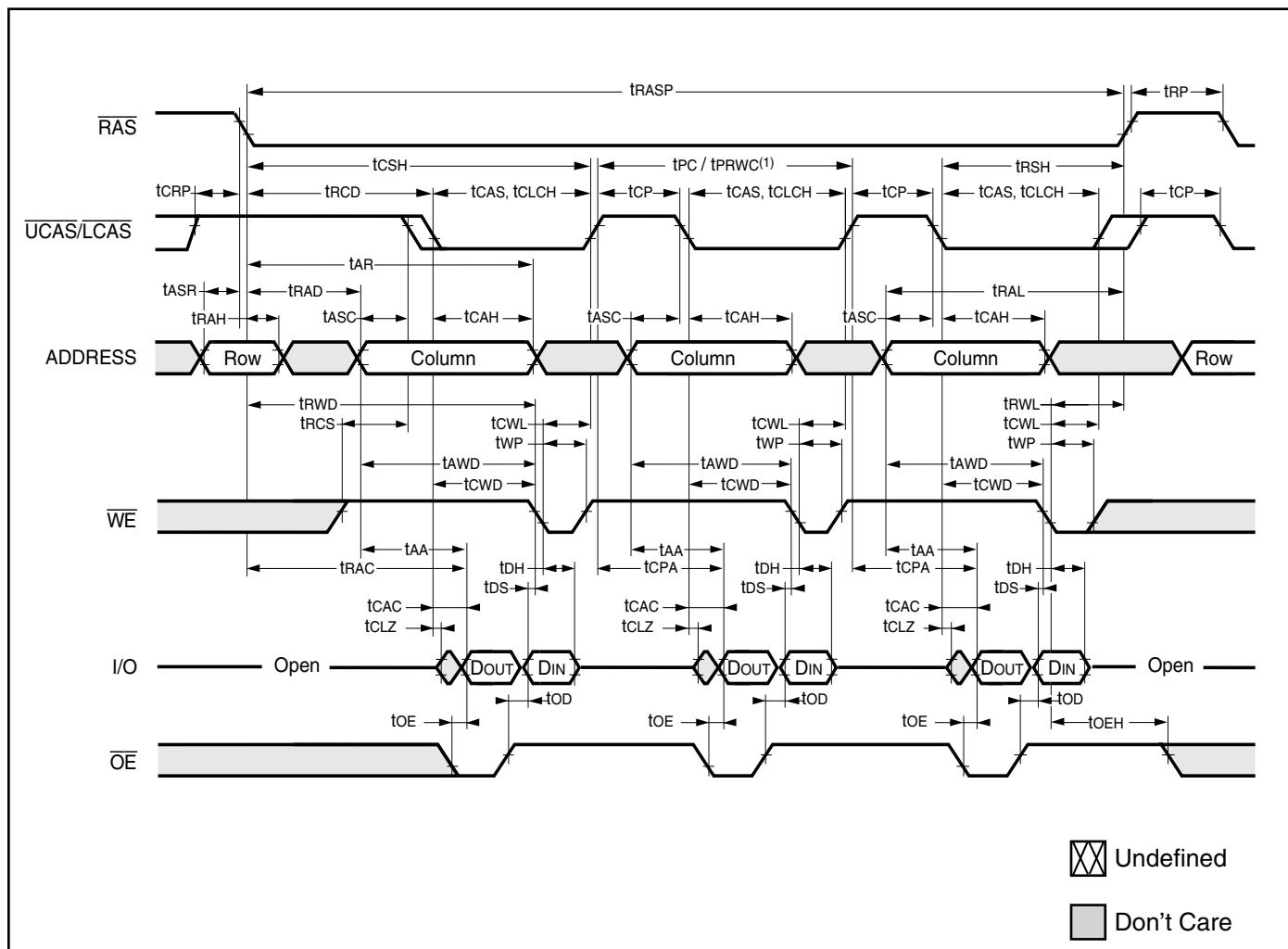


Note:

1. t_{PC} can be measured from falling edge of \overline{CAS} to falling edge of \overline{CAS} , or from rising edge of \overline{CAS} to rising edge of \overline{CAS} . Both measurements must meet the t_{PC} specifications.

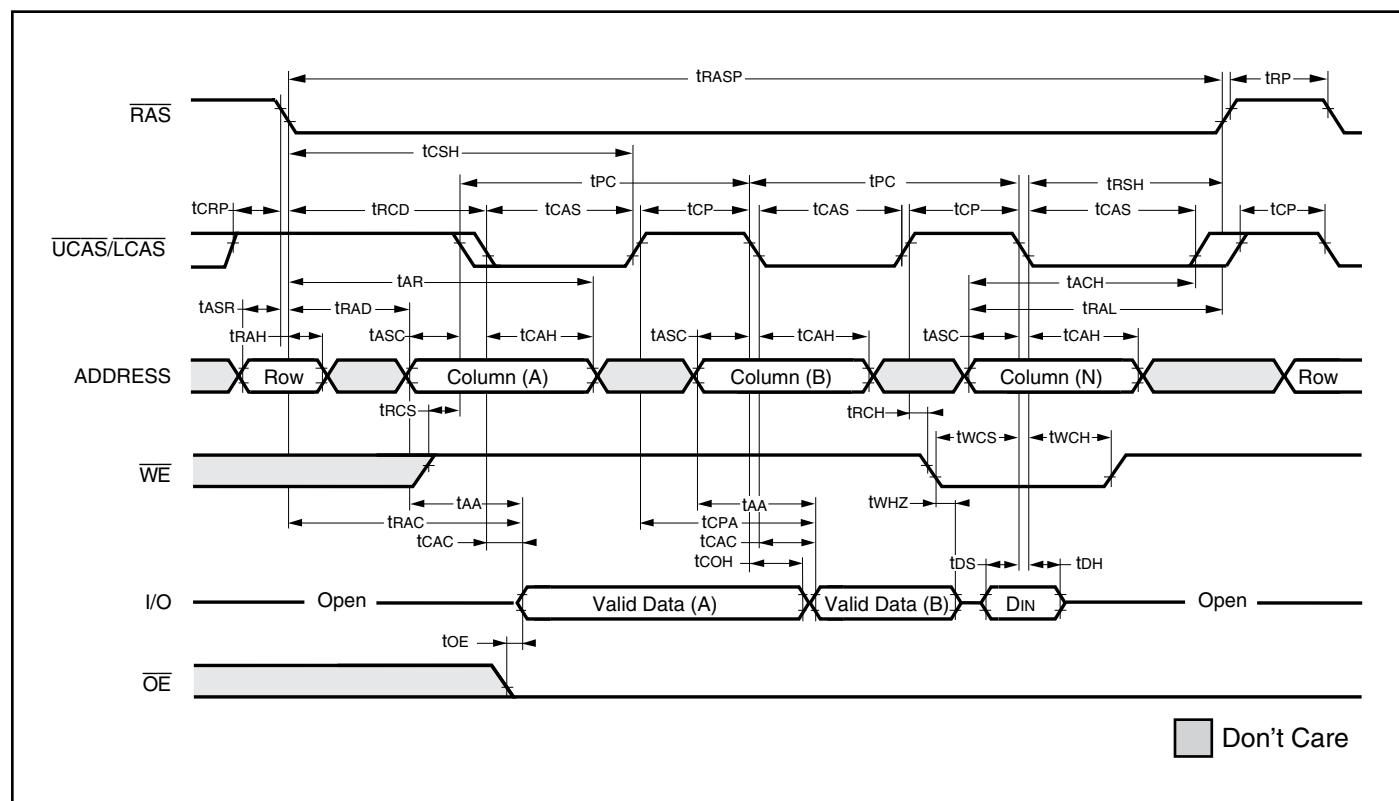
EDO-PAGE-MODE EARLY-WRITE CYCLE



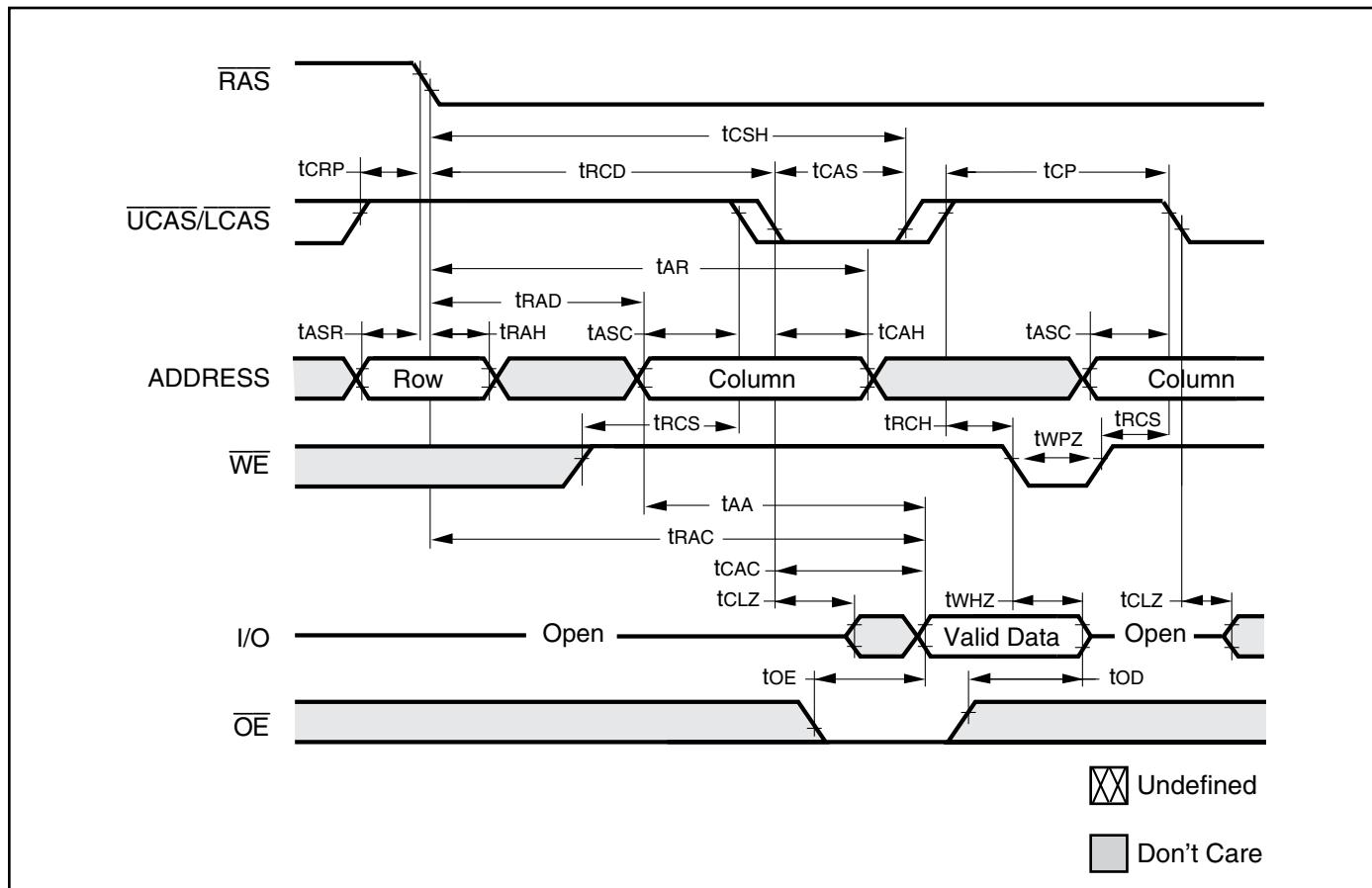
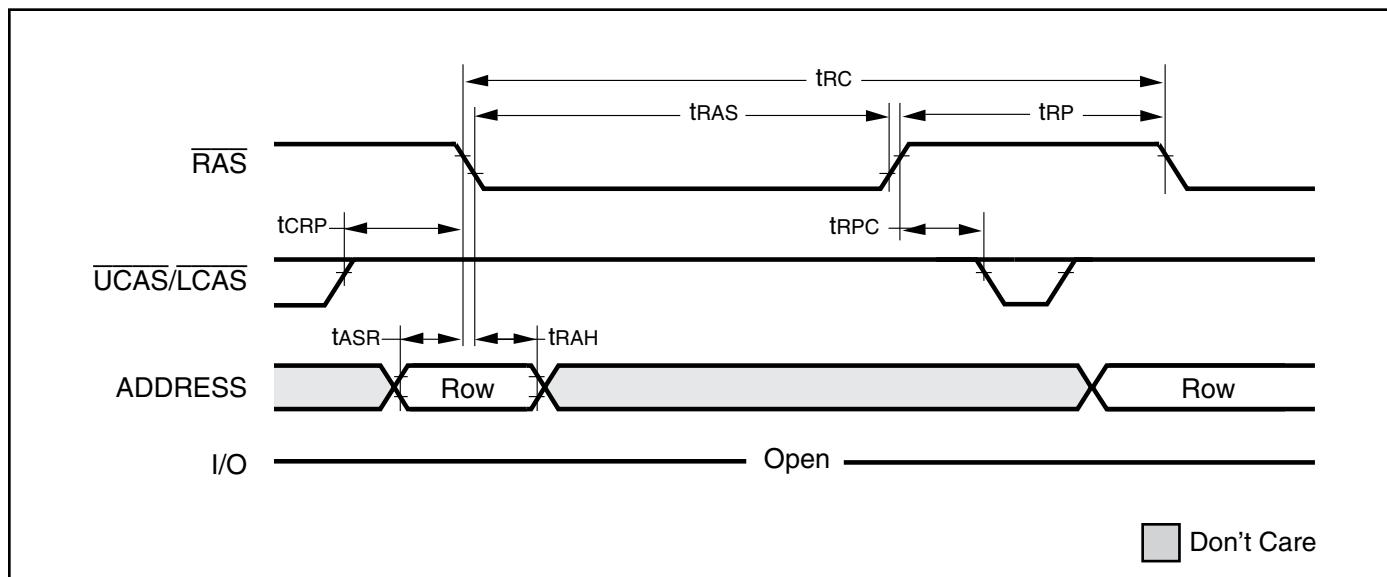
EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)

Note:

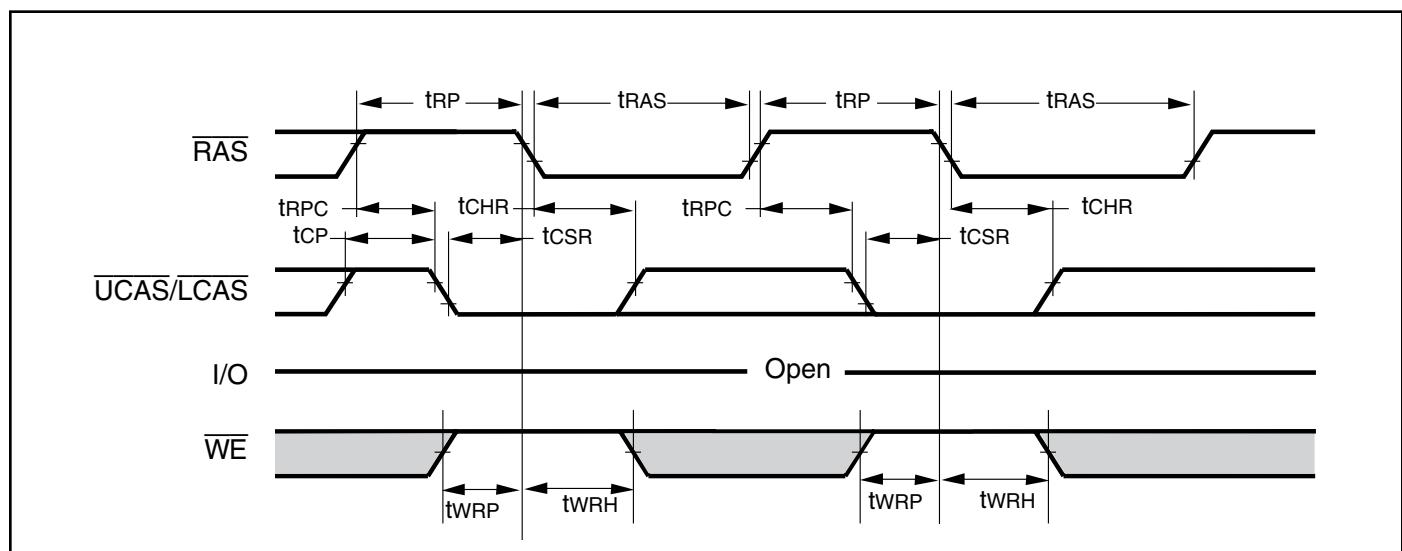
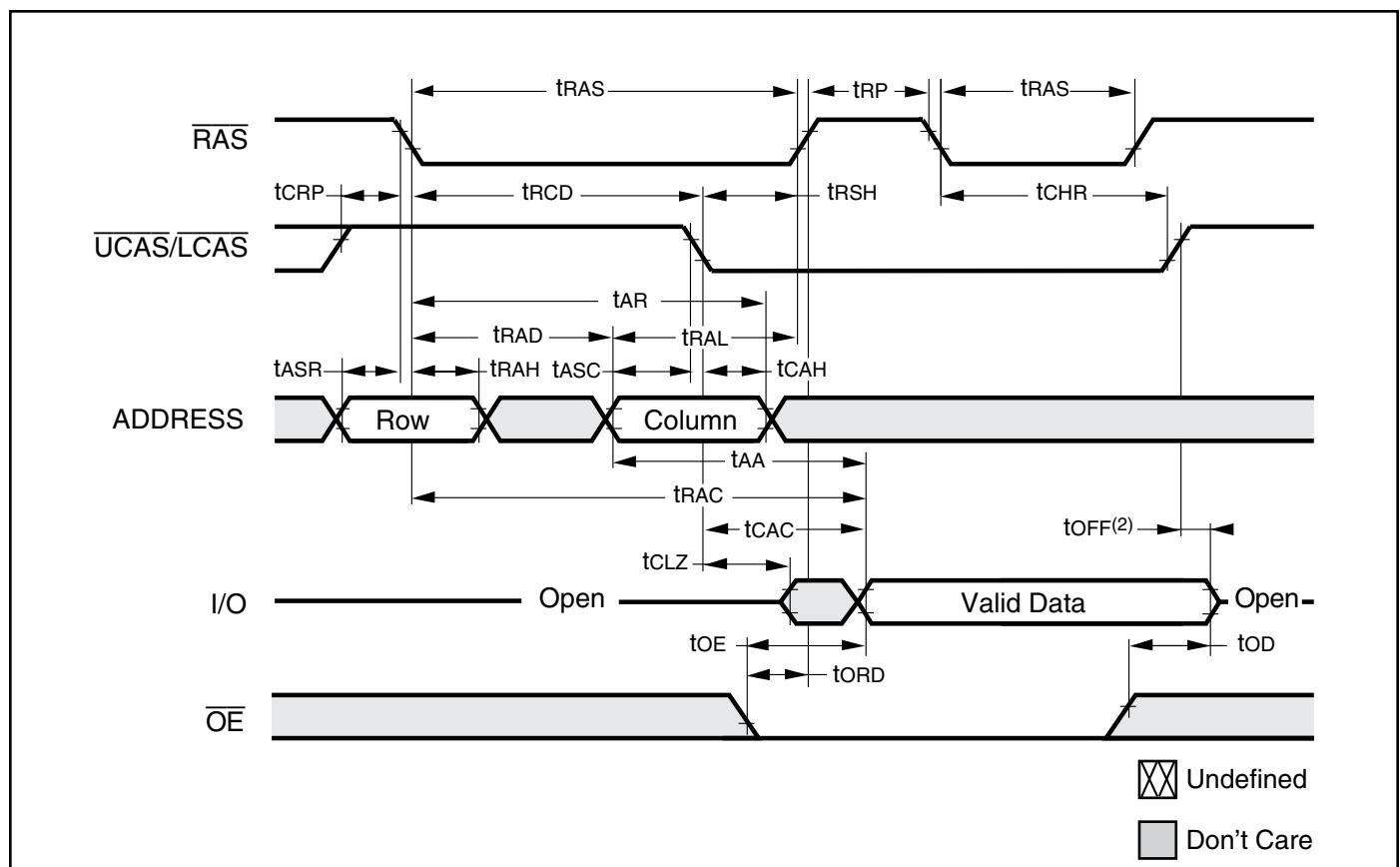
1. tPC can be measured from falling edge of \overline{CAS} to falling edge of \overline{CAS} , or from rising edge of \overline{CAS} to rising edge of \overline{CAS} . Both measurements must meet the tPC specifications.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY WRITE)



AC WAVEFORMS

READ CYCLE (With \overline{WE} -Controlled Disable)RAS-ONLY REFRESH CYCLE (\overline{OE} , \overline{WE} = DON'T CARE)

CBR REFRESH CYCLE (Addresses; \overline{OE} = DON'T CARE)HIDDEN REFRESH CYCLE⁽¹⁾ (\overline{WE} = HIGH; \overline{OE} = LOW)

Notes:

1. A Hidden Refresh may also be performed after a Write Cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
2. tOFF is referenced from rising edge of RAS or CAS, whichever occurs last.

IS41LV16100D

ORDERING INFORMATION :

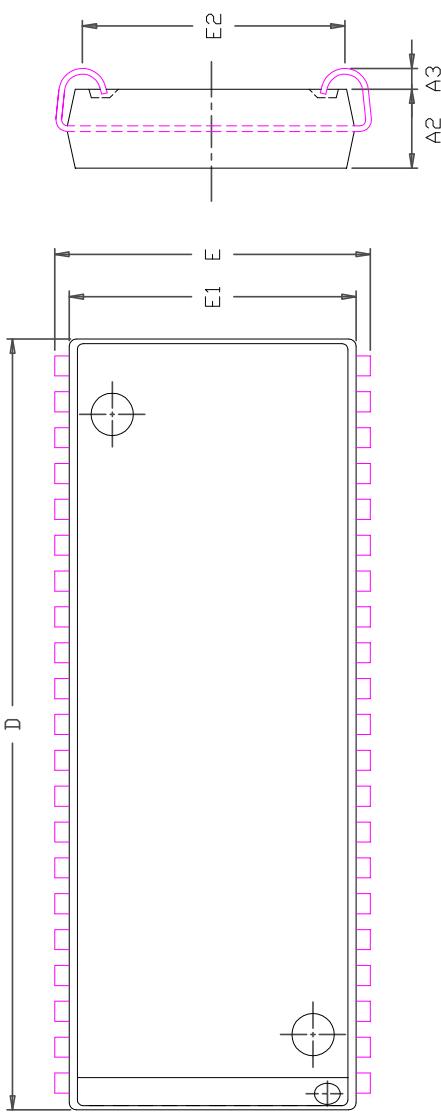
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
50	IS41LV16100D-50KI	400-mil SOJ
	IS41LV16100D-50KLI	400-mil SOJ, Lead-free
	IS41LV16100D-50TI	400-mil TSOP (Type II)
	IS41LV16100D-50TLI	400-mil TSOP (Type II), Lead-free

Note:

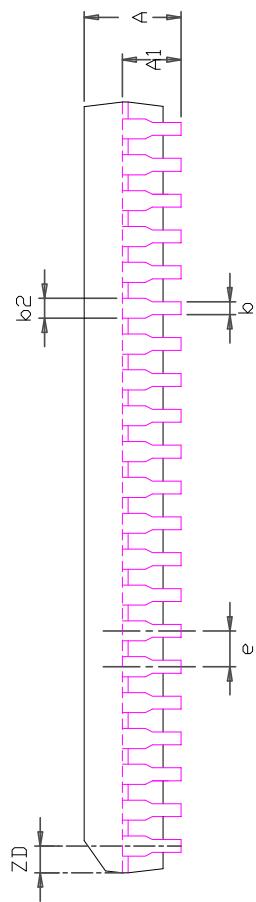
The -50 speed option supports 50ns and 60ns timing specifications.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	3.76	0.128	0.1148		
A1	2.08	2.70	0.082	0.106		
A2	2.61	2.92	0.103	0.115		
A3	0.64	0.84	0.025	0.033		
b	0.38	0.51	0.015	0.020		
b2	0.66	0.81	0.026	0.032		
D	27.18	27.43	1.070	1.080		
E	11.03	11.18	11.33	0.434	0.440	0.446
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.14	9.65	0.360	0.380		
e	1.27	BSC.		0.050	BSC.	
ZD	0.95	REF.		0.037	REF.	



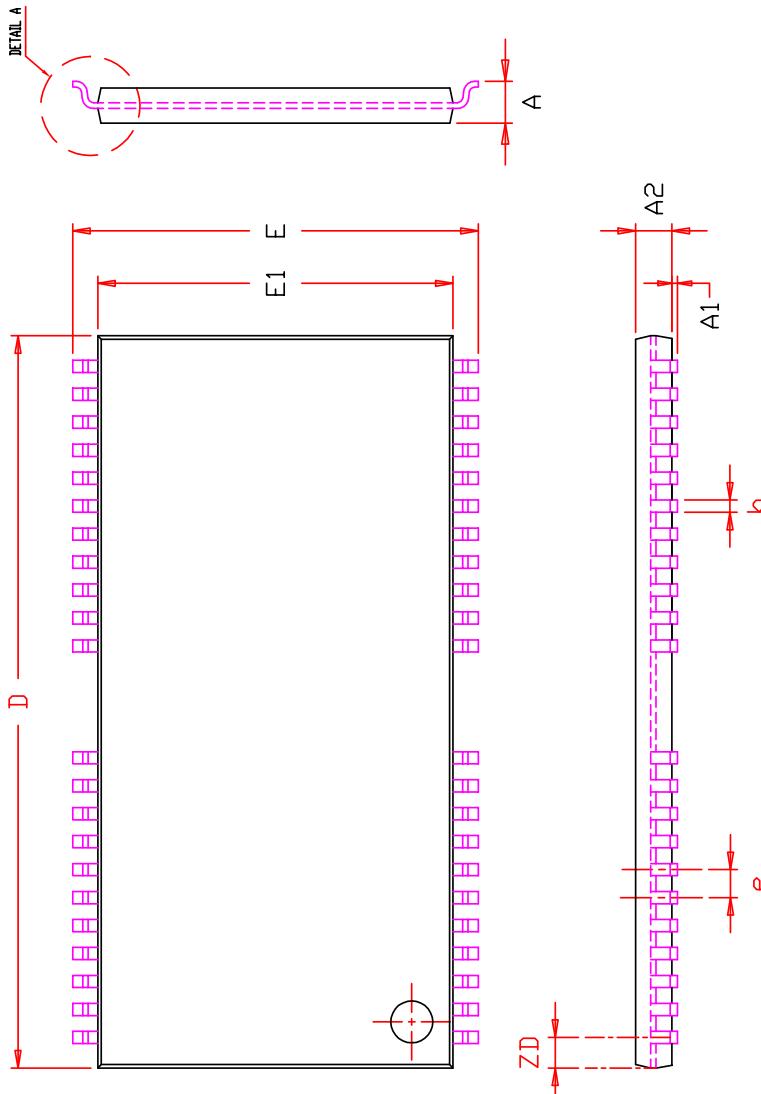
NOTE :

1. CONTROLLING DIMENSION: MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



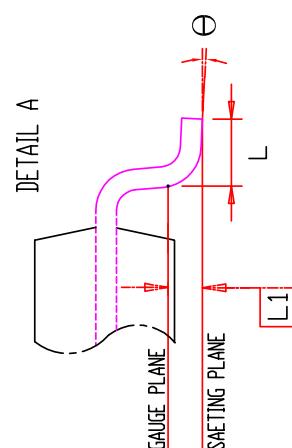
ISSI	TITLE	42L 400mil SOJ Package Outline	REV.	C	DATE	03/19/2009
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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN. NOM.	MAX.	MIN. NOM.	MAX.	MIN. NOM.	MAX.
A	1.00	1.20	0.039	0.047		
A1	0.05	0.15	0.002	0.006		
A2	0.95	1.00	0.05	0.037	0.039	0.041
b	0.30	0.45	0.012	0.018		
D	20.82	20.95	21.08	0.8220	0.825	0.830
E	11.56	11.76	11.96	0.4550	0.4630	0.471
E1	10.03	10.16	10.29	0.3950	0.4000	0.405
e	0.80	BSC.	0.031	BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25	BSC.	0.010	BSC.		
ZD	0.875	REF.	0.034	REF.		
Θ	0		8°	0		8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



	TITLE	44/50L 400mil TSOP-2	REV.	E	DATE	03/19/2009
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