

|               |                                                                                                                                                                               |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STRUCTURE     | Silicon monolithic integrated circuits                                                                                                                                        |
| PRODUCTSERIES | 3-phase brushless motor driver                                                                                                                                                |
| TYPE          | <b>BD67922EFV</b>                                                                                                                                                             |
| FUNCTION      | <ul style="list-style-type: none"> <li>• 3-phase MOS direct PWM driver</li> <li>• Built-in PLL control circuit</li> <li>• Built-in over current protection circuit</li> </ul> |

## ○Absolute maximum ratings (Ta=25°C)

| Item                                   | Symbol              | Limit              | Unit |
|----------------------------------------|---------------------|--------------------|------|
| Supply voltage                         | V <sub>CC</sub>     | -0.2~+36.0         | V    |
| LD, FG applied voltage                 | V <sub>LD, FG</sub> | -0.2~+6.5          | V    |
| HB applied voltage                     | V <sub>HB</sub>     | -0.2~+6.5          | V    |
| Hall signal input voltage              | V <sub>HALL</sub>   | -0.2~+6.5          | V    |
| Input voltage for CLK pin              | V <sub>CLK</sub>    | -0.2~+6.5          | V    |
| Input voltage for control pin (SS, SB) | V <sub>IN</sub>     | -0.2~+6.5          | V    |
| Power dissipation                      | Pd                  | 1.45 <sup>※1</sup> | W    |
|                                        |                     | 4.70 <sup>※2</sup> | W    |
| Output current                         | I <sub>OUT</sub>    | 2300 <sup>※3</sup> | mA   |
| Operating temperature range            | T <sub>opr</sub>    | -25~+85            | °C   |
| Storage temperature range              | T <sub>stg</sub>    | -55~+150           | °C   |
| Junction temperature                   | T <sub>jmax</sub>   | +150               | °C   |

※1 70mm × 70mm × 1.6mm glass epoxy board. Derating in done at 11.6mW/°C for operating above Ta=25°C.

※2 4-layer recommended board. Derating in done at 37.6mW/°C for operating above Ta=25°C.

※3 Do not, however exceed Pd, ASO, and T<sub>jmax</sub>=150°C.

## ○Recommend operating conditions (Ta= -25~+85°C)

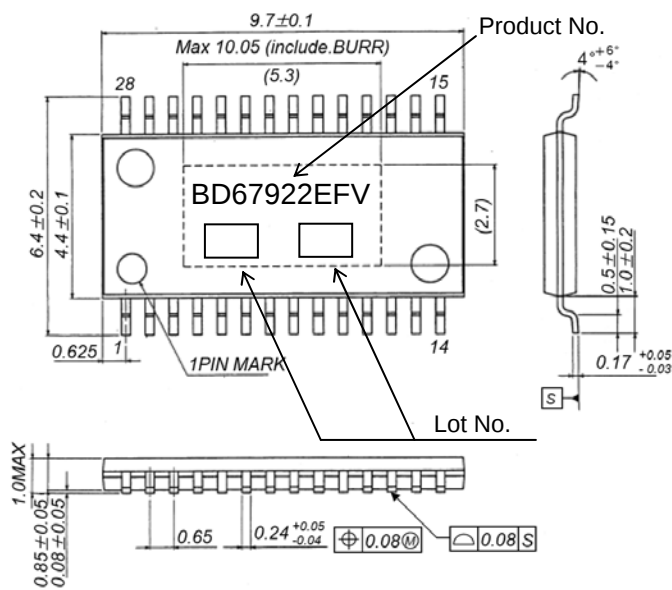
| Item                               | Symbol              | Min. | Typ. | Max. | Unit |
|------------------------------------|---------------------|------|------|------|------|
| Supply voltage                     | V <sub>CC</sub>     | 19   | 24   | 28   | V    |
| 5V constant voltage output current | I <sub>REG</sub>    | -20  | -    | 0    | mA   |
| HB pin current                     | I <sub>HB</sub>     | 0    | -    | 20   | mA   |
| LD, FG pin supply voltage          | V <sub>LD, FG</sub> | 0    | -    | 5.5  | V    |
| LD, FG pin current                 | I <sub>LD, FG</sub> | 0    | -    | 15   | mA   |

This product isn't designed for protection against radioactive rays.

○Electrical characteristics (Unless otherwise specified, Ta=25°C, V<sub>CC</sub>=24V)

| Item                                                 | Symbol            | Limit |      |      | Unit  | Conditions                                       |
|------------------------------------------------------|-------------------|-------|------|------|-------|--------------------------------------------------|
|                                                      |                   | Min.  | Typ. | Max. |       |                                                  |
| Whole                                                |                   |       |      |      |       |                                                  |
| Circuit current 1                                    | I <sub>CC1</sub>  | -     | 4.0  | 9.0  | mA    | SS=L output ON mode                              |
| Circuit current 2                                    | I <sub>CC2</sub>  | -     | 1.5  | 2.3  | mA    | SS=H output OFF mode                             |
| VREG output                                          |                   |       |      |      |       |                                                  |
| Output voltage                                       | V <sub>REG</sub>  | 4.65  | 5.00 | 5.35 | V     |                                                  |
| Output (U, V, W)                                     |                   |       |      |      |       |                                                  |
| Output on resistance                                 | R <sub>ON</sub>   | -     | 1.35 | 1.76 | Ω     | I <sub>OUT</sub> =1.0A<br>Sum of upper and lower |
| Lower side diode forward voltage                     | V <sub>D1</sub>   | 0.70  | 1.10 | 1.55 | V     | I <sub>OUT</sub> =-1.0A                          |
| Upper side diode forward voltage                     | V <sub>D2</sub>   | 0.70  | 1.10 | 1.55 | V     | I <sub>OUT</sub> =1.0A                           |
| Output leak current                                  | I <sub>LEAK</sub> | -     | -    | 10   | μA    |                                                  |
| Hall comparator Input (HUP, HUN, HVP, HVN, HWP, HWN) |                   |       |      |      |       |                                                  |
| Common mode input voltage range                      | V <sub>ICM</sub>  | 1.5   | -    | 3.5  | V     |                                                  |
| Hysteresis width                                     | ΔV <sub>IN</sub>  | 15    | 24   | 42   | mV    | Sum of upper and lower                           |
| LD, FG output                                        |                   |       |      |      |       |                                                  |
| Low level output voltage                             | V <sub>OD</sub>   | -     | 0.15 | 0.50 | V     | I <sub>LD, FG</sub> =10mA                        |
| PD output                                            |                   |       |      |      |       |                                                  |
| High level output voltage                            | V <sub>PDH</sub>  | 4.5   | 4.9  | -    | V     | I <sub>PD</sub> =-100 μA                         |
| Low level output voltage                             | V <sub>PDL</sub>  | -     | 0.2  | 0.3  | V     | I <sub>PD</sub> =100 μA                          |
| Integral amplifier                                   |                   |       |      |      |       |                                                  |
| EO High level output voltage                         | V <sub>EOH</sub>  | 3.5   | 4.1  | -    | V     | I <sub>EO</sub> =-500 μA                         |
| EO Low level output voltage                          | V <sub>EOL</sub>  | -     | 0.9  | 1.5  | V     | I <sub>EO</sub> =500 μA                          |
| EI input current                                     | I <sub>EI</sub>   | -2.0  | -0.1 | -    | μA    | V <sub>EI</sub> =0V                              |
| Current limit circuit                                |                   |       |      |      |       |                                                  |
| Drive gain during starting mode                      | G <sub>H</sub>    | 1.2   | 1.5  | 1.8  | times |                                                  |
| Drive gain during steady mode                        | G <sub>L</sub>    | 0.4   | 0.5  | 0.6  | times |                                                  |
| Limiter voltage                                      | V <sub>CL</sub>   | 0.45  | 0.50 | 0.55 | V     |                                                  |
| CLK input                                            |                   |       |      |      |       |                                                  |
| External input frequency                             | F <sub>CLK</sub>  | -     | -    | 10   | kHz   |                                                  |
| High level input voltage                             | V <sub>CLKH</sub> | 3.0   | -    | -    | V     |                                                  |
| Low level input voltage                              | V <sub>CLKL</sub> | -     | -    | 1.5  | V     |                                                  |
| Low level input current                              | I <sub>CLKL</sub> | -75   | -50  | -25  | μA    | V <sub>CLK</sub> =0V                             |
| Control input (SS, SB)                               |                   |       |      |      |       |                                                  |
| High level input voltage                             | V <sub>INH</sub>  | 3.0   | -    | -    | V     |                                                  |
| Low level input voltage                              | V <sub>INL</sub>  | -     | -    | 1.5  | V     |                                                  |
| Low level input current                              | I <sub>INL</sub>  | -75   | -50  | -25  | μA    | V <sub>IN</sub> =0V                              |
| OSC                                                  |                   |       |      |      |       |                                                  |
| OSC oscillating frequency                            | F <sub>OSC</sub>  | 130   | 200  | 270  | kHz   | C <sub>OSC</sub> =220pF                          |
| OSC High voltage                                     | V <sub>OSCH</sub> | 1.6   | 2.0  | 2.4  | V     |                                                  |
| OSC Low voltage                                      | V <sub>OSCL</sub> | 1.2   | 1.5  | 1.8  | V     |                                                  |
| PROCLK                                               |                   |       |      |      |       |                                                  |
| CLK cycle for protection circuit                     | T <sub>PCLK</sub> | 13    | 20   | 27   | msec  | C <sub>PCLK</sub> =0.1 μF                        |
| Hall bias                                            |                   |       |      |      |       |                                                  |
| Hall bias voltage                                    | V <sub>HR</sub>   | 0.70  | 0.85 | 1.00 | V     | I <sub>HR</sub> =10mA                            |

OPackage outline

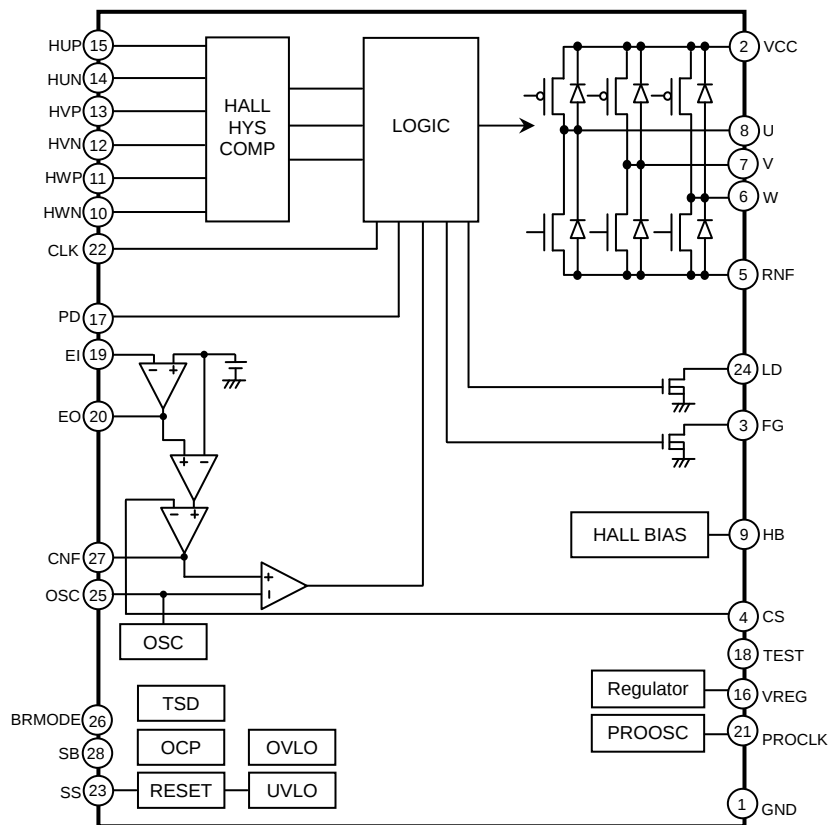


HTSSOP-B28 (Unit: mm)

OPin No. / Pin name

| Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|
| 1       | GND      | 15      | HUP      |
| 2       | VCC      | 16      | VREG     |
| 3       | FG       | 17      | PD       |
| 4       | CS       | 18      | TEST     |
| 5       | RNF      | 19      | EI       |
| 6       | W        | 20      | EO       |
| 7       | V        | 21      | PROCLK   |
| 8       | U        | 22      | CLK      |
| 9       | HB       | 23      | SS       |
| 10      | HWN      | 24      | LD       |
| 11      | HWP      | 25      | OSC      |
| 12      | HVN      | 26      | BRMODE   |
| 13      | HVP      | 27      | CNF      |
| 14      | HUN      | 28      | SB       |

OBlock diagram



## ○Operation Notes

- (1) Absolute maximum ratings  
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
- (2) Power supply lines  
As return of current regenerated by back EMF of motor happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.
- (3) GND potential  
The potential of GND pin must be minimum potential in all operating conditions.
- (4) Metal on the backside (Define the side where product markings are printed as front)  
The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that there is a possibility of malfunction or destruction if it is shorted with any potential other than GND.
- (5) Thermal design  
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.
- (6) Actions in strong electromagnetic field  
The IC is not designed for using in the presence of strong electromagnetic field. Be sure to confirm that no malfunction is found when using the IC in a strong electromagnetic field.
- (7) ASO  
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.
- (8) Thermal shutdown circuit  
The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes  $T_{jmax}=150^{\circ}\text{C}$ , and higher, coil output to the motor will be open. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.
- (9) Ground Wiring Pattern  
When using both large current and small signal GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
- (10) Mounting errors and Inter-pin short  
When attaching to a printed circuit board, pay attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short-circuits which can be caused by foreign matter entering between pins.
- (11) TEST pin  
Be sure to connect TEST pin to GND.

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