

HD74AC164/HD74ACT164

Serial-In, Parallel-Out Shift Register

REJ03D0253-0200Z
(Previous ADE-205-373 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC164/HD74ACT164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the Low-to-High transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs Low independent of the clock.

Features

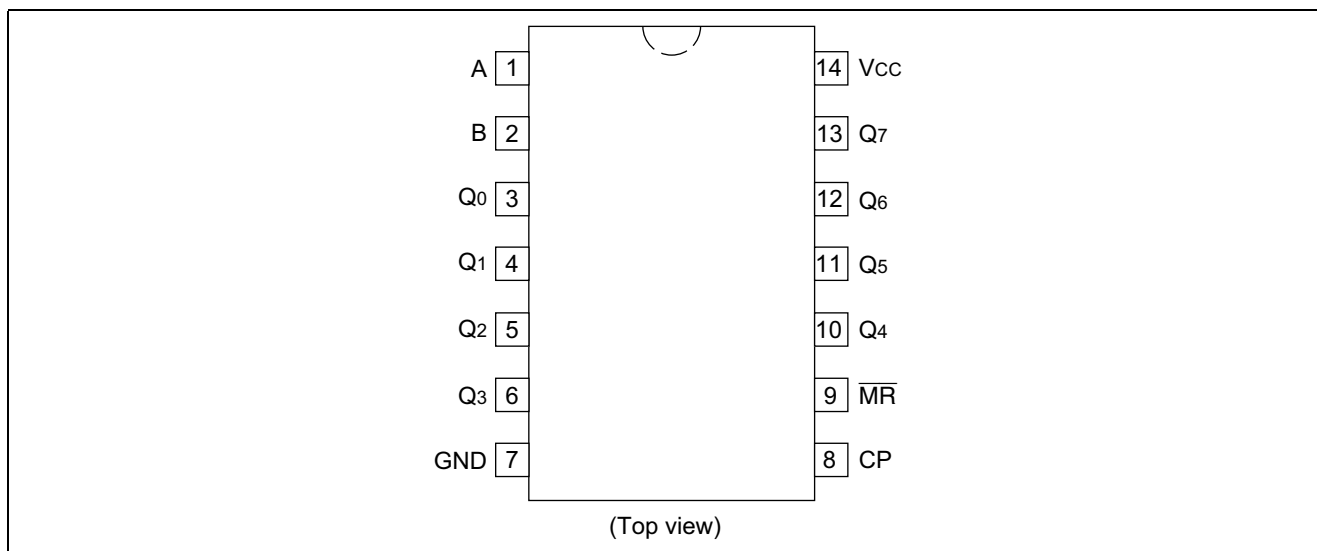
- Outputs Source/Sink 24 mA
- HD74ACT164 has TTL-Compatible Inputs
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC164P	DIP-14 pin	DP-14, -14AV	P	—
HD74AC164FPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74AC164RPEL	SOP-14 pin (JEDEC)	FP-14DNV	RP	EL (2,500 pcs/reel)
HD74AC164TELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

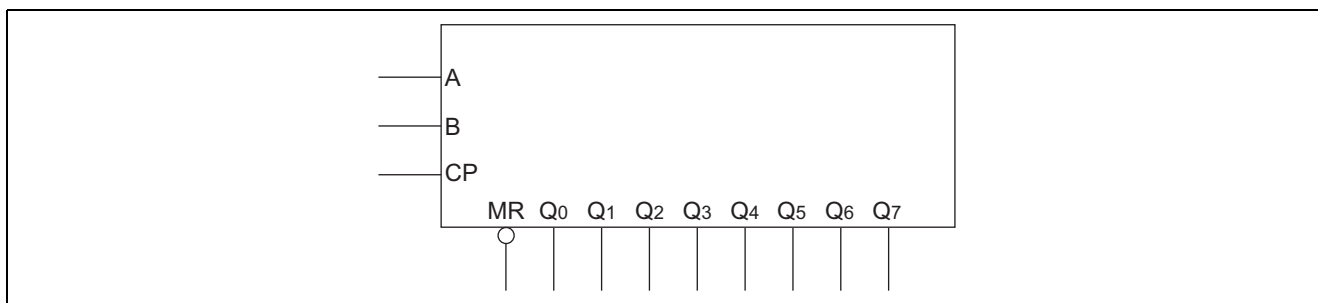
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

A, B	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{\text{MR}}$	Master Reset Input (Active Low)
Q_0 to Q_7	Outputs

Functional Description

The HD74AC164/HD74ACT164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other inputs. An unused input must be tied High.

Each Low-to-High transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs ($A \cdot B$) that existed before the rising clock edge. A Low level on the Master Reset ($\overline{\text{MR}}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs Low.

Mode Select Table

Operating Mode	Inputs			Outputs	
	$\overline{\text{MR}}$	A	B	Q_0	Q_1 to Q_7
Reset (Clear)	L	X	X	L	L to L
Shift	H	L	L	L	q_0 to q_6
	H	L	H	L	q_0 to q_6
	H	H	L	L	q_0 to q_6
	H	H	H	H	q_0 to q_6

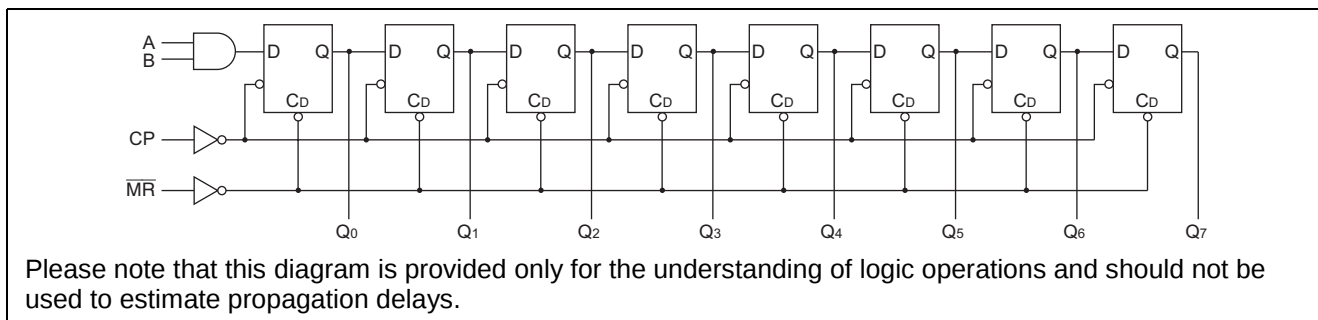
H : High Voltage Level

L : Low Voltage Level

X : Immaterial

q_n : Lower case letters indicate the state of the referenced input or output one setup time prior to the Low-to-High clock transition.

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	T_{stg}	-65 to +150	°C	

Recommended Operating Conditions: HD74AC164

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	t_r, t_f	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5V$
				$V_{CC} = 5.5V$

DC Characteristics: HD74AC164

Item	Sym- bol	V_{CC} (V)	$T_a = 25^\circ C$			$T_a = -40 \text{ to } +85^\circ C$		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	$V_{OUT} = 0.1V \text{ or } V_{CC} - 0.1V$	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		$V_{OUT} = 0.1V \text{ or } V_{CC} - 0.1V$	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OUT} = -50 \mu A$	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—			
		4.5	3.94	—	—	3.80	—			
		5.5	4.94	—	—	4.80	—			
	V_{OL}	3.0	—	0.002	0.1	—	0.1		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OUT} = 50 \mu A$	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37			
		4.5	—	—	0.32	—	0.37		$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 12 \text{ mA}$
		5.5	—	—	0.32	—	0.37			$I_{OL} = 24 \text{ mA}$
										$I_{OL} = 24 \text{ mA}$
Input leakage current	I_{IN}	5.5	—	—	± 0.1	—	± 1.0	μA	$V_{IN} = V_{CC} \text{ or } GND$	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	$V_{OLD} = 1.1V$	
	I_{OHD}	5.5	—	—	—	-75	—	mA	$V_{OHD} = 3.85V$	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	μA	$V_{IN} = V_{CC} \text{ or } \text{ground}$	

*Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions: HD74ACT164

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 0.8 to 2.0 V	t_r, t_f	8	ns/V	$V_{CC} = 4.5V$ $V_{CC} = 5.5V$

DC Characteristics: HD74ACT164

Item	Sym- bol	V_{CC} (V)	$T_a = 25^\circ C$			$T_a = -40 \text{ to } +85^\circ C$		Unit	Condition
			min.	typ.	max.	min.	max.		
Input voltage	V_{IH}	4.5	2.0	1.5	—	2.0	—	V	$V_{OUT} = 0.1 \text{ V or } V_{CC}-0.1 \text{ V}$
		5.5	2.0	1.5	—	2.0	—		
	V_{IL}	4.5	—	1.5	0.8	—	0.8		$V_{OUT} = 0.1 \text{ V or } V_{CC}-0.1 \text{ V}$
		5.5	—	1.5	0.8	—	0.8		
Output voltage	V_{OH}	4.5	4.4	4.49	—	4.4	—	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OUT} = -50 \mu A$
		5.5	5.4	5.49	—	5.4	—		
		4.5	3.94	—	—	3.80	—		$V_{IN} = V_{IL}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.94	—	—	4.80	—		$I_{OH} = -24 \text{ mA}$
	V_{OL}	4.5	—	0.001	0.1	—	0.1		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OUT} = 50 \mu A$
		5.5	—	0.001	0.1	—	0.1		
		4.5	—	—	0.32	—	0.37		$V_{IN} = V_{IL}$ $I_{OL} = 24 \text{ mA}$
		5.5	—	—	0.32	—	0.37		$I_{OL} = 24 \text{ mA}$
Input current	I_{IN}	5.5	—	—	± 0.1	—	± 1.0	μA	$V_{IN} = V_{CC} \text{ or GND}$
I_{CC} /input current	I_{CCT}	5.5	—	0.6	—	—	1.5	mA	$V_{IN} = V_{CC}-2.1 \text{ V}$
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	$V_{OLD} = 1.1 \text{ V}$
	I_{OHD}	5.5	—	—	—	-75	—	mA	$V_{OHD} = 3.85 \text{ V}$
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	μA	$V_{IN} = V_{CC} \text{ or ground}$

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC164

Item	Symbol	$V_{CC} \text{ (V)}^{*1}$	$T_a = +25^\circ C$ $C_L = 50 \text{ pF}$			$T_a = -40^\circ C \text{ to } +85^\circ C$ $C_L = 50 \text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	125	—	—	100	—	MHz
		5.0	150	—	—	125	—	
Propagation delay CP to Q_n	t_{PLH}	3.3	1.0	8.5	13.0	1.0	13.5	ns
		5.0	1.0	6.5	10.0	1.0	10.5	
Propagation delay CP to Q_n	t_{PHL}	3.3	1.0	8.5	13.0	1.0	14.5	
		5.0	1.0	6.5	10.0	1.0	10.5	
Propagation delay MR to Q_n	t_{PHL}	3.3	1.0	9.5	16.0	1.0	18.0	
		5.0	1.0	7.5	11.5	1.0	13.5	

Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

AC Operating Requirements: HD74AC164

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = −40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time A or B to CP	t _{su}	3.3	3.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	
Hold time CP to A or B	t _h	3.3	−1.5	0.0	0.0	
		5.0	−1.5	0.0	0.0	
Pulse width CP or $\overline{MR}$	t _w	3.3	2.0	5.5	7.0	
		5.0	2.0	4.5	5.0	
Recovery time $\overline{MR}$ or CP	t _{rec}	3.3	0.0	2.0	2.0	
		5.0	0.0	2.0	2.0	

Note: 1. Voltage Range 3.3 is 3.3 V $\pm$ 0.3 V
Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

AC Characteristics: HD74ACT164

Item	Symbol	$V_{CC} (V)^{*1}$	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay CP to Q _n	t_{PLH}	5.0	1.0	9.0	11.5	1.0	12.5	ns
Propagation delay CP to Q _n	t_{PHL}	5.0	1.0	9.0	11.5	1.0	12.5	
Propagation delay $\overline{MR}$ to Q _n	t_{PHL}	5.0	1.0	9.5	13.0	1.0	14.5	

Note: 1. Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

AC Operating Requirements: HD74AC164

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = −40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time A or B to CP	t _{SU}	5.0	2.5	7.0	8.0	ns
Hold time CP to A or B	t _H	5.0	0.0	1.5	1.5	
Pulse width CP or MR	t _W	5.0	4.5	7.0	8.0	
Recovery time MR or CP	t _{REC}	5.0	0.0	2.0	2.0	

Note: 1. Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

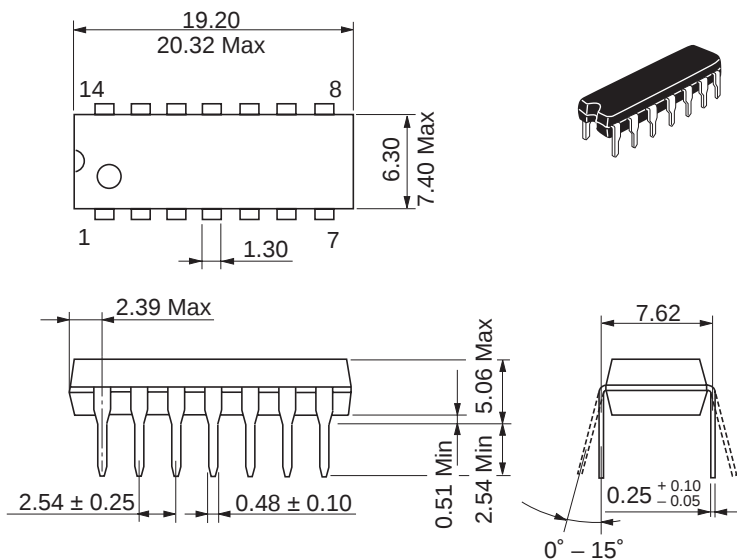
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	20.0	pF	V _{CC} = 5.0 V

Package Dimensions

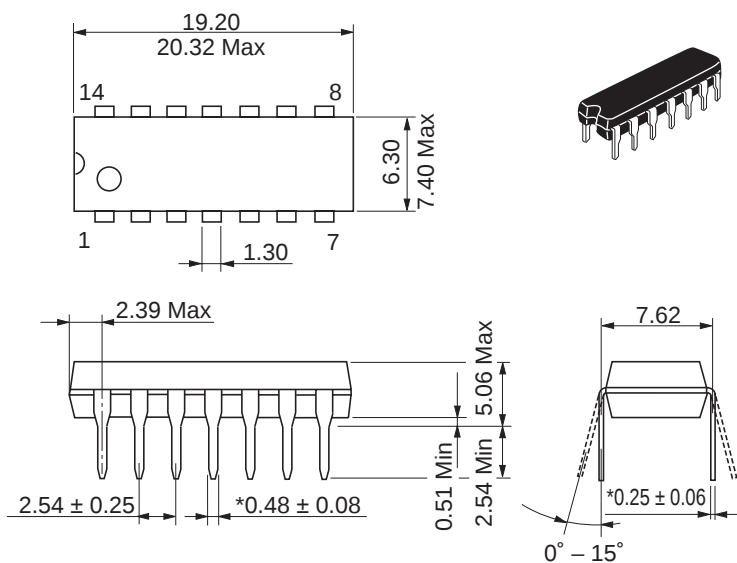
As of January, 2003

Unit: mm



Package Code	DP-14
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.97 g

Unit: mm

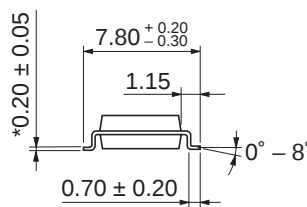
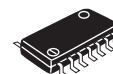
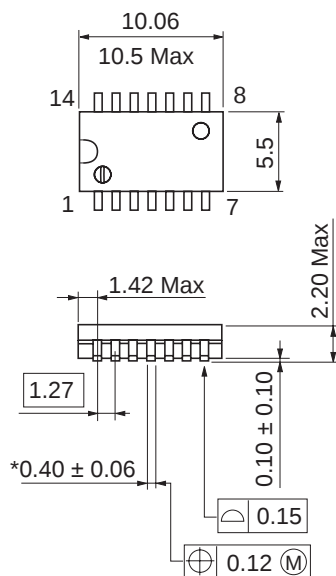


*Ni/Pd/AU Plating

Package Code	DP-14AV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.97 g

As of January, 2003

Unit: mm

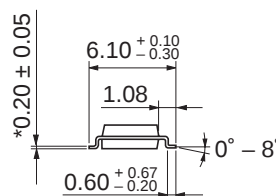
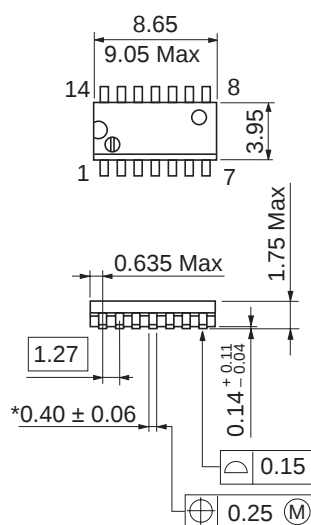


*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003

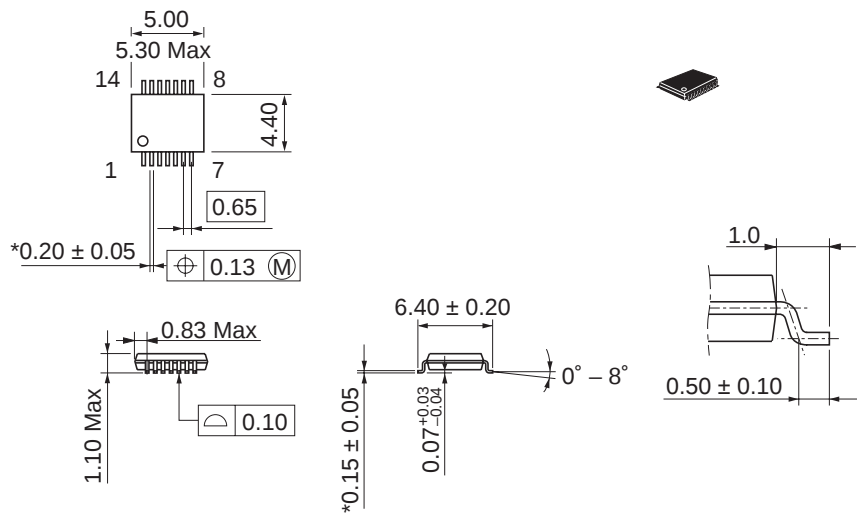
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-14DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.13 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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