Panasonic

AN26027A

Ultra small, Low NF, Single Band LNA-IC for 600 MHz Band Applications

FEATURES

- Low voltage operation +2.85 V typ.
- Low current consumption
  3 mA typ. (High-Gain mode)
  1 µA typ. (Low-Gain mode)
- High gain 15.0 dB typ. fRX = 620 MHz (High-Gain mode)
- Low noise figure
  1.20 dB typ. fRX = 620 MHz (High-Gain mode)
- Low distortion (IIP3 +10 MHz offset)
  –4.0 dBm typ. fRX = 620 MHz (High-Gain mode)
- 5 pin Wafer level chip size package (WLCSP)

DESCRIPTION

AN26027A is single band LNA-IC for 600 MHz Band applications.

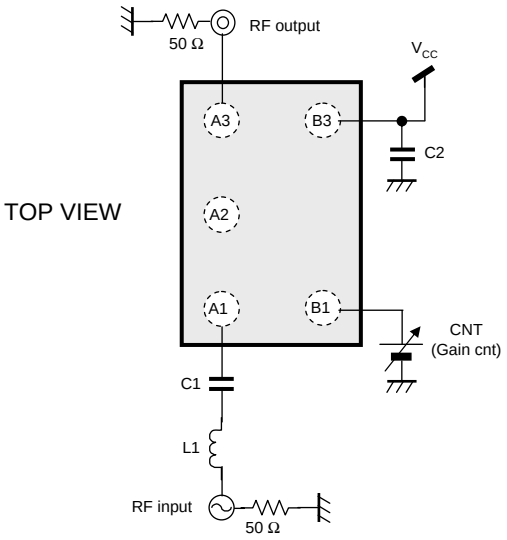
It realizes high performance by using 0.18 µm SiGeC Bi-CMOS process (f_T = 90 GHz, f_{max} = 140 GHz). High/Low Gain-mode is changeable, controlled by integrated CMOS logic circuit.

A WLCSP package (Wafer Level Chip Sized Package) achieves miniaturization.

APPLICATIONS

●DTV（UHF）

SIMPLIFIED APPLICATION



Components	Size	Value	Part Number	Vendor
L1	0603	8.2 nH	LQP03TN8N2H04	Murata
C1	0603	1 000 pF	GRM033B11C102KD01	Murata
C2	0603	100 000 pF	GRM33B30J104KE18	Murata

Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{CC}	3.6	V	*1
Supply current	I_{CC}	18	mA	—
Operating ambient temperature	T_{opr}	–25 to 75	°C	*2
Operating junction temperature	T_j	–40 to +125	°C	*2
Storage temperature	T_{stg}	–40 to +125	°C	*2
Input Voltage Range	IN (Pin No.A1)	—	V	*3
	CNT (Pin No.B1)	-0.3 to V_{CC}	V	—
	OUT (Pin No.A3)	—	V	*4
ESD	HBM (Human Body Model)	1	kV	—
	MM (Machine Model)	100	V	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2:Except for the operating ambient temperature, operating junction temperature, and storage temperature, all ratings are for Ta = 25°C.
*3:RF signal input pin. Do not apply DC.
*4:RF signal output pin. Do not apply DC.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	PD (Ta=25 °C)	PD (Ta=75 °C)
WLCSP	1391.0°C/W	0.072W	0.036W

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	V_{CC}	2.5	2.85	3.0	V	*1

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

ELECRTRICAL CHARACTERISTICS

Note) Vcc = 2.85 V, Ta = 25°C±2°C, unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC electrical characteristics							
Supply current HG	IccH	Vcc current at High-Gain mode No input signal	—	3.0	4.4	mA	—
Supply current LG	IccL	Vcc current at Low-Gain mode No input signal	—	1.0	10	µA	—
Switching voltage (High Gain Mode)	VIH	VIH = Vcc × 0.90	2.57	2.85	—	V	—
Switching voltage (Low Gain Mode)	VIL	VIL = Vcc × 0.14	—	0.0	0.4	V	—
Switching current(High)	IIH	Current at CNT pin VIH = Vcc	—	4.6	20	µA	—

ELECRTRICAL CHARACTERISTICS (continued)

Note) Vcc = 2.85 V, Ta= 25°C±2°C, fRXa = 620 MHz, PRX = –30 dBm, CW unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LNA AC electrical characteristics							
Power Gain HG	GHS	High-Gain mode	13.0	15.0	17.0	dB	—
Power Gain LG	GLS	Low-Gain mode PRX = –20 dBm	–7.5	–4.0	–1.0	dB	—
IIP3 +10 MHz offset HG	IIP3H1	High-Gain mode f1 = fRXa + 10 MHz f2 = fRXa + 20 MHz Input 2 signals (f1, f2)	–12	–4.0	—	dBm	—

APPLICATION INFORMATION

REFERENCE VALUES FOR DESIGN

Notes) Vcc = 2.85 V

Ta = 25°C±2°C, fRXb = 470 MHz, 620 MHz, 770 MHz, PRX = –30 dBm, CW unless otherwise specified.

Parameter		Symbol	Conditions	Reference values			Unit	Note
				Min	Typ	Max		
LNA AC electrical characteristics								
	Power Gain HG	GH	High-Gain mode	11.5	15.0	17.5	dB	*1
	Power GainLG	GL	Low-Gain mode PRX = –20 dBm	–8.0	–4.0	–1.0	dB	*1
	Noise Figure HG	NFH	High-Gain mode	—	1.3	2.3	dB	*1,*3
	Noise Figure LG	NFL	Low-Gain mode	—	6.5	8.5	dB	*1
	IIP3 +10 MHz offset HG	IIP3H1	High-Gain mode f1 = fRXb + 10 MHz f2 = fRXb + 20 MHz Input 2 signals (f1, f2)	–13	–4.0	—	dBm	*1
	IIP3 +10 MHz offset HG	IIP3H2	High-Gain mode f1 = fRXb – 10 MHz f2 = fRXb – 20 MHz Input 2 signals (f1, f2)	–13	–4.0	—	dBm	*1
	Input P1dB HG	IP1dBH	High-Gain mode	–10	–6	—	dBm	*1
	Reverse Isolation HG	ISOH	High-Gain mode	—	–24	—	dB	*2
	Reverse Isolation LG	ISOL	High-Gain mode	—	–3.5	—	dB	*2

Note) *1 : Checked by design, not production tested.
*2 : Typical Value checked by design.
*3 : Connector & substrate loss (0.10 dB) included.

APPLICATION INFORMATION (continued)

REFERENCE VALUES FOR DESIGN (continued)

Notes) Vcc = 2.5 V to 3.0 V

Ta = –25°C to 75°C unless otherwise specified.

Parameter	Symbol	Conditions	Reference values			Unit	Note
			Min	Typ	Max		
DC electrical characteristics							
Supply current HG	IccHT	VCC current at High-Gain mode No input signal	—	3.0	4.5	mA	*1
Supply current LG	IccLT	VCC current at Low-Gain mode No input signal	—	1.0	10.0	µA	*1
Switching current (High)	IIHT	Current at CNT pin VIH = V_{CC}	—	4.6	20	µA	*1

Note) *1 : Checked by design, not production tested.

APPLICATION INFORMATION (continued)

REFERENCE VALUES FOR DESIGN (continued)

Notes) Vcc = 2.5 V to 3.0 V

Ta = –25°C to 75°C, fRXb = 470 MHz, 620 MHz, 770 MHz, PRX = –30 dBm, CW unless otherwise specified

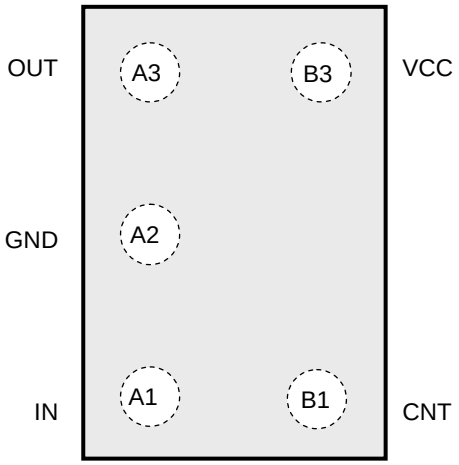
Parameter	Symbol	Conditions	Reference values			Unit	Note
			Min	Typ	Max		
LNA AC electrical characteristics							
Power Gain HG	GHT	High-Gain mode	11.0	15.0	18.0	dB	*1
Power Gain LG	GLT	Low-Gain mode PRX = –20 dBm	–8.5	–4.0	–1.0	dB	*1
Noise Figure HG	NFHT	High-Gain mode	—	1.3	3.0	dB	*1,*3
Noise Figure LG	NFLT	Low-Gain mode	—	6.5	9.0	dB	*1
IIP3 +10 MHz offset HG	IIP3H1Ta	High-Gain mode f1 = fRXb + 10 MHz f2 = fRXb + 20 MHz Input 2 signals (f1, f2)	–14.0	–4.0	—	dBm	*1
IIP3 +10 MHz offset HG	IIP3H2Ta	High-Gain mode f1 = fRXb – 10 MHz f2 = fRXb – 20 MHz Input 2 signals (f1, f2)	–14.0	–4.0	—	dBm	*1
Input P1dB HG	P1dBHT	High-Gain mode f1 = fRXb – 190 MHz PRX1 = –27 dBm f2 = fRXb – 95 MHz PRX2 = –33 dBm Input 2 signals (f1, f2)	–12.0	–6.0	—	dBm	*1

Note) *1 : Checked by design, not production tested.

*3 : Connector & substrate loss (0.10 dB) included.

PIN CONFIGURATION

Top View

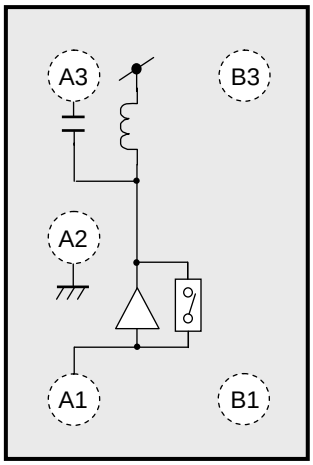


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
A1	IN	Input	RF Input
A2	GND	Ground	GND
A3	OUT	Output	RF Output
B1	CNT	Input	High-Gain / Low-Gain switch L: Low-Gain Mode H: High-Gain Mode
B3	VCC	Power Supply	V_{CC}

FUNCTIONAL BLOCK DIAGRAM

Top View

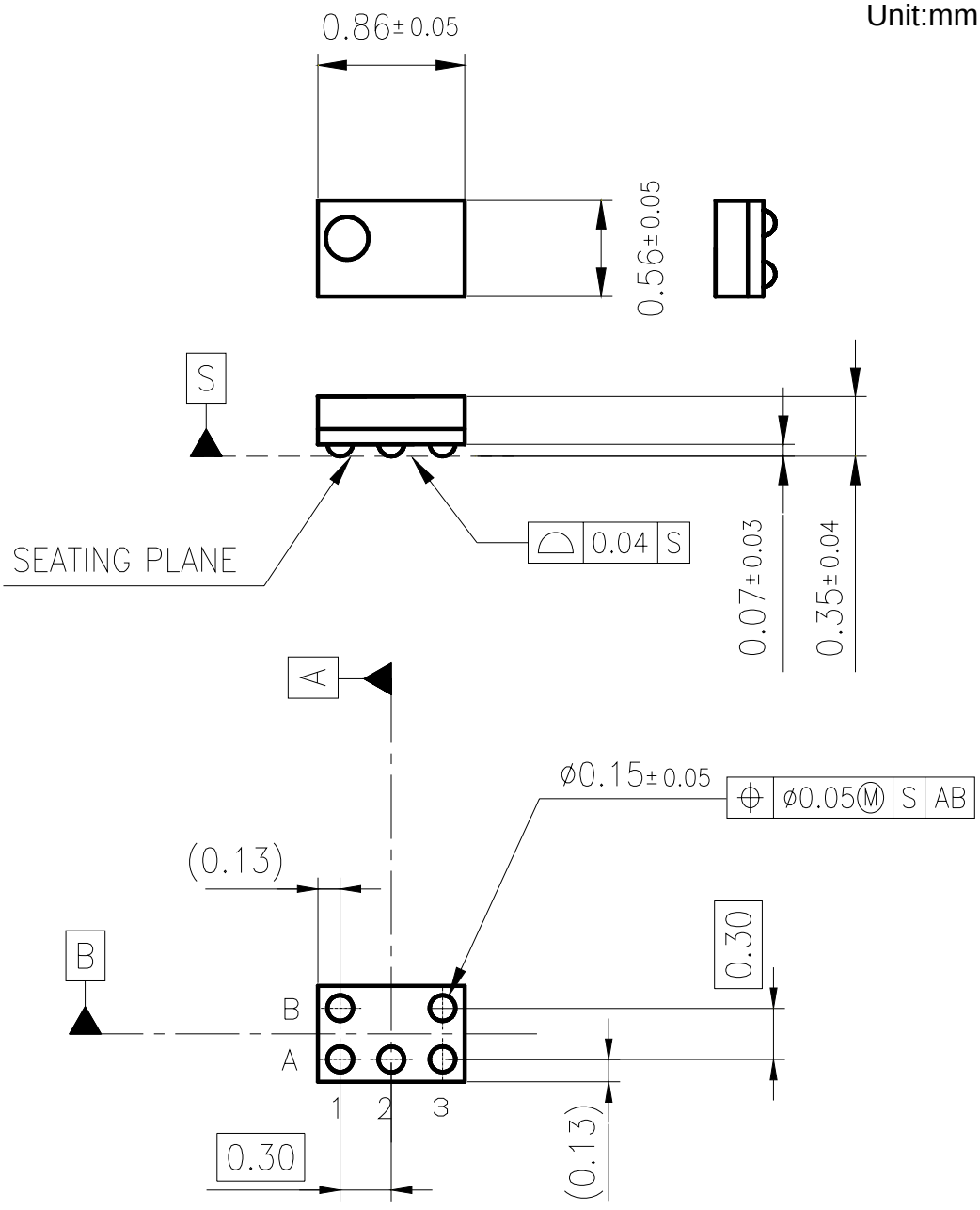


Notes) This circuit and these circuit constants show an example and do not guarantee the design as a mass-production set.
This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

PACKAGE INFORMATION (Reference Data)

Package Code:ALGA005-W-0609ANA

Unit:mm



Body Material : Br/Sb Free Epoxy Resin
Reroute Material : Cu
Bump : SnAgCu

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(6) Disaster prevention and security device
(7) Weapon
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USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

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2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. Due to unshielded structure of this LSI, under exposure of light, function and characteristic of the product cannot be guaranteed. During normal operation or even under testing condition, please ensure that LSI is not exposed to light.

8. Basically, chip surface is ground potential. Please design to ensure no contact between chip surface and metal shielding.

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