VSC3304

8.5 Gbps 4 × 4 Asynchronous Crosspoint Switch

Datasheet

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Revision 4.0
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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.0

Revision 4.0 of this datasheet was published in December 2008. The following is a summary of the changes implemented in the datasheet:

- In the register map for the individual registers, the functionality of bits 2:0 (LOS threshold) in the Input LOS register was corrected to be consistent with the register. For more information, see Figure 2, page 26.
- The moisture sensitivity is now specified as level 4.
- For reference purposes, typical ranges are now provided for long and short pre-emphasis levels and pre-emphasis decay settings. For more information, see Table 8, page 30, Table 9, page 30, Table 19, page 37, and Table 20, page 37.
- The reset value for output power levels, bits 3:0 in the individual and global Output Level registers, was corrected from 0000 to 0001.
- The recommended operating temperature was changed to –40 °C to 110 °C for 6.5 Gbps operation and –40 °C to 100 °C for 8.5 Gbps operation, based on characterization results. For more information, see "Operating Conditions," page 49.
- As a result of final characterization, the input voltage swing parameter was updated, based on the operating conditions stated earlier in this section. For more information, see Table 29, page 42, Table 34, page 45, and Table 35, page 46.
- Power dissipation values for nominal and maximum drive levels were also updated based on final characterization. For more information, see Table 33, page 44.
- The typical value for the propagation delay was changed from 450 ps to 420 ps.
- A design consideration was added about using the OOB forwarding feature with SAS or SATA applications. For more information, see "Design Considerations," page 56.
- Information about the Software Reset register was removed, because the same information is provided in the Initial Setup register.

Revision 2.2

Revision 2.2 of this datasheet was published in August 2008. The following is a summary of the changes implemented in the datasheet:

- Electrostatic discharge (ESD) voltage was added. For human body model (HBM), it is Class 2. For charged device model (CDM), it is ±750 V.
- The power-on reset sequence was clarified to state that if an external controller is connected to a power supply other than VDD, VDD must be powered up first. The

power-on reset circuitry sequence was also modified to include the VDDIO supply as well as the VDD supply.

- It is recommended that an external heatsink be used for higher power level configurations.
- Theta JB is now specified as 28 °C/W.
- The maximum case operating temperature was extended from 85 °C to 110 °C.
- Package dimensions and tolerances were modified. The most significant modification was the maximum package height, which changed from 1.44 mm to 1.40 mm.
- The first write operation when configuring the device was modified to include the SPI interface in proper format.
- Restrictions on I/O configurations and output level and pre-emphasis settings were added to ensure that the device does not exceed maximum power dissipation specifications.
- In the individual and global Input LOS registers, the input loss-of-signal (LOS) threshold bit settings (bits 2:0) were updated.
- The minimum value for the input voltage swing, differential drive, changed from 100 mV to 200 mV.
- The serial data output voltage swing levels were updated based on characterization results.
- Four-wire serial timing has been fully characterized and is now supported.
- In the Stress Ratings, the potential to ground rating was separated into two specifications to clarify the maximum value for each power supply. For V_{DD}, the maximum value is 3.0 V, and for V_{DDIO}, the maximum value is 3.8 V. For both parameters, the minimum value remains at –0.5 V. Additionally, the maximum value for the TTL DC input voltage applied changed from V_{DD} + 1.0 V to V_{DD} + 0.5 V.
- For clarification purposes, the output common-mode voltage was updated to include the V_{DDIO} 2.5 V condition, with values of 0.5 V minimum, 1.1 V typical, and 1.7 V maximum. For the 3.3 V condition, the minimum value changed from 1.9 V to 1.3 V, the typical value changed from 2.1 V to 1.9 V, and the maximum value changed from 2.3 V to 2.5 V.
- For the LVTTL/CMOS input signals, the maximum value for the input HIGH voltage changed from V_{DD} + 0.7 V to V_{DD} + 0.5 V. Additionally, the input HIGH current and the input LOW current changed from ±10 mA to ±150 µA.
- A pull-up resistor is required on the SDA pin for the LVTTL/CMOS output signals.
- References to “any input A” and “any output Y” and their associated symbols were removed, because they do not apply to this device.
- The minimum and maximum values for the propagation delay were removed; the typical value remains at 450 ps. The minimum and maximum values for the output channel-to-channel delay skew parameter were also removed, and a typical value of 50 ps was added.

- The parameter name of the serial output data jitter specification changed to “Serial output data total added random jitter” to reflect the type of jitter specified, and a condition of BER = 10^{-12} was added. The typical value changed from 20 ps to 6 ps, and a maximum value of 14 ps was added. For the serial data output rise and fall time parameter, the minimum value of 50 ps was removed, a typical value of 45 ps was added, and the maximum value changed from 100 ps to 70 ps.
- For the two-wire serial interface AC specifications, a setup time of 0.6 µs minimum for the START condition was added. The setup time for the STOP condition parameter was removed, because it is not supported.
- The serial data input rise time and fall time and the serial data output duty cycle parameters for the high-speed outputs were removed.
- Information about the Software Reset register was missing in previous revisions of the datasheet. The information has been added.
- The bus load parameter for the two-wire interface was updated to differentiate between resistor and active pull-up devices; the maximum value for the resistive pull-up is 200 pF, and the maximum value for the active pull-up (3 mA maximum) is 400 pF.

Revision 2.1

Revision 2.1 of this datasheet was published in November 2007. The following is a summary of the changes implemented in the datasheet:

- The initialization sequence was changed by adding a second operation, which is to write 06’h to register 7A’h. This configures the addressing mode for bi-directional ports A through H. This reconfiguration also changes the numerical addressing associated with the input and output ports (matching the bi-directional port addressing for the device). This change was necessary to correct for a programming logic error.
- The data rate was corrected from 6 Gbps to 8.5 Gbps.
- The naming convention for the ports was modified to reflect that they are bidirectional ports. The following pins have been renamed:
  E and EN (formally A0 and AN0)
  F and FN (formally A1 and AN1)
  G and GN (formally A2 and AN2)
  H and HN (formally A3 and AN3)
  A and AN (formally Y0 and YN0)
  B and BN (formally Y1 and YN1)
  C and CN (formally Y2 and YN2)
  D and DN (formally Y3 and YN3)
- In the last release of this datasheet, the pin numbers for the G and H (formerly A2 and A3) signals were inadvertently switched. In this datasheet release, the pin numbers were corrected: pin E6 is G, and pin F5 is H. In addition, the pin number for signal D was corrected to A5.
- Throughout this datasheet, references to the latched LOS condition were removed, because it is not supported.

- The power-up sequence was clarified. If the external controller uses 3.3 V logic, VDD should be powered up before VDDIO.
- Bit 4 of the Output Level register (individual address 22'h and global address 56'h) was corrected from reserved to "terminate to VDDIO – 0.7 V."
- Bit 2 of the Input State register (individual page address 11'h and global address 52'h) was corrected from "terminate to VDD" to reserved.
- The previous release of the datasheet incorrectly referenced the input port termination to V_{DD} – 0.8 V. It has been corrected to reference V_{DDIO} – 0.7 V.
- In the Global Register Map table, the bit description for bit 0 in the Interface Mode register was corrected to match the register bit description.
- In the DC specifications for the high-speed data inputs, the maximum value for the input common-mode voltage was corrected from V_{DD} to V_{DDIO} – 0.7 V. For the LVTTL and CMOS input signals, the maximum value for the input HIGH voltage parameter was corrected from V_{DD} + 0.6 V to V_{DD} + 0.7 V.
- For the input voltage swing, differential drive parameter, the minimum value was changed from 100 mV to 200 mV.
- In the AC specifications, the measurement conditions for the high-speed data serial data input and output rise and fall times were corrected.
- In the recommended operating conditions, the minimum and maximum values for the VDDIO power supply voltage were added.
- The 1.8 V power supply option was removed, because it is not supported.
- Design improvements resolved the CMOS I/O operation issue; the control pins SADDR, SDA, SCK, SMI, SMO, and VTSS[3:2] now have internal pull-down resistors.
- In the pin description for the VDDIO power supply, the voltage range was updated to include 2.5 V.
- In the Status State registers, the descriptions for bit 1 and bit 0 were corrected.

Revision 2.0

Revision 2.0 of this datasheet was published in September 2006. This was the first publication of the document.

1 Product Overview

The VSC3304 is a low-cost, low-power asynchronous crosspoint switch capable of data rates up to 8.5 Gbps. The VSC3304 finds purpose not only as a switch, but also as a buffer that simplifies the design of high-speed signal paths by providing signal equalization at both inputs and outputs to reduce or reverse signal degradation due to transmission line effects.

The VSC3304 has a total of eight ports. All eight may be configured as either inputs or outputs without restriction. This provides the flexibility of using the device as a standard 4 × 4 crosspoint, or anything between a 1:7 to a 7:1 multiplexer, as well as other combinations.

Featuring programmable input signal equalization and output pre-emphasis (each with multiple time constants), the VSC3304 is also ideal for countering signal degradation over a wide variety of transmission media types and lengths.

Typical power consumption for the device is 200 mW per active channel, and unused channels may be deactivated to save the power associated with those ports. Further power savings can be realized by setting the output level settings to the minimum effective value for a specific application.

The VSC3304 has a loss of signal (LOS) detector on every input port with programmable thresholds. The LOS status can be directed to either of two status registers. The LOS signal is also switched to each connected output monitored through the high-speed switching core. Out of band (OOB) signal forwarding can be enabled for each of the outputs, which causes the outputs to be squelched in response to an LOS detect at the corresponding input, thereby propagating an OOB envelope through the switch.

Programming of the VSC3304 is performed through a two-wire or a four-wire serial interface. The two-wire serial interface address can be hardwired using the three address pins or a proprietary two-wire serial interface that allows for address selection after power-up. Functions such as ResetB and Status states are accessible using the registers to ensure maximum flexibility.

1.1 Features

The following table lists the key aspects of the VSC3304 functionality and design along with the corresponding benefits to Vitesse customers.

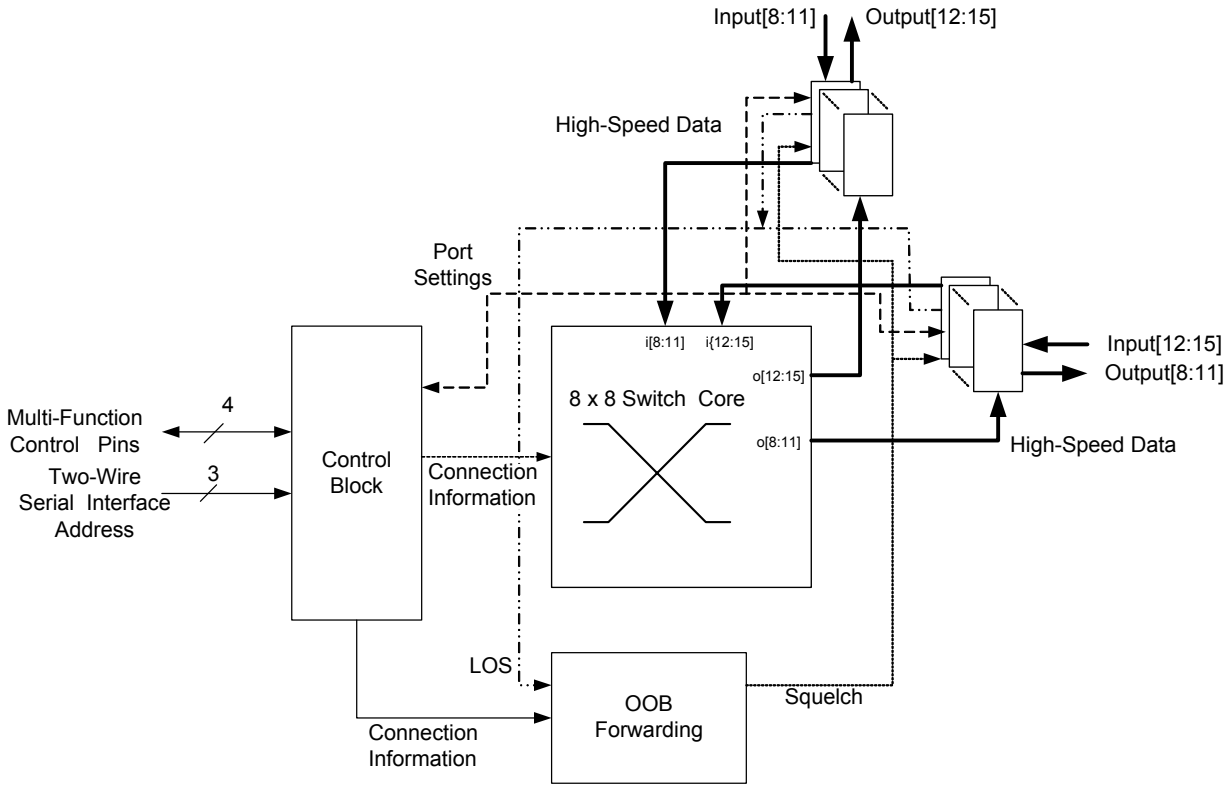
Table 1. Features and Benefits

Feature	Benefit
8.5 Gbps operation	Supports latest high speed protocols
Flexible switching options: multicast, loopback, and snoop capability	Allows great flexibility in routing and fanning signals in distributed and centralized architectures
Two-wire serial bus	Simple programming interface
High-speed four-wire serial programming interface	Allows complete reassignment of all switch connections in less than 14 µs, which is suitable for video switching applications
Asynchronous operation	Data agnostic transfers allow each lane to run speed independent without an external reference clock
User-programmable input and output signal equalization	Flexibility in correcting transmission line effects in a variety of media
Fully reconfigurable high-speed I/O ports	Optimizes signal routing and board design
LOS detection and forwarding	Supports signal monitoring and OOB signal forwarding for SAS and SATA applications
Optional output signal squelch on a per-channel basis	Supports OOB signal forwarding for SAS and SATA applications

1.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC3304 device.

Figure 1. Block Diagram



1.3 Applications

Some of the applications for the VSC3304 device are:

- Wideband signal switching and clean-up
- Line driver or receiver
- Backplane signal fanout, driver, or receiver
- Copper cable driver or receiver
- PCB signal enhancement

2 Functional Descriptions

This section provides descriptions of the functions and features of VSC3304.

2.1 Reset

The VSC3304 can be reset either by writing 1 to the Reset bit or by using the internal power-on reset circuit. The power-on reset circuit is linked to both the VDD and VDDIO supplies.

The reset state is released by energizing the VDD supply. The reset register bit is self-clearing. In general, the power-on reset circuit ensures that the VSC3304 powers up correctly. However, if any of the control pins are connected to a power supply other than VDD, either through a resistor or through an external controller, then the VDD supply should be energized before the other supply.

The minimum threshold for the power-on reset circuit is approximately 2.2 V. Therefore, it is important that there is sufficient decoupling on the circuit board to ensure that the VDD and the VDDIO supply voltage at the pins of the package does not drop below this value when multiple connection paths on the VSC3304 are energized simultaneously. Using the global programming registers can cause multiple paths to transition from an off state to an on state simultaneously.

2.2 Initialization

On reset, the VSC3304 is in low-power state. Initialization requires two consecutive register writes. The first required operation is to select the serial interface mode. Upon reset, the device monitors the pins required for the two-wire and four-wire serial interfaces for a properly formatted write in either mode. To select the two-wire serial interface, the first command must write the value 02'h to address 79'h in correct two-wire format. To select the four-wire interface, the first command must write the value 01'h to address 79'h in proper SPI format. For more information, see “Two-Wire Serial Interface,” page 15 or “Four-Wire Serial Bus (Serial Peripheral Interface),” page 17.

Upon reset, all inputs, outputs, and bias generators are in an off state to reduce the power consumption. Before any connections can be activated, setting the appropriate registers bits energizes these circuits.

2.3 Page-Based Programming

The VSC3304 uses page-based register programming to configure the features and functions of the device. Pages are grouped according to function and each page typically has a maximum of 8 addresses but has a potential address space of 128 8-bit words. The register address within each page corresponds to the number of the input or output that it controls. A specific page is selected by programming the value for the desired page into the Current Page register at address 7F’h.

The Current Page register and all other registers that have an address of 50’h or higher are not linked to a specific page and can be programmed regardless of the value in the Current Page register (address 7F’h). These registers are used to set features and functions of the VSC3304 globally by either setting all 8 registers in an associated page

with a single programming step or by setting a configuration that affects the operation of the entire device. For more information about the registers and their functions, see "Registers," page 26.

2.4 Two-Wire Serial Interface

The VSC3304 supports a slave mode two-wire serial interface where an external master device controls the VSC3304 slave device. The two-wire serial interface operates in both standard mode (up to 100 kbps) and fast mode (up to 400 kbps) data transfer rates.

A master device generates a start condition <S> by transitioning SDA HIGH to LOW while SCK is HIGH. Data is then transferred on the SDA line with the most significant bit (MSB) first and the SCK line clocking each bit. Data transitions occur when the SCK is low and is valid (read) or stable (write) when on the HIGH to LOW transition of the SCK. Data transfers are acknowledged (ACK or <A>) by the receiving device (VSC3304 for data writes and the master device for data reads) by holding the SDA signal low while strobing SCK HIGH, then LOW. The master generates a stop condition <P> (terminates the data transfer) with a LOW to HIGH transition on the SDA signal while SCK is HIGH. For more information, see Figure 4, page 47.

Serial Write A serial write starts with the master sending a byte to the VSC3304. The first seven bits represent the serial interface address, and the eighth must be a 0 to indicate a write operation. The VSC3304 compares its serial interface address (set by the SADDR[5, 3:2] or the Serial Address register) to the one transmitted. An acknowledge is generated only if they match.

Without issuing a start or stop condition, the master then sends a second byte to the VSC3304. The VSC3304 interprets this byte as the register address. Finally, the master sends a third byte to the VSC3304. This is interpreted as the data for the register write. At this point, the write has taken effect.

The following is an example of the write sequence (assuming the serial interface address is set to 00'h):

One Byte Write: <S><00'h><A><Address><A><Data><A><P>

Serial Read A read cycle starts out similarly to the serial write, but immediately after the desired register address (the second byte) is sent, a stop condition is issued. The master then sends the serial interface address again but this time uses a 1 in the LSB to indicate a read operation. After the acknowledge cycle from the VSC3304, the master stops driving the SDA line. At this point, the VSC3304 outputs one bit at a time on the falling edge of SCK, transmitting the MSB first until eight bits are transmitted. After the eighth falling edge of the SCK, the VSC3304 releases control of the SDA bus and the master issues the clock for the acknowledge cycle. After the master issues the acknowledge cycle, the master issues a stop condition, which signals the end of the transmission.

The following is an example sequence (assuming the serial interface address is set to 00'h):

Read: <S><00'h><A><Address><A><P>

The VSC3304 two-wire serial interface supports a 7-bit slave address. This address may be set either of two ways. The first is to hardwire the appropriate SADDR[5, 3:2] pins

to VDD or VSS. Although the VSC3304 has a 7-bit chip address space, only three address pins are actually brought out of the package, limiting the hard-wired addressing to eight addresses. The accessible pins are labeled SADR5, SADR3, and SADR2. Of the remaining four bits, bit 0 is internally tied HIGH, bit 6 is tied LOW, bit 4 is tied to bit 5, and bit 1 is tied to bit 2. These are described in the following table. Note that all 7 bits must appear in the serial device address.

Table 2. Device Address vs. Address Pin State

(SADR6)	SADR5[1] (SADR4)	SADR3[1]	SADR2[1] (SADR1)	(SADR0)	CHP_ADDR in Binary	CHP_ADDR in Hex
0	0	0	0	1	0000001	1'h
0	0	0	1	1	0000111	7'h
0	0	1	0	1	0001001	9'h
0	0	1	1	1	0001111	F'h
0	1	0	0	1	0110001	31'h
0	1	0	1	1	0110111	37'h
0	1	1	0	1	0111001	39'h
0	1	1	1	1	0111111	3F'h

1. Only these three address bits are connected to external pins. The remaining four bits are either tied to fixed levels or to adjacent address pins as shown.

The second addressing method uses a proprietary interface that requires two additional signal wires (SMI and SMO) and permits the address to be programmed on initialization. On reset, the address of the VSC3304 is read from the SADDR[5, 3:2] pins. If no address is programmed into the Serial Address register, then the pin voltages define the permanent address for the device. When a value other than all zeros is programmed into the Serial Address register, then that new value overrides the value on the SADDR[5, 3:2] pins. The SMI pin must be held HIGH to program the Serial Address register.

The Serial Address register does not latch a programmed value unless the SMI pin is held HIGH concurrent with the programming instruction. Also, the MSB (bit 7) of the Serial Address register controls the state of the SMO pin. Therefore, by chaining the SMO of one VSC3304 to the SMI pin of the next, it is possible to change the address of up to 64 different devices connected to the same SCK and SDA lines even if they all initially have identical addresses. Writing an address to the first device with the SMI pin held HIGH changes the address of that device, but the remaining devices all have their SMI pins LOW, so they do not latch the address.

When the address is written to the first device, the state of the SMO can be set HIGH, which sets the SMI pin of the next device HIGH. Now the first device has a different address from the remaining devices, and the SMI pin of the second device is HIGH. The first device does not acknowledge the programming instruction to write to the Serial Address register, and only the second device latches the new address. This process is repeated until all of the devices on the serial bus are defined.

The first programming instruction to the VSC3304 is used to enable the two-wire serial interface. The programming instruction is in the standard format and sets the address 79'h to the value 02'h.

2.5 Four-Wire Serial Bus (Serial Peripheral Interface)

Accessing the VSC3304 registers by means of the SPI interface re-assigns the pins used in the two-wire serial interface as follows:

SPI	Two-Wire
SSB	SMI
SCK	SCK
MOSI	SDA
MISO	SMO

The four-wire serial bus, or serial peripheral interface (SPI), is designed for applications where higher data transfer rates are required. The four-wire interface has a maximum data transfer rate of 30 Mbps. Unlike the two-wire serial interface, chip selection is accomplished through an active LOW serial select signal, SSB(SMI). When the VSC3304 is reset, the VSC3304 is not in a dedicated serial interface mode. To place the VSC3304 in the four-wire SPI mode, the first command to the device must be to write the value 01'h to the register address 79'h. After this command, the MISO(SMO) pin acts as an output when SSB is LOW, and reverts to high impedance when SSB is HIGH. Prior to the initial command to select the four-wire SPI, the MISO pin will always be an active output.

When SSB is LOW, the VSC3304 responds as a slave device. Raising SSB at any time during a read or write terminates that transaction and resets the interface.

SPI Write A write sequence for the SPI interface of the VSC3304 is comprised of three consecutive 8-bit words. Each bit value applied to MOSI(SDA) is latched on the falling edge of SCK. The first word of the sequence indicates whether the command is a write or a read. For a write these first 8-bits are all zero. The next eight bits indicate which register address will be changed, and the last eight bits contain the value to be written to the selected register address. Both the address and data words are transmitted MSB first. SSB must be set LOW to initiate the write sequence and held LOW throughout the sequence. SSB can remain LOW for multiple write operations, but the entire three-byte sequence must be transmitted for each write. There is no sequential or burst mode for the SPI interface.

SPI Read The read sequence for the SPI interface of the VSC3304 requires 32 consecutive cycles of the SCK signal. The first eight bits of the MOSI signal are set to all ones to indicate that it is a read operation. The next eight bits set the register address from which data is to be read. During the third and fourth sets of eight bits, the MOSI signal can be of any value. The third set of eight clock cycles are used to allow the address value and the associated data to propagate between the register and the serial interface. The bits read from MISO during these clock cycles can be discarded. During the fourth and last eight clock cycles of the read sequence, the requested data is clocked out on the MISO pin on each rising edge of SCK. The address, data, and read data are all transmitted MSB first. The SSB pin must be set LOW to begin the sequence and held LOW throughout each sequence. SSB can remain LOW for multiple read operations, but the entire four-byte sequence must be followed for each read. There is no sequential mode for the SPI interface.

2.6 Crosspoint Connections

A complete connection through the VSC3304 requires that the inputs and outputs be properly energized and configured. This section provides the necessary steps to create a complete connection.

The first step is to program a connection through the switch core. The connection page is on page 00'h. Therefore, the first step is to set the current page in the Current Page register (7F'h = 00'h). Next, the value of the desired output port is the value that is used as the address in the connection programming instruction. The data value in the programming instruction is the number of the input port to be connected. The connection register also controls the on and off state of an output. When bit 4 is a 1, the output is disabled and the power used by that output is also turned off.

Consequently, when programming an input value to an output address, bit 4 must be set to 0 for the output to be enabled. The default state for an output is minimum swing and no pre-emphasis. For more information about configuring the output, see "Output Configuration," page 21.

The next step is to configure the selected input correctly. By default, all inputs are turned off to save power on start-up. To turn on the power for a given input, the correct page in the register map must be selected. The Input State Register is in page 11'h. Programming the Current Page register 7F'h to 11'h selects the Input State register page. Bit 1 of this register controls the on and off state of the input. On reset, this bit is set to 1 to turn off the input. To turn the input on, this bit must be set to 0. The selected input becomes the value for the address on this register page, and the value to be written for a basic connection is 0. For more information about configuring the input to optimize performance, see "Input Configuration," page 19.

2.7 Reconfigurable Ports

The standard pin designators identify eight re-programmable ports as inputs or outputs (designated as A, B, C, D, E, F, G, and H). Consequently, the VSC3304 can be set up in a variety of configurations from 1:7 to 7:1 inputs to outputs, depending on the application.

The output circuit sharing a port must be turned off before valid data can be received at the shared input. To turn off a reconfigurable output, write 1 in the bit 4 location of the address for the desired output on page 00'h of the memory map.

The following input and output pairs share the same physical ports:

- A is input 12 or output 8.
- B is input 13 or output 9.
- C is input 14 or output 10.
- D is input 15 or output 11.
- E is input 8 or output 12.
- F is input 9 or output 13.
- G is input 10 or output 14.

- H is input 11 or output 15.

For instance, if using A as in input rather than an output, the first step is to write a 1 to bit 4 of address 08'h on page 00'h, turning off the A output function. Next, turn on input A by writing a 0 to bit 1 of address 0C'h on page 11'h. Finally, make a connection between A and the desired output by writing a 0C'h into the address of the desired output on page 00'h. For more information, see "Two-Wire Serial Interface," page 15.

2.8 Input Configuration

Each input has three sets of registers that are used to configure the various features associated with it. Each of the three sets of registers are on three separate pages of the memory map. Setting the Current Page register (address 7F'h) to 10'h, 11'h, or 12'h provides access to the three pages named Input ISE (Input Signal Equalization), Input State, or Input LOS respectively.

There are a total of eight input ports. Inputs 8 through 11 share physical ports with outputs 12 through 15, respectively. Inputs 12 through 15 share physical ports with outputs 8 through 11, respectively. Enabling the inputs requires additional current. Therefore to reduce the power consumption, it is recommended that any input sharing a port with an output be disabled (which is the default start-up state) before using that port as an output. For more information, see "Reconfigurable Ports," page 18 and "Input Port Disable," page 20.

2.8.1 Input Signal Equalization (ISE)

The input signal equalization on the VSC3304 helps to combat the intersymbol interference (ISI) of high-speed data as it passes through lossy media. This is accomplished by increasing the sensitivity of the receive circuits to the high frequency components of the data edges and works to reverse, in part or in whole, the degradation of signal quality due to propagation through the transmission media.

Discontinuities and losses in the transmission media act as low-pass filters and attenuate the high frequency components of a signal. The cut-off frequency and slope of the filter depend on the specifics of the discontinuities and the losses of the data path. Typically, discontinuities that are small in electrical terms, such as solder pads and connectors, have a high cutoff frequency. Lossy media, such as transmission lines or backplanes, have a lower cutoff frequency bandwidth. The electrical length of the transmission line or the size of a discontinuity affects the magnitude of the attenuation.

The VSC3304 provides flexibility in correcting for transmission losses by providing three independent ISE stages. Each stage has a different time constant (long, medium, and short) associated with it. These designations correspond to the size of the discontinuities described in the previous paragraph. The short time constant ISE is best suited to small discontinuities. The long time constant ISE is well-suited to reducing ISI over long lossy transmission lines. Each ISE stage can be de-activated or set to one of three levels, depending on the magnitude of the signal filtering that occurred during propagation. The bits that control the ISE settings are in the input ISE register (address 10'h). For more information about the registers, see "Input ISE," page 28.

2.8.2 Input Port Termination

Each input is terminated to a 100 Ω differential impedance. The VSC3304 offers eight bidirectional high-speed ports that can be configured as either inputs or outputs. The termination for these ports is shared for both inputs and outputs. In this case, the input is terminated to a supply of V_{DDIO} – 0.7 V. Connecting the input port termination to V_{DDIO} – 0.7 V on a bidirectional port is set by writing a 1 into bit 4 of the output associated with the desired input. The mapping is as follows:

- To connect the termination for input E to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 0C'h on page 22'h.
- To connect the termination for input F to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 0D'h on page 22'h.
- To connect the termination for input G to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 0E'h on page 22'h.
- To connect the termination for input H to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 0F'h on page 22'h.
- To connect the termination for input A to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 08'h on page 22'h.
- To connect the termination for input B to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 09'h on page 22'h.
- To connect the termination for input C to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 0A'h on page 22'h.
- To connect the termination for input D to V_{DDIO} – 0.7 V, write a 1 into bit 4 of register address 0B'h on page 22'h.

For more information, see "Output Level," page 31.

2.8.3 Input Port Disable

Each input port must be enabled before it forwards received data to the switching core. The on and off control bit for the inputs is located on page 11'h. Each address on this page refers to the number of the corresponding input. When bit 1 is set to 1, then the input port is disabled and the power associated with that port is conserved. When the part is reset, this bit is set to a 1 by default. Therefore, any inputs that are used must be enabled before use. For more information about these registers, see "Input State," page 29.

2.8.4 Input Signal Invert

The VSC3304 incorporates the ability to invert the signal at the input to simplify the design of high-speed boards and interconnect.

Bit 0 of the registers on the input state page (11'h) selects whether the input is inverted or normal. Each register address on the input state page corresponds to the like numbered input. For more information about the register settings, see "Input State," page 29.

2.8.5 Input LOS

Each input has an LOS (loss of signal) detector associated with it that sets a bit HIGH whenever the signal level drops below a selected value. Although there is a time component to the detection, the primary metric for asserting the LOS signal is the signal amplitude. This amplitude is selectable in the registers on the input LOS page (12'h). For more information about the amplitude settings, see "Input LOS," page 29.

The LOS signal is asserted upon a loss of signal or deasserted when a signal is present for more than 2 ns from when the signal level again exceeds the threshold.

This signal can be read from the registers on the channel status page.

This signal is also forwarded to any output that is connected to the corresponding input and can be used to squelch a transmitted signal when the connected input goes into an LOS state.

2.9 Output Configuration

Each output has four sets of registers that are used to configure the various features associated with the selected output. Each of the four registers is on a separate page of the memory map. Setting the Current Page register (address 7F'h) to 20'h, 21'h, 22'h, or 23'h provides access to the four pages named Output Pre Long, Output Pre Short, Output Level, or Output State, respectively.

The sum of all the levels for the amplitude and the long and short pre-emphasis must not exceed a total of 15. For example, if the output level is set to 8 and the short pre-emphasis amplitude is set to 5, then the amplitude setting for the long pre-emphasis should not exceed 2. If only one of the pre-emphasis time constants is required, then the sum of 15 need only be divided between the output level and the pre-emphasis setting of the selected time constant. If no pre-emphasis is used, then there is no restriction on the output amplitude. To maximize flexibility in configuring the output equalization at low output amplitude settings, there are equalization settings that are excessive at high output amplitudes. It is possible to select the large equalization amplitudes even with the higher output levels, but these stress the limits of the output driver. The result is a deformed output waveform rather than one that has been properly equalized, accompanied by excessive power dissipation.

There are a total of eight output ports. Outputs 8 through 11 share physical ports with inputs 12 through 15, respectively. Outputs 12 through 15 share physical ports with inputs 8 through 11, respectively. Enabling the inputs requires additional current. Therefore to reduce the power consumption, it is recommended that any input sharing a port with an output be disabled (which is the default start-up state) before using that port as an output.

The output ports must be configured in such a way as to not exceed power limits of the device. For information about the power requirements, see "Power Supply Requirements," page 44.

2.9.1 Output Pre-Emphasis

The output pre-emphasis function of the VSC3304 helps to combat the intersymbol interference (ISI) of high-speed data as it passes through lossy media. This is accomplished by shaping the output waveform to boost the magnitude of those

frequency components of the transmitted signal that are most susceptible to attenuation as it propagates through the transmission media.

Discontinuities and losses in the transmission media act as low-pass filters and attenuate the high-frequency components of a signal. The cutoff frequency and slope of the filter depend on the specifics of the discontinuities and the losses as the signal propagates through the discontinuities or media. Typically, discontinuities that are small in electrical terms, such as solder pads and connectors, have a high cutoff frequency. Lossy media, such as transmission lines or backplanes, have a lower cutoff frequency bandwidth. The electrical length of the transmission line or the size of a discontinuity affects the magnitude of the attenuation.

The VSC3304 provides flexibility in correcting for transmission losses with two independent pre-emphasis stages that are additive. Each stage has a different time constant (long and short) associated with it. The short time constant pre-emphasis is best suited to small discontinuities and electrically short transmission lines. The long time constant pre-emphasis is well suited to reducing ISI over long lossy transmission lines.

Each pre-emphasis stage can be deactivated or set to one of 15 levels, depending on the magnitude of the signal filtering that occurred during propagation. Additionally, each of the pre-emphasis stages permits the bandwidth of the boosted signal to be adjusted. Both the long and short pre-emphasis stages have eight bandwidth settings. The bandwidth settings adjust the lower limit of the signal boost and have a single pole roll-off. The uppermost frequency of the signal boost is limited by the slew rate of the output amplifier.

The bits that control the pre-emphasis settings are in the Output Pre Long and Output Pre Short registers (address 20’h and 21’h). For more information about these settings and registers, see “Output Pre Long,” page 30 and “Output Pre Short,” page 30.

2.9.2 Output Power Level

The VSC3304 provides a selection of 13 power levels that enable compliance with most popular transmission standards. The output level is selectable using bits [3:0] in the registers on the output level page (address 22’h). The register address within the page is used to identify the number of the output that it controls.

The output ports must be configured in such a way as to not exceed power limits of the device. For information about the power requirements, see “Power Supply Requirements,” page 44.

The uppermost level setting is only available when the V_{DDIO} supply is connected to a 3.3 V supply. All other levels are available with a 2.5 V supply connected to V_{DDIO}.

For more information about the specific output levels and the values used to select them, see “Output Level,” page 31.

2.9.3 Output Signal Suppression and Inversion

The VSC3304 can be configured to selectively invert any output to simplify the design of high-speed boards and interconnects.

It is also possible to suppress an output signal to reduce signal noise in a system. When the output signal is suppressed, the true and complement values are driven to the common mode value. This signal level is stable and maintains a DC level that is within ±50 mV.

Both of these functions are controlled by bits [4:1] of the registers on the output state page 23'h. For more information about the bit values that set the state of the output for normal, inverted, or suppressed operations, see "Output State," page 32.

2.9.4 Out of Band Signal Forwarding

As mentioned previously, VSC3304 has the ability to suppress the output signal in response to an LOS assertion at the connected input. For more information, see "Input LOS," page 21. The purpose of this feature is to propagate out of band (OOB) signaling information through the VSC3304 and is compatible with SAS and SATA operation. For information about SAS and SATA compatibility, see "Design Considerations," page 56.

The VSC3304 features an OOB forwarding switch core that duplicates the connections in the high-speed switch core. This core is used to switch the LOS detect signal. With bit 0 of an Output State Register set to 1, the selected output is suppressed whenever the connected input asserts an LOS condition. This overrides the current output state for as long as the LOS from the input remains asserted. After the LOS condition is removed and the LOS is deasserted, the output assumes whatever state is set in bits [4:1] for that output.

It takes approximately 4 ns for the LOS condition to be propagated from the input to the output.

For more information about controlling this function, see "Output State," page 32.

2.10 Status Bits

The VSC3304 provides two status bits (STAT0 and STAT1) that permit monitoring of LOS conditions of one or more selected inputs. LOS signals from one or more of the inputs can be OR'ed together to generate the final state of either of these status bits.

There is a separate page for both STAT0 and STAT1. The registers on the Status 0 page (80'h) control STAT0, and the registers on the Status 1 page (81'h) control STAT1. Each address on each page refers to the input with the same number. Bit 0 connects the LOS condition for the selected input to the status bit associated with the page that is being programmed. For more information about the term LOS, see "Channel Status," page 24.

For example, when the value 01'h is programmed to address 08'h and the value 01'h is programmed to address 09'h (both located on page 80'h), the value of STAT0 bit 1 is equal to 1 whenever input 8 or input 9 detects an LOS condition. When neither input 8 nor input 9 detects an LOS position, then STAT0 bit 1 is equal to 0.

The state of STAT0 and STAT1 can be monitored using the programming interface. The Status register is located on the Channel Status page (F0'h) at register address 10'h. The two LSBs of this register show the current state of STAT0 and STAT1. Bit 0 reflects the state of STAT0, and bit 1 reflects the state of STAT1.

This provides a convenient and efficient way of polling the VSC3304 for the LOS conditions of multiple inputs by using a single register read. The LOS condition of each of the inputs can be assigned to one STAT bit or divided between STAT0 and STAT1 using the registers on the Status 0 and Status 1 pages. When the value is nonzero, then more detailed polling of each of the registers on the Channel Status page reveals which input exhibited the LOS condition. If the LOS conditions of the inputs are split among STAT0 and STAT1, fewer reads are required to locate the input with the LOS condition.

For more information about these registers, see "Status State," page 34. For more information about STAT0 and STAT1 in the registers, see "Status 0 Configuration," page 33 and "Status 1 Configuration," page 33.

2.11 Channel Status

The VSC3304 has a register associated with each input that reflects its LOS status. These registers are located on the channel status page (address F0'h) and the address of each register corresponds to the number value of the input that it represents.

Bit 0 is described as the LOS bit. This is the bit that reflects the current LOS state for the input as identified by the address that is read. For more information about these registers, see "Channel Status," page 32.

2.12 Global Programming

The VSC3304 provides the convenience of Global Programming registers to reduce the number of instructions required to initialize the device. A global programming register is associated with each page of registers with the exception of the one read-only page (F0'h) that contains the Channel Status and Pin Status registers. A single programming instruction to one of the global programming registers copies the same value to all the registers on the associated page. The global programming registers are assigned to each page as shown in the following table.

Table 3. Global Registers and Associated Pages

Global Register Name	Address	Page of Registers	Address
Global Input ISE	51'h	Input ISE	10'h
Global Input State	52'h	Input State	11'h
Global Input LOS	53'h	Input LOS	12'h
Global Output Pre Long	54'h	Output Pre Long	20'h
Global Output Pre Short	55'h	Output Pre Short	21'h
Global Output Level	56'h	Output Level	22'h
Global Output State	57'h	Output State	23'h
Global Status 0	58'h	Status 0	80'h
Global Status 1	59'h	Status 1	81'h

Caution should be exercised when using the global programming registers to change values on input state pages. Because this programs all 8 inputs simultaneously, it either turns all of them on or all of them off as well. This may cause a connection to be

broken, or may cause data corruption if an input is turned on for a bidirectional port currently being used as an output.

Turning on additional inputs does not affect the signal quality of the output on a bidirectional port, but it does use additional power. Turning on all inputs simultaneously also generates an instantaneous current spike. If there is insufficient decoupling capacitance connected to the package pins, the instantaneous power supply voltage may drop below the minimum level required to trip the device power-on reset that would change the device configuration.

3 Registers

This section contains information about the software interface. The purpose of this section is to provide information about the programming interface, register maps, register descriptions, and register tables.

3.1 Individual Register Map

This section provides a register map containing summary descriptions for the individual registers. For more information about setting the individual registers, see "Individual Registers," page 28.

Figure 2. Register Map for the Individual Registers

Page	Address Range	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00'h	08'h to 0F'h	Connection	Reserved - read only			Output off	Input to connect (0 to 7)			
10'h	08'h to 0F'h	Input ISE	Reserved - read only		ISE - Short time constant		ISE - medium time constant		ISE - long time constant	
11'h	08'h to 0F'h	Input State	Reserved - read only			Reserved - do not program			Input off	Invert input
12'h	08'h to 0F'h	Input LOS	Reserved - read only					LOS threshold		
20'h	08'h to 0F'h	Output Pre Long	Reserved - read only	Long time constant pre-emphasis level				Long time constant pre-emphasis decay		
21'h	08'h to 0F'h	Output Pre Short	Reserved - read only	Short time constant pre-emphasis level				Short time constant pre-emphasis decay		
22'h	08'h to 0F'h	Output Level	Reserved - read only		Reserved - do not program	Terminate to VDDIO – 0.7 V (Input)	Output power level			
23'h	08'h to 0F'h	Output State	Reserved - read only			Output Operation mode				Enable LOS forwarding
80'h	08'h to 0F'h	Status Pin 0	Reserved - read only							LOS
81'h	08'h to 0F'h	Status Pin 1	Reserved - read only							LOS
A0'h	08'h to 0F'h	Reserved	Reserved – do not program							
F0'h	08'h to 0F'h	Channel Status	Reserved - read only							LOS
F0'h	10'h	Status State	Reserved - read only						STAT1	STAT0
FF'h	00'h	Reserved	Reserved – read only							

3.2 Global Register Map

This section provides a register map containing summary descriptions for the global registers. For information about setting the global registers, see "Global Registers," page 35.

Figure 3. Register Map for Global Registers

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50'h	Reserved	Reserved - do not program							
51'h	Global Input ISE	Reserved - read only		ISE - short time constant		ISE - medium time constant		ISE - long time constant	
52'h	Global Input State	Reserved - read only			Reserved - do not program			Input off	Invert input
53'h	Global Input LOS	Reserved - read only					LOS threshold		
54'h	Global Output Pre Long	Reserved - read only	Long time constant pre-emphasis level				Long time constant pre-emphasis decay		
55'h	Global Output Pre Short	Reserved - read only	Short time constant pre-emphasis level				Short time constant pre-emphasis decay		
56'h	Global Output Level	Reserved - read only		Reserved – do not program	Terminate inputs to VDDIO – 0.7 V	Output power level			
57'h	Global Output State	Reserved - read only			Output operation mode				Enable LOS forwarding
58'h	Global Status 0 Pin	Reserved - read only							LOS
59'h	Global Status 1 Pin	Reserved - read only							LOS
74'h	Reserved	Reserved - do not program							
75'h	Reserved	Reserved - do not program							
78'h	Serial Address	SMO value	Serial port address						
79'h	Interface Mode	Reserved - read only					Reserved - do not program	Two-wire serial	Four-wire serial
7A'h	Initial Setup	Reserved - do not program			RESET	Address range setting			
7B'h	Reserved	Reserved - do not program							
7C'h	Reserved	Reserved - do not program							
7D'h	Reserved	Reserved - do not program							
7E'h	Reserved	Reserved - do not program							
7F'h	Current Page	Current page address							

3.3 Individual Registers

This section contains information about the individual registers.

3.3.1 Connection

The settings in these registers make connections and enable outputs.

Register name: Connection

Page address: 00'h

Register address: 08'h - 0F'h

Register type: R/W

Table 4. Connection

Bit	Bit Label	Description	Access	Reset
7:5	Reserved	Reserved - Read only	R	000
4	Turn off output	0 = Output enabled 1 = Output off	R/W	1
3:0	Input number	Number of the input to connect to the selected output	R/W	0000

3.3.2 Input ISE

This register configures the input signal equalization for the selected input.

Register name: Input ISE

Page address: 10'h

Register address: 08'h - 0F'h

Register type: R/W

Table 5. Input ISE

Bit	Bit Label	Description	Access	Reset
7:6	Reserved	Reserved - Read only	R	00
5:4	ISE – short time constant	00 = Off 01 = Minimum 10 = Moderate 11 = Maximum	R/W	00
3:2	ISE – medium time constant	00 = Off 01 = Minimum 10 = Moderate 11 = Maximum	R/W	00
1:0	ISE – long time constant	00 = Off 01 = Minimum 10 = Moderate 11 = Maximum	R/W	00

3.3.3 Input State

This register defines the input enable, polarity, and terminations settings for the selected input.

Register name: Input State

Page address: 11'h

Register address: 08'h - 0F'h

Register type: R/W

Table 6. Input State

Bit	Bit Label	Description	Access	Reset
7:5	Reserved	Reserved - Read only	R	000
4:2	Reserved	Reserved - Do not program	R/W	001
1	Input power off	0 = On 1 = Off	R/W	1
0	Invert signal at input	0 = Normal 1 = Inverted	R/W	0

3.3.4 Input LOS

This register configures the input LOS threshold value for the selected input.

Register name: Input LOS

Page address: 12'h

Register address: 08'h - 0F'h

Register type: R/W

Table 7. Input LOS

Bit	Bit Label	Description	Access	Reset
7:3	Reserved	Reserved - Read only	R	00000
2:0	LOS threshold settings (peak-to-peak differential voltage)	111 = Unused 110 = Unused 101 = Unused 100 = Unused 011 = Unused 010 = 400 mV 001 = 200 mV 000 = Unused	R/W	100

3.3.5 Output Pre Long

This register sets the long time constant pre-emphasis for selected output.

Register name: Output Pre Long

Page address: 20'h

Register address: 08'h - 0F'h

Register type: R/W

Table 8. Output Pre Long

Bit	Bit Label	Description	Access	Reset
7	Reserved	Reserved - Read only	R	0
6:3	Pre-emphasis level	0000 = Off 0001 = Minimum ... 1111 = Maximum Typical range is 0 dB to 6 dB.	R/W	0000
2:0	Pre-emphasis decay	000 = Fastest ... 111 = Slowest Typical range is 500 ps to 1500 ps.	R/W	000

3.3.6 Output Pre Short

This register sets the short time constant pre-emphasis for selected output.

Register name: Output Pre Short

Page address: 21'h

Register address: 08'h - 0F'h

Register type: R/W

Table 9. Output Pre Short

Bit	Bit Label	Description	Access	Reset
7	Reserved	Reserved - Read only	R	0
6:3	Pre-emphasis level	0000 = Off 0001 = Minimum ... 1111 = Maximum Typical range is 0 dB to 6 dB.	R/W	0000
2:0	Pre-emphasis decay	000 = Fastest ... 111 = Slowest Typical range is 30 ps to 500 ps.	R/W	000

3.3.7 Output Level

This register sets the output power level (peak-to-peak differential voltage).

Register name: Output Level

Page address: 22'h

Register address: 08'h - 0F'h

Register type: R/W

Table 10. Output Level

Bit	Bit Label	Description	Access	Reset
7:6	Reserved	Reserved - Read only	R	00
5	Reserved	Reserved - Do not program	R/W	0
4	Terminate to VDDIO – 0.7 V (input only)	0 = Normal 1 = Connect	R/W	0
3:0	Output power level (peak-to-peak differential voltage)	0000 = Unused 0001 = Unused 0010 = 405 mV 0011 = 425 mV 0100 = 455 mV 0101 = 485 mV 0110 = 520 mV 0111 = 555 mV 1000 = 605 mV 1001 = 655 mV 1010 = 720 mV 1011 = 790 mV 1100 = 890 mV 1101 = 990 mV (3.3 V supply required) 1110 = Unused 1111 = Unused	R/W	0001

3.3.8 Output State

This register provides OOB signaling and output invert for selected output.

Register name: Output State

Page address: 23'h

Register address: 08'h - 0F'h

Register type: R/W

Table 11. Output State

Bit	Bit Label	Description	Access	Reset
7:5	Reserved	Reserved - Read only	R	000
4:1	Output operation mode	1010 = Inverted 0101 = Normal operation 0000 = Suppressed Any other combinations result in undefined operation.	R/W	0101
0	Enable LOS forwarding	0 = Ignore LOS 1 = Enable OOB forwarding	R/W	0

3.3.9 Channel Status

This register provides the LOS status for the selected input.

Register name: Channel Status

Page address: F0'h

Register address: 08'h - 0F'h

Register type: R

Table 12. Channel Status

Bit	Bit Label	Description	Access	Reset
7:1	Reserved	Reserved - Read only	R	0000000
0	LOS	0 = Signal present 1 = LOS detected	R	0

3.3.10 Status 0 Configuration

This register assigns LOS signals from selected input to STAT0.

Register name: Status 0 Configuration

Page address: 80'h

Register address: 08'h - 0F'h

Register type: R/W

Table 13. Status 0 Configuration

Bit	Bit Label	Description	Access	Reset
7:1	Reserved	Reserved - Read only	R	0000000
0	LOS Channel Status value OR'ed on STAT0	0 = No connection 1 = LOS assigned to STAT0	R/W	0

3.3.11 Status 1 Configuration

This register assigns LOS signals from selected input to STAT1.

Register name: Status 1 Configuration

Page address: 81'h

Register address: 08'h - 0F'h

Register type: R/W

Table 14. Status 1 Configuration

Bit	Bit Label	Description	Access	Reset
7:1	Reserved	Reserved - Read only	R	0000000
0	LOS Channel Status value OR'ed on STAT1	0 = No connection 1 = LOS assigned to STAT1	R/W	0

3.3.12 Status State

This register provides the state of STAT0 and STAT1.

Register name: Status State

Page address: F0'h

Register address: 10'h

Register type: R

Table 15. Status State

Bit	Bit Label	Description	Access	Reset
7:2	Reserved	Reserved - Read only	R	000000
1	Value of STAT1	0: STAT1 = 0 1: STAT1 = 1	R	0
0	Value of STAT0	0: STAT0 = 0 1: STAT0 = 1	R	0

3.4 Global Registers

This section contains information about the global registers.

3.4.1 Global Input ISE

This register configures input signal equalization for all inputs.

Register name: Global Input ISE

Register address: 51'h

Register type: R/W

Table 16. Global Input ISE

Bit	Bit Label	Description	Access	Reset
7:6	Reserved	Reserved - Read only	R	00
5:4	ISE – Short Time Constant	00 = Off 01 = Minimum 10 = Moderate 11 = Maximum	R/W	00
3:2	ISE – Medium Time Constant	00 = Off 01 = Minimum 10 = Moderate 11 = Maximum	R/W	00
1:0	ISE – Long Time Constant	00 = Off 01 = Minimum 10 = Moderate 11 = Maximum	R/W	00

3.4.2 Global Input State

This register sets the input enable, polarity, and terminations settings for all inputs.

Register name: Global Input State

Register address: 52'h

Register type: R/W

Table 17. Global Input State

Bit	Bit Label	Description	Access	Reset
7:5	Reserved	Reserved - Read only	RO	000
4:2	Reserved	Reserved - Do not program	R/W	000
1	Input power off	0 = On 1 = Off	R/W	0
0	Invert signal at input	0 = Normal 1 = Inverted	R/W	0

3.4.3 Global Input LOS

This register configures the loss of signal (LOS) threshold value for all inputs.

Register name: Global Input LOS

Register address: 53'h

Register type: R/W

Table 18. Global Input LOS

Bit	Bit Label	Description	Access	Reset
7:3	Reserved	Reserved - Read only	R	00000
2:0	LOS threshold settings (peak-to-peak differential voltage)	111 = Unused 110 = Unused 101 = Unused 100 = Unused 011 = Unused 010 = 400 mV 001 = 200 mV 000 = Unused	R/W	000

3.4.4 Global Output Pre Long

This register provides the long time constant pre-emphasis settings for all outputs.

Register name: Global Output Pre Long

Register address: 54'h

Register type: R/W

Table 19. Global Output Pre Long

Bit	Bit Label	Description	Access	Reset
7	Reserved	Reserved - Read only	R	0
6:3	Pre-emphasis level	0000 = Off 0001 = Minimum ... 1111 = Maximum Typical range is 0 dB to 6 dB.	R/W	0000
2:0	Pre-emphasis decay	000 = Fastest ... 111 = Slowest Typical range is 500 ps to 1500 ps.	R/W	000

3.4.5 Global Output Pre Short

This register provides the short time constant pre-emphasis settings for all outputs.

Register name: Global Output Pre Short

Register address: 55'h

Register type: R/W

Table 20. Global Output Pre Short

Bit	Bit Label	Description	Access	Reset
7	Reserved	Reserved - Read only	R	0
6:3	Pre-emphasis Level	0000 = Off 0001 = Minimum ... 1111 = Maximum Typical range is 0 dB to 6 dB.	R/W	0000
2:0	Pre-emphasis decay	000 = Fastest ... 111 = Slowest Typical range is 30 ps to 500 ps.	R/W	000

3.4.6 Global Output Level

This register provides the output power level for all outputs. In this table, signal levels are single-ended peak-to-peak voltages for true or complement outputs.

Register name: Global Output Level

Register address: 56'h

Register type: R/W

Table 21. Global Output Level

Bit	Bit Label	Description	Access	Reset
7:6	Reserved	Reserved - Read only	R	00
5	Reserved	Reserved - Do not program	R/W	0
4	Terminate inputs to VDDIO – 0.7 V	0 = Normal 1 = Connect	R/W	0
3:0	Output power level (peak-to-peak differential voltage)	0000 = Unused 0001 = Unused 0010 = 405 mV 0011 = 425 mV 0100 = 455 mV 0101 = 485 mV 0110 = 520 mV 0111 = 555 mV 1000 = 605 mV 1001 = 655 mV 1010 = 720 mV 1011 = 790 mV 1100 = 890 mV 1101 = 990 mV (3.3 V supply required) 1110 = Unused 1111 = Unused	R/W	0001

3.4.7 Global Output State

This register sets the out of band (OOB) signaling and output inversion for all outputs.

Register name: Global Output State

Register address: 57'h

Register type: R/W

Table 22. Global Output State

Bit	Bit Label	Description	Access	Reset
7:5	Reserved	Reserved - Read only	R	000
4:1	Output Operation mode	1010 = Inverted 0101 = Normal operation 0000 = Common mode Any other combinations result in undefined operations.	R/W	0000
0	Enable LOS forwarding	0 = Ignore LOS 1 = Enable OOB forwarding	R/W	0

3.4.8 Global Status 0 Configuration

This register assigns LOS signals from all inputs to STAT0.

Register name: Global Status 0 Configuration

Register address: 58'h

Register type: R/W

Table 23. Global Status 0 Configuration

Bit	Bit Label	Description	Access	Reset
7:1	Reserved	Reserved - Read only	R	0000000
0	LOS channel status value OR'ed on the STAT0	0 = No connection 1 = LOS assigned to STAT0	R/W	0

3.4.9 Global Status 1 Configuration

This register assigns LOS signals from all inputs to the STAT1.

Register name: Global Status 1 Configuration

Register address: 59'h

Register type: R/W

Table 24. Global Status 1 Configuration

Bit	Bit Label	Description	Access	Reset
7:1	Reserved	Reserved - Read only	R	0000000
0	LOS channel status value OR'ed on the STAT1	0 = No connection 1 = LOS assigned to STAT1	R/W	0

3.4.10 Serial Address

This register sets the two-wire serial address.

Register name: Serial Address

Register address: 78'h

Register type: R/W

Table 25. Serial Address

Bit	Bit Label	Description	Access	Reset
7	SMO pin setting	Sets the value of the SMO pin in Two-Wire Serial mode.	R/W	0

Table 25. Serial Address *(continued)*

6:0	Device address setting	Sets the device address for the Two-Wire Serial mode. This setting overrides the values set on the SADDR[5, 3:2] pins. The SMI pin must be pulled High to enable a write to this register.	R/W	0000000

3.4.11 Interface Mode

This register sets the serial interface mode.

Register name: Interface Mode

Register address: 79'h

Register type: R/W

Table 26. Interface Mode

Bit	Bit Label	Description	Access	Reset
7:3	Reserved	Reserved - Read only.	R	00000
2	Reserved	Reserved - Do not program.	R/W	0
1	Two-Wire Serial mode	0 = Unselected 1 = Selected **Important** The first two-wire serial programming sequence must be to program a 1 into this location.	R/W	0
0	Four-Wire Serial mode	0 = Unselected 1 = Selected **Important** The first four-wire serial programming sequence must be to program a 1 into this location.	R/W	0

3.4.12 Initial Setup

This register sets the addressing range and provides a software reset function.

Register name: Initial Setup

Register address: 7A'h

Register type: R/W

Table 27. Initial Setup

Bit	Bit Label	Description	Access	Reset
7:5	Reserved	Reserved - Do not program.	R/W	000
4	Reset	Software reset. This bit is self-clearing.	R/W	0

Table 27. Initial Setup

3:0	Address Range Setting	Sets the port address range to 8'h to F'h. **Important** The second programming sequence must program 6'h into this location.	R/W	3'h

3.4.13 Current Page

This register sets the page value for register programming.

Register name: Current Page

Register address: 7F'h

Register type: R/W

Table 28. Current Page

Bit	Bit Label	Description	Access	Reset
7:0	Current page address	Sets the page for subsequent programming instructions.	R/W	00000000

4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC3304 device.

4.1 DC Characteristics

This section contains the DC specifications for the VSC3304 device.

4.1.1 High-Speed Data Inputs

The following table shows the high-speed data inputs.

Table 29. High-Speed Data Inputs

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input voltage swing, differential drive, up to 6.5 Gbps operation	V_{A-DE}	200		2000	mV	Differential peak-to-peak. Maximum case temperature up to 110 °C.
Input voltage swing, differential drive, up to 8.5 Gbps operation	V_{A-DE}	600		2000	mV	Differential peak-to-peak Maximum case temperature up to 100 °C.
Input common-mode voltage	V_{ICM}	1.0		V_{DDIO} – 0.7	V	
Input resistance	R_{IN}	80	100	120	Ω	Between true and complement of same input

4.1.2 High-Speed Data Outputs

The following table shows the high-speed data outputs. The serial data output voltage swing levels show the voltage peak-to-peak differential between true and complement outputs and 0.1 µF coupling capacitor with 50 Ω to V_{DDIO}.

The output ports must be configured in such a way as to not exceed power limits of the device. For information about the power requirements, see "Power Supply Requirements," page 44.

Table 30. High-Speed Data Outputs

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial data output voltage swing, Level 2	V_{OUT-2}	275	405	575	mV	

Table 30. High-Speed Data Outputs *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial data output voltage swing, Level 3	V_{OUT-3}	290	425	590	mV	
Serial data output voltage swing, Level 4	V_{OUT-4}	315	455	635	mV	
Serial data output voltage swing, Level 5	V_{OUT-5}	335	485	675	mV	
Serial data output voltage swing, Level 6	V_{OUT-6}	355	520	725	mV	
Serial data output voltage swing, Level 7	V_{OUT-7}	380	555	775	mV	
Serial data output voltage swing, Level 8	V_{OUT-8}	410	605	840	mV	
Serial data output voltage swing, Level 9	V_{OUT-9}	455	655	915	mV	
Serial data output voltage swing, Level 10	V_{OUT-10}	500	720	1000	mV	
Serial data output voltage swing, Level 11	V_{OUT-11}	550	790	1100	mV	
Serial data output voltage swing, Level 12	V_{OUT-12}	615	890	1230	mV	
Serial data output voltage swing, Level 13	V_{OUT-13}	690	990	1400	mV	Requires V_{DDIO} = 3.3 V
Back-terminated output resistance	R_{OUT}	40	50	60	Ω	From true or complement to AC ground
Output common-mode voltage	V_{OCM}	1.3	1.9	2.5	V	Depending on output swing (for V_{DDIO} = 3.3 V)
		0.5	1.1	1.7	V	Depending on output swing (for V_{DDIO} = 2.5 V)

4.1.3 LVTTL/CMOS Input Signals

The following table shows the LVTTL/CMOS input signals.

Table 31. LVTTL/CMOS Input Signals

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input HIGH voltage	V_{IH}	1.7	V_{DD} + 0.5	V	V_{DD} = 2.5 V
Input LOW voltage	V_{IL}	0	0.8	V	V_{DD} = 2.5 V
Input HIGH current	I_{IH}		150	µA	
Input LOW current	I_{IL}	–150		µA	

4.1.4 LVTTL/CMOS Output Signals

The following table shows the LVTTL/CMOS output signals.

Table 32. LVTTL/CMOS Output Signals

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output HIGH voltage	V_{OH}	V_{DD} – 0.4	V_{DD}	V	DC load < 500 µA. SDA pin requires external pull-up resistor.
Output LOW voltage	V_{OL}	0	0.4	V	DC load < 2 mA. SDA pin requires external pull-up resistor.

4.1.5 Power Supply Requirements

Vitesse recommends using an external heatsink for higher power level configurations to ensure that the VSC3304 device maintains a case temperature below 110 °C. For information about thermal data, which can help you determine the type of heatsink required for your application, see "Thermal Specifications," page 55.

Total power consumption must remain below 1.95 W for reliable operation of the VSC3304 device, with junction temperature under 125 °C and maximum case temperature at 110 °C. Depending on the configuration and the number of active inputs and outputs, it is possible to dissipate more than 1.95 W of power with the VSC3304 device. For configurations requiring power dissipation greater than 1.95 W, the case temperature must be lowered sufficiently to maintain a junction temperature of less than 125 °C. For more information about the thermal characteristics of the VSC3304 device, see "Thermal Specifications," page 55.

Table 33. Power Supply Requirements

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Power supply voltage	V_{DD}	2.375	2.5	2.625	V	
Power supply voltage, high-speed outputs	V_{DDIO}	2.375 or 3.135	2.5 or 3.3	2.625 or 3.465	V	3.3 V for maximum output swing

Table 33. Power Supply Requirements *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Total power dissipation, nominal drive – Level 5	$P_{D\text{-}L5}$		0.95	1.5	W	4 inputs and 4 outputs enabled V_{DDIO} = 2.5 V Maximum value is worst case.
Total power dissipation, maximum drive – Level 13	$P_{D\text{-}L13}$		1.8	2.8(1)	W	4 inputs and 4 outputs enabled; V_{DDIO} = 3.3 V Maximum value is worst case.

1. The maximum case temperature must not exceed 100 °C for reliable operation at 2.8 W. For more information, see the guidelines earlier in this section.

4.2 AC Characteristics

This section contains the AC specifications for the VSC3304 device.

4.2.1 High-Speed Data Inputs

The following table shows the high-speed data inputs.

Table 34. High-Speed Data Inputs

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial NRZ input data rate	DR_{IN}	0		6.5	Gbps	Minimum data rate is limited by the AC-coupling capacitor value (if AC-coupled). Minimum input swing of 200 mV, and maximum case temperature up to 110 °C.
		0		8.5	Gbps	Minimum data rate is limited by the AC-coupling capacitor value (if AC-coupled). Minimum input swing of 600 mV, and maximum case temperature up to 100 °C.
Propagation delay from any input to any output			420		ps	

Table 34. High-Speed Data Inputs *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Output channel-to-channel delay skew	t_{SKEW}		50		ps	

4.2.2 High-Speed Data Outputs

The following table shows the high-speed data outputs.

Table 35. High-Speed Data Outputs

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial NRZ output data rate	DR_{OUT}	0		6.5	Gbps	Minimum data rate is limited by the AC-coupling capacitor value (if AC-coupled). Minimum input swing of 200 mV, and maximum case temperature up to 110 °C.
		0		8.5	Gbps	Minimum data rate is limited by the AC-coupling capacitor value (if AC-coupled). Minimum input swing of 600 mV, and maximum case temperature up to 100 °C.
Serial output data total added random jitter			6	14	ps	Measured peak-to-peak. BER = 10^{-12}.
Serial data output rise time and fall time	$t_{R\text{-}OUT}$, $t_{F\text{-}OUT}$		45	70	ps	20% to 80% with 50 Ω to AC ground (adjustable).

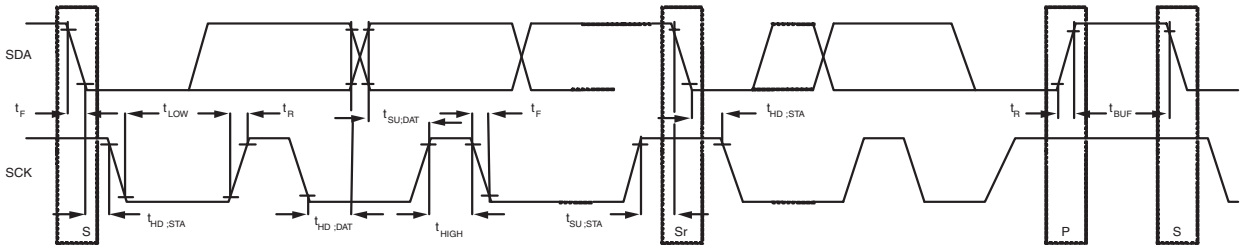
4.2.3 Two-Wire Serial Interface

The following table shows the two-wire serial interface parameters. The illustration provides a two-wire serial interface timing diagram.

Table 36. Two-Wire Serial Interface AC Signal Characteristics

Parameter	Symbol	Minimum	Maximum	Unit
Serial clock	f_{SCK}		400	kHz
Serial I/O	SDA		400	kHz
Hold time START condition after this period, the first CLK pulse is generated	$t_{HD;STA}$	0.6		µs
Low period of SCK	t_{LOW}	1.3		µs
High period of SCK	t_{HIGH}	0.6		µs
Data hold time	$t_{HD;DAT}$	0.09		µs
Data setup time	$t_{SU;DAT}$	100		ns
Rise time of both SDA and SCK	t_R		300	ns
Fall time of both SDA and SCK	t_F		300	ns
Setup time for START	$t_{SU;STA}$	0.6		µs
Bus free time between STOP and START	t_{BUF}	1.3		µs
Maximum bus load for SDA (resistive pull-up)	C_B		200	pF
Maximum bus load for SDA (active pull-up, 3 mA maximum)	C_B		400	pF

Figure 4. Two-Wire Serial Interface Timing Diagram



S = START, P = STOP, and Sr = repeated START.

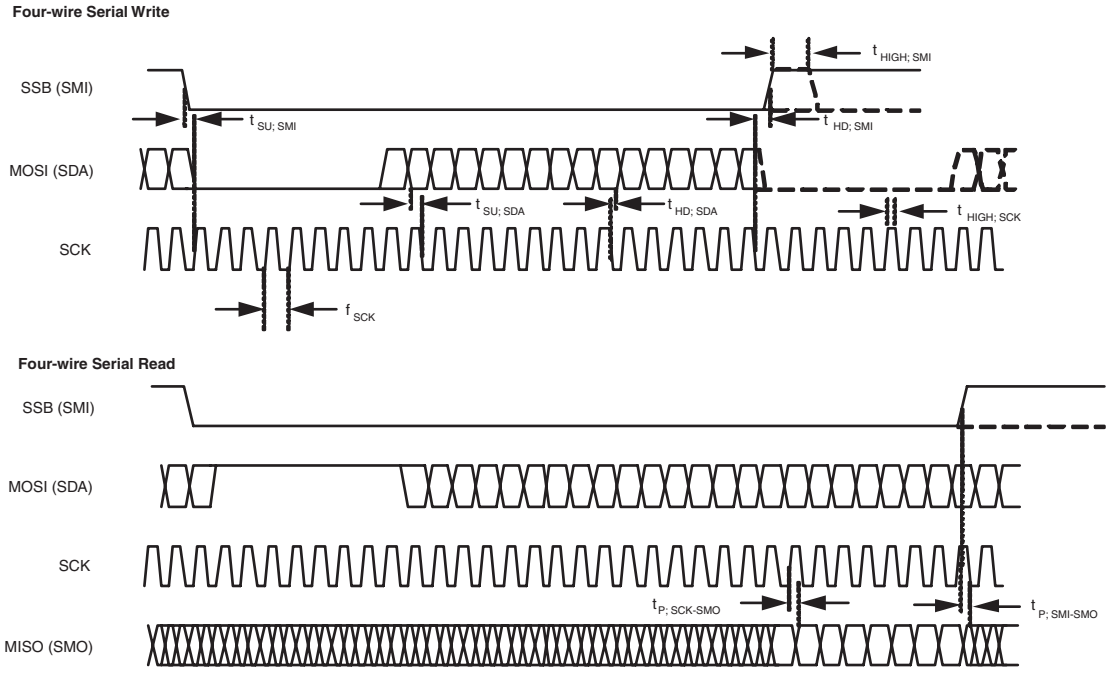
4.2.4 Four-Wire Serial Interface

The section provides information about the four-wire serial interface.

Table 37. Four-Wire Serial Interface AC Signal Characteristics

Parameter	Symbol	Minimum	Maximum	Unit
Serial clock frequency	f_{SCK}		30	MHz
Serial clock minimum pulse width	$t_{HIGH;\ SCK}$	5		ns
SDA setup time to falling edge of SCK	$t_{SU;\ SDA}$	1		ns
SDA hold time to falling edge of SCK	$t_{HD;\ SDA}$	2		ns
SMI setup time to rising edge of SCK	$t_{SU;\ SMI}$	2		ns
Falling SCK in last valid data to rising SMI	$t_{HD;\ SMI}$	100		ns
SMI minimum pulse width	$t_{HIGH;\ SMI}$	5		ns
Rising edge of SCK to SMO propagation delay	$t_{P;\ SCK\text{-}SMO}$	15		ns
Falling edge of SMI to tristate condition of SMO propagation delay	$t_{P;\ SMI\text{-}SMO}$	2		ns
Rise time of all four-wire signals	t_R		3	ns
Fall time of all four-wire signals	t_F		3	ns
Wait time after reset before start of SPI operation	t_{SPI}	600		ns
Rise time of all four-wire signals (maximum rate)	C_B		3	ns
Maximum bus load for MISO			15	pF

Figure 5. Four-Wire Interface Operation



4.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC3304 device.

Table 38. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	2.375	2.5	2.625	V
Power supply voltage, high-speed I/O	V_{DDIO}	2.375 or 3.135	2.5 or 3.3	2.625 or 3.465	V
Operating temperature up to 6.5 Gbps(1)	T	–40		110	°C
Operating temperature up t0 8.5 Gbps(1)	T	–40		100	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

4.4 Stress Ratings

This section contains the stress ratings for the VSC3304 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 39. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for switch core and logic, potential to GND	V_{DD}	–0.5	3.0	V
Power supply voltage for high-speed outputs, potential to GND	V_{DDIO}	–0.5	3.8	V
DC input voltage applied (TTL)		–0.5	V_{DD} + 0.5	V
DC input voltage applied (CML)		–0.5	V_{DDIO} + 0.5	V
Output current	I_{OUT}	–50	50	mA
Storage temperature	T_S	–40	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–750	750	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note(1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge voltage (ESD). Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

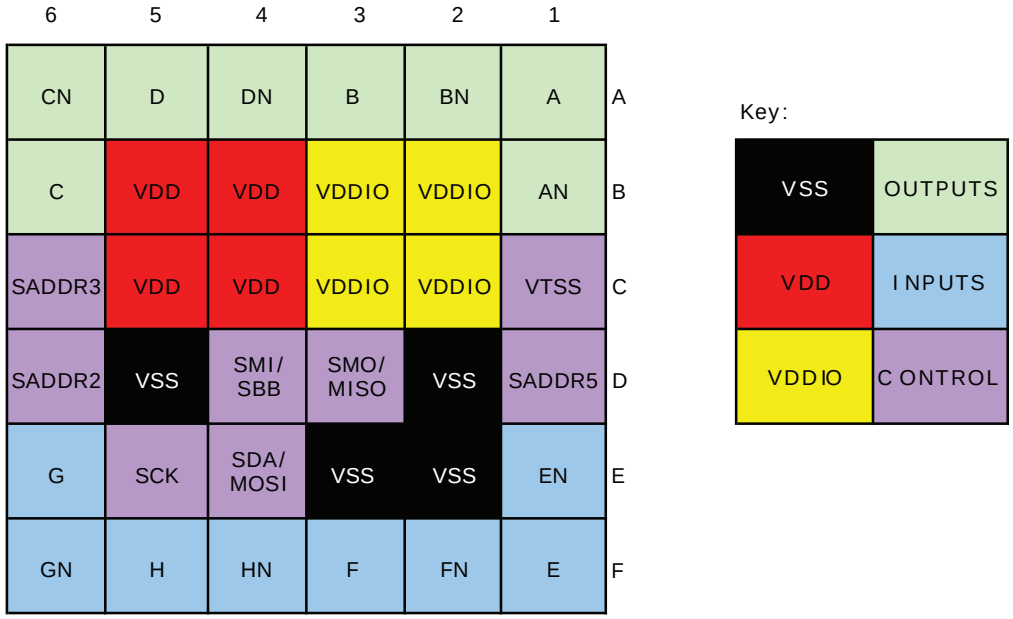
5 Pin Descriptions

This section provides the pin diagram and descriptions for the VSC3304 device.

5.1 Pin Diagram

The following illustration shows the bottom view of the pin diagram for the VSC3304 device.

Figure 6. Pin Diagram



5.2 Pin Identifications

This sections contains the pin descriptions for the VSC3304 device.

5.2.1 High-Speed Data Pins

The following table lists the high-speed data pins for the device.

Table 40. High-Speed Data Pins

Signal Name	Pin Number	Type	Signal Level	Description
E	F1	I or O	CML	Differential port - true
F	F3	I or O	CML	Differential port - true
G	E6	I or O	CML	Differential port - true
H	F5	I or O	CML	Differential port - true

Table 40. High-Speed Data Pins *(continued)*

Signal Name	Pin Number	Type	Signal Level	Description
EN	E1	I or O	CML	Differential port - complement
FN	F2	I or O	CML	Differential port - complement
GN	F6	I or O	CML	Differential port - complement
HN	F4	I or O	CML	Differential port - complement
A	A1	O or I	CML	Differential port - true
B	A3	O or I	CML	Differential port - true
C	B6	O or I	CML	Differential port - true
D	A5	O or I	CML	Differential port - true
AN	B1	O or I	CML	Differential port - complement
BN	A2	O or I	CML	Differential port - complement
CN	A6	O or I	CML	Differential port - complement
DN	A4	O or I	CML	Differential port - complement

5.2.2 Control Pins

The following table lists the control pins for the device.

Table 41. Control Pins

Signal Name	Pin Number	Type	Signal Level	Description
SADDR2	D6	I	LVTTL	Two-wire serial address. Set to zero when not in use. Internal pull-down resistor.
SADDR3	C6	I	LVTTL	Two-wire serial address. Set to zero when not in use. Internal pull-down resistor.
SADDR5	D1	I	LVTTL	Two-wire serial address. Set to zero when not in use. Internal pull-down resistor.
VTSS	C1	I	LVTTL	Reserved pin. Tie to VSS through 1-kΩ resistor.
SCK	E5	I	LVTTL	Serial clock in for two-wire serial bus.
SDA/MOSI	E4	I/O	LVTTL	Serial data port for two-wire serial bus. In four-wire serial mode, this data port acts as the slave input.
SMI/SSB	D4	I	LVTTL	Input for optional proprietary two-wire addressing scheme. In four-wire serial mode, this data port is the serial interface select (active low). Tie to VDD when not in use. Tie to VDD when not in use.
SMO/MISO	D3	O	LVTTL	Output for optional proprietary two-wire addressing scheme. In four-wire serial mode, this data port acts as the slave input.

5.2.3 Power Supplies

The following table lists the power supply pins for the device.

Table 42. Power Supplies

Signal Name	Pin Number	Description
VDD	B4, B5, C4, C5	Power supply for switch core and control logic (2.5 V)
VDDIO	B2, B3, C2, C3	Power supply for high-speed outputs 2.5 V nominal (2.5 V or 3.3 V)
VSS	D2, D5, E2, E3	Ground for VDD and VDDIO

6 Package Information

The VSC3304 device is available in two package types. VSC3304HV is a 36-pin, flip chip ball grid array (FCBGA) with a 7 mm × 7 mm body size, 1 mm pin pitch, and 1.4 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC3304XHV.

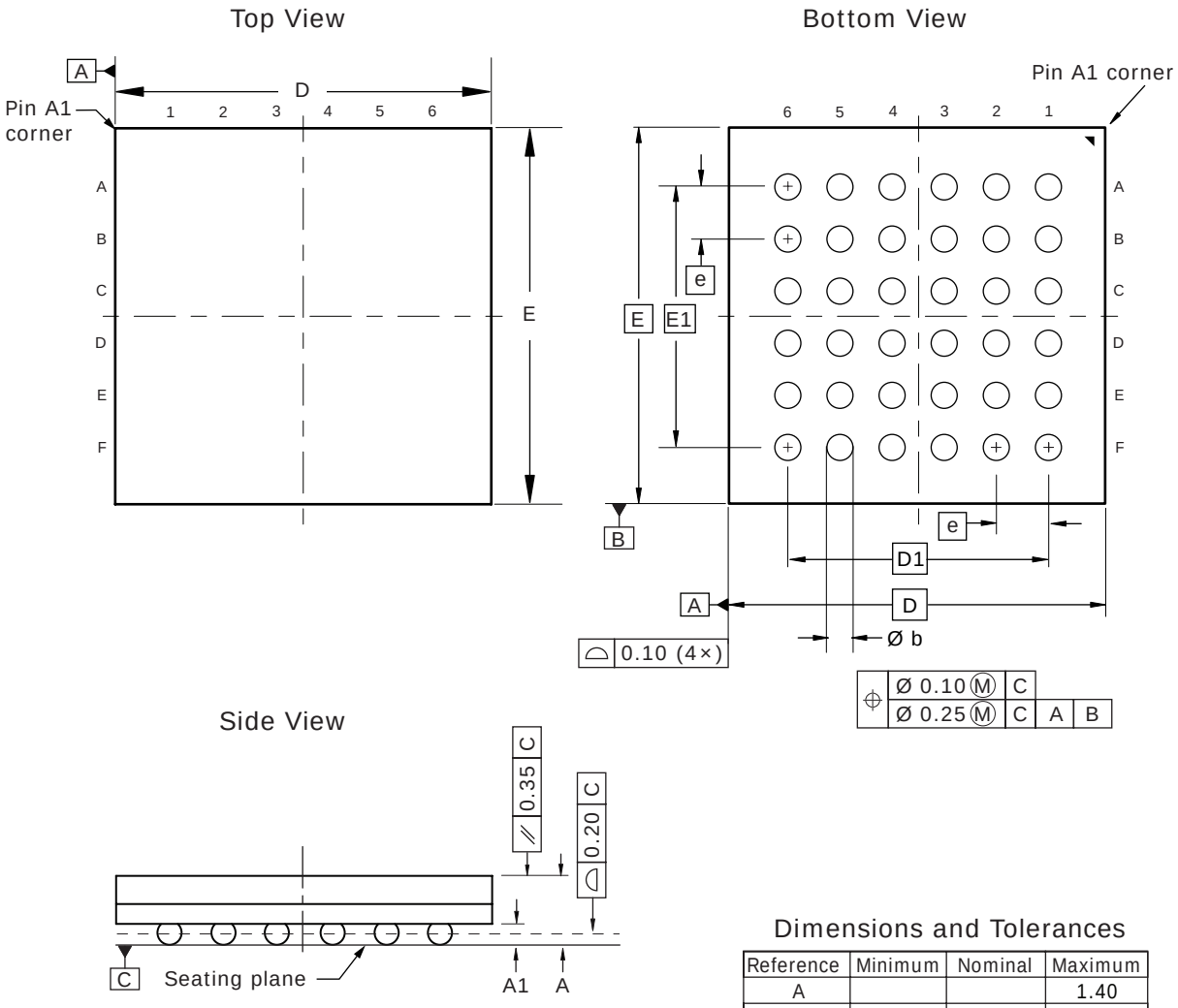
Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC3304 device.

6.1 Package Drawing

The following illustration shows the package drawing for the VSC3304 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 7. Package Drawing



Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			1.40
A1	0.36		0.46
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1		5.00	
E1		5.00	
e		1.00	
b	0.44	0.50	0.64

Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Radial true position is represented by typical values.

6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Vitesse recommends using an external heatsink for higher power level configurations to ensure that the VSC3304 device maintains a case temperature below 110 °C. For information about stress ratings for the device, see Table 39, page 49.

Table 43. Thermal Resistances

			θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	θ_{JB}	**0**	**100**	**200**
VSC3304HV	12.2	28	87	78	72
VSC3304XHV	12.2	28	87	78	72

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

6.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

7 Design Considerations

When using the OOB forwarding with SAS or SATA applications, the burst envelope width becomes distorted beyond compliance at high operating temperatures or at low supply voltage conditions. As a workaround, maintain the case temperature at or below 75 °C, and the V_{DD} power supply between 2.5 VDC and 2.625 VDC to ensure proper OOB forwarding operation.

8 Ordering Information

The VSC3304 device is available in two package types. VSC3304HV is a 36-pin, flip chip ball grid array (FCBGA) with a 7 mm × 7 mm body size, 1 mm pin pitch, and 1.4 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC3304XHV.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC3304 device.

Table 44. Ordering Information

Part Order Number	Description
VSC3304HV	36-pin FCBGA with a 7 mm × 7 mm body size, 1 mm pin pitch, and 1.4 mm maximum height
VSC3304XHV	Lead(Pb)-free (second-level interconnect only), 36-pin FCBGA with a 7 mm × 7 mm body size, 1 mm pin pitch, and 1.4 mm maximum height