155Mbps ATM SAR

General Description

The TC35854AF chip has been designed for use in an Asynchronous Transfer Mode (ATM) User Network Interface (UNI) and Switched Mul-timegabit Data Service (SMDS) Subscriber Net-work Interface (SNI), or a general packet relay interface.

The chip supports the standard UTOPIA interface, and several vendor specific interfaces for connecting to SONET /SDH STS-3c/STM-1, DS3, E3, DS1, and E1 transmission links.

Transmit packets are sent to the TC35854AF chip on a flow-controlled, byte-wide interface. Each packet contains a circuit identifier header. A packet is segmented according to the AAL type specified for that circuit and is placed on a linked-list cell queue in SRAM buffer. Up to 4095 circuits are supported. The cell queues are served by a traffic shaper, which allows CBR, VBR, ABR and UBR traffic.

The TC35854AF chip implements ABR using the explicit rate flow control (ER) ATM Forum UNI 4.0 compliant. Also, the Quantum Flow Control (QFC), FLOWmaster™ flow control and Generic Flow Control (GFC) ITU-T SG13 are supported.

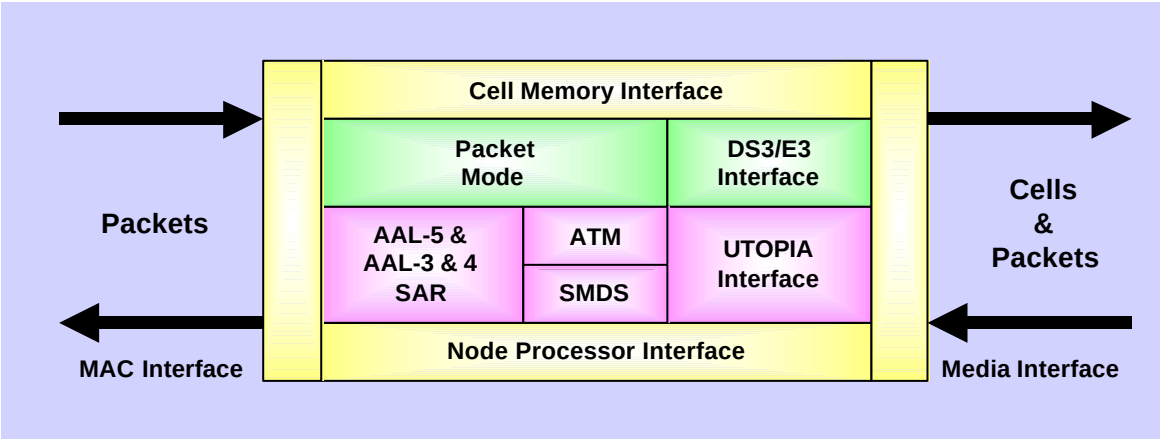
When used on aFLOWmaster™ link or QFC link, all ABR circuits are given equal/fair access to available bandwidth with guaranteed loss-less op-eration.

The TC35854F chip receives cells via the UTOPIA interface. VPI/VCI(MID) fields are then mapped to a local circuit identifier directly. Cells are checked and reassembled on a linked-list cell queue in SRAM buffer. The reassembled packet is moved to one of two packet queues according to the priority set per circuit. All CRCs are also checked. The packets are then passed to the receive MAC inter-face, where a header is attached to identify the as-sociated circuit.

Features

· Full OC3/STM-1 line-rate segmentation and reas-sembly for UTOPIA link
· Up to 4095 VPI/VCI circuits supported and up to 1K MIDs per VPI/VCI circuit
· ABR (ATM Forum UNI 4.0 compliant)
· ITU-I and ATM Forum compliant ATM User Network Interface
· SMDS SIP-2 and SIP-1 (single CPE) according to TR-TSV-000772 and TR-TSV-000773
· AAL3/4 and AAL5 support
· Supports up to 4 CBR VP
· Supports PVC and SVC connections
· Supports F4 and F5 OAM flows
· Traffic shaper supporting peak rate, sustained rate, minimum guaranteed rate, maximum burst size and priority level
· Credit Based flow control (Digital Equipment's FLOWmaster™ and Quantum Flow Control)
· GFC support
· UTOPIA Level 1 compliant media interface
· 32-bit CRC generation and checking for AAL5 and SMDS packets
· Open MAC-style interface for packet transfer up to 200 Mbps
· Two priority packet queues in MAC-style receive interface
· M68000-style node processor interface
· Supporting 1 Megaword (64-bit word) SRAM buffer
· 0.4µm CMOS technology
· 3.3V / 5V dual power supply
· 3.3V and 5V I/O
· 0 - +70 degree temperature range
· 240 pin HQFP package
(body size 32x32 sqmm with 0.5mm pin pitch)

Block Diagram



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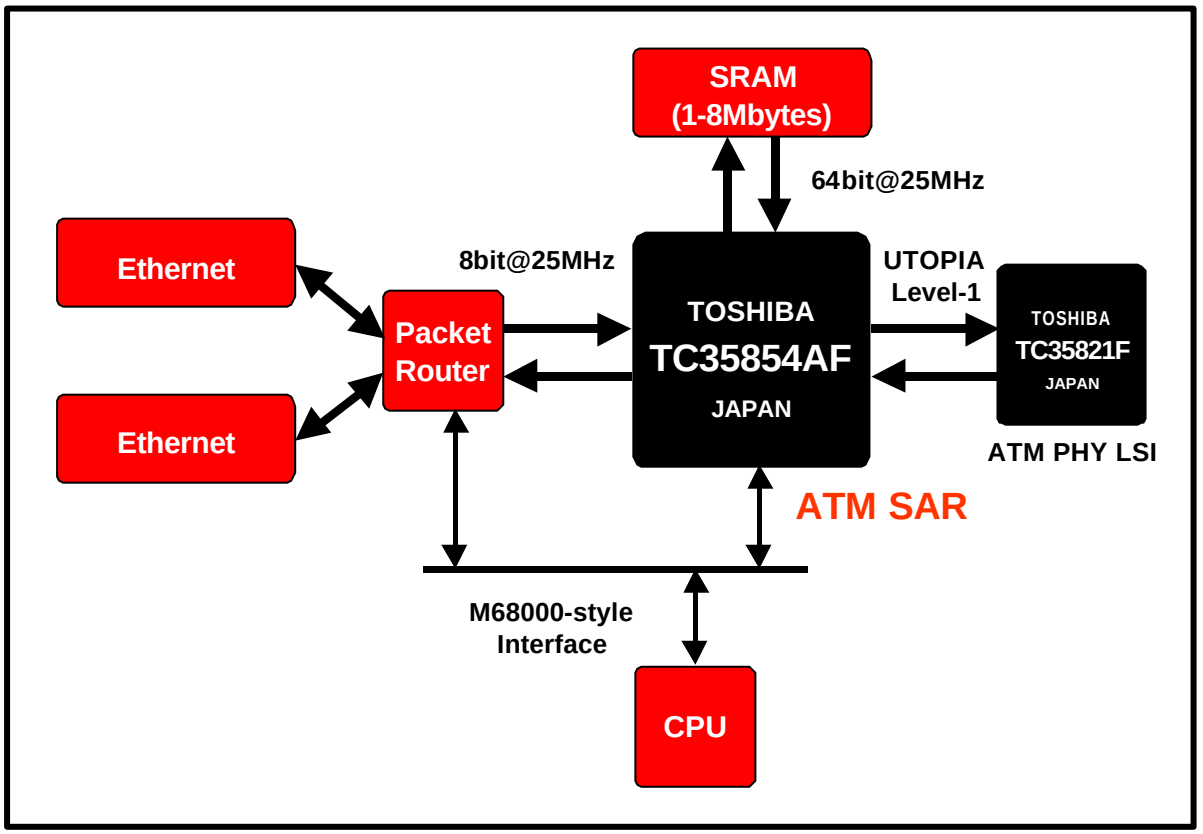
Applications

•High performance ATM switches and Hubs

Application Examples

•This is an Ethernet to ATM Switch system. A packet router between The TC35854AF and Ethernet is developed with a visitor's specification for visitor itself.



CAUTION