

# Octal Bus Buffer

## Inverting

### MC74VHC540

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND-ed active-low output enables. When either  $\overline{OE1}$  or  $\overline{OE2}$  are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 5.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

#### Features

- High Speed:  $t_{PD} = 3.7$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4.0$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 1.2$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

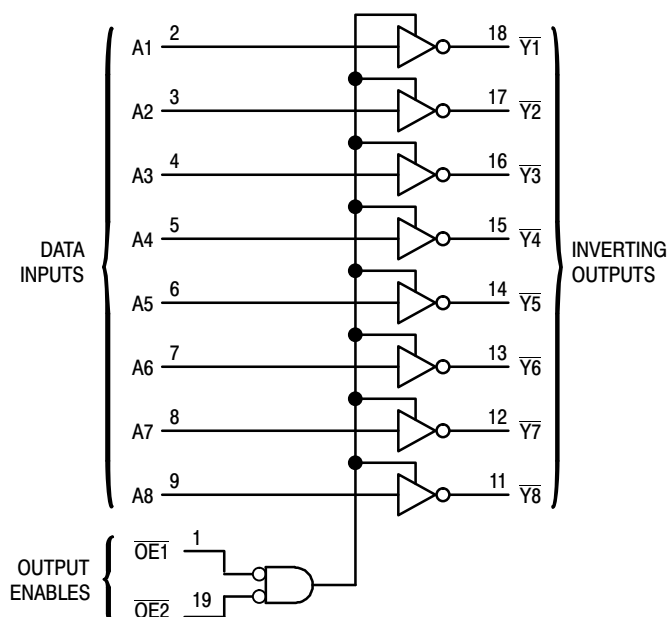


Figure 1. Logic Diagram

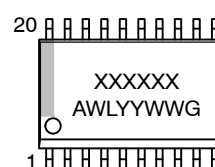


SOIC-20  
DW SUFFIX  
CASE 751D

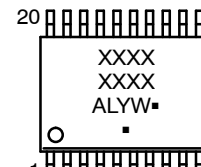


TSSOP-20  
DT SUFFIX  
CASE 948E

#### MARKING DIAGRAMS



SOIC-20



TSSOP-20

- A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT

$\overline{OE1}$	1	20	$V_{CC}$
A1	2	19	$\overline{OE2}$
A2	3	18	$\overline{Y1}$
A3	4	17	$\overline{Y2}$
A4	5	16	$\overline{Y3}$
A5	6	15	$\overline{Y4}$
A6	7	14	$\overline{Y5}$
A7	8	13	$\overline{Y6}$
A8	9	12	$\overline{Y7}$
GND	10	11	$\overline{Y8}$

#### FUNCTION TABLE

Inputs			Output $\overline{Y}$
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# MC74VHC540

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	DC Supply Voltage	−0.5 to +6.5	V	
V <sub>IN</sub>	DC Input Voltage	−0.5 to +6.5	V	
V <sub>OUT</sub>	DC Output Voltage	−0.5 to V <sub>CC</sub> +0.5	V	
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA	
I <sub>OUT</sub>	DC Output Current, Per Pin	±25	mA	
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA	
I <sub>IK</sub>	Input Clamp Current	−20	mA	
I <sub>OK</sub>	Output Clamp Current	±20	mA	
T <sub>STG</sub>	Storage Temperature Range	−65 to +150	°C	
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C	
θ <sub>JA</sub>	Thermal Resistance (Note 1)	SOIC−20W TSSOP−20	96 150	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25°C	SOIC−20W TSSOP−20	1302 833	mW
MSL	Moisture Sensitivity	SOIC−20W All Other Packages	Level 3 Level 1	–
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.540 in	–
V <sub>ESD</sub>	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V
I <sub>LATCHUP</sub>	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	DC Input Voltage (Note 4)	0	5.5	V
V <sub>OUT</sub>	DC Output Voltage (Note 4)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	−55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	V <sub>CC</sub> = 3.0 V to 3.6 V V <sub>CC</sub> = 4.5 V to 5.5 V	0 100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

# MC74VHC540

## DC ELECTRICAL CHARACTERISTICS (MC74VHC540)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 55 to 125°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7			1.50 V <sub>CC</sub> × 0.7		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V <sub>CC</sub> × 0.3		0.50 V <sub>CC</sub> × 0.3	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 4 mA I <sub>OH</sub> = - 8 mA	3.0 4.5	2.58 3.94			2.48 3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5			±0.25		±2.5	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74VHC540

## AC ELECTRICAL CHARACTERISTICS (MC74VHC540)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = – 55 to 125°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to $\bar{Y}$ (Figures 1 and 3)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		4.8 7.3	7.0 10.5	1.0 1.0	8.5 12.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		3.7 5.2	5.0 7.0	1.0 1.0	6.0 8.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OEn to $\bar{Y}$ (Figures 2 and 4)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OEn to $\bar{Y}$ (Figures 2 and 4)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 50 pF		11.2	15.4	1.0	17.5	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 50 pF		6.0	8.8	1.0	10.0	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 50 pF (Note 5)			1.5			ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50 pF (Note 5)			1.0			ns
C <sub>in</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High Impedance State)			6				pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		17	

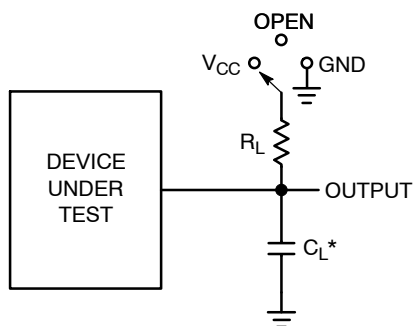
5. Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> – t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> – t<sub>PHLn</sub>|.

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (MC74VHC540)

Symbol	Parameter	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.9	1.2	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	–0.9	–1.2	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		3.5	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		1.5	V

MC74VHC540



\*C<sub>L</sub> Includes probe and jig capacitance  
Input signal t<sub>R</sub> = t<sub>F</sub> = 3 ns

Test	Switch Position	C <sub>L</sub>	R <sub>L</sub>
t <sub>PLH</sub> / t <sub>PHL</sub>	Open	See AC Characteristics Table	1 kΩ
t <sub>PLZ</sub> / t <sub>PZL</sub>	V <sub>CC</sub>		
t <sub>PHZ</sub> / t <sub>PZH</sub>	GND		

Figure 2. Test Circuits

SWITCHING WAVEFORMS

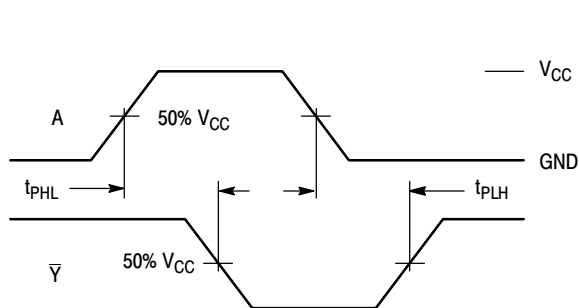


Figure 3.

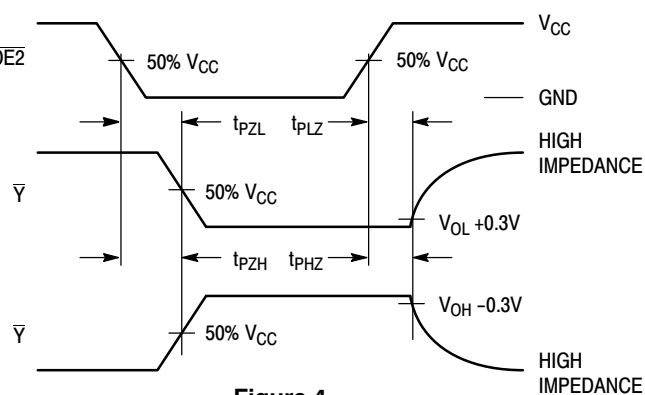


Figure 4.

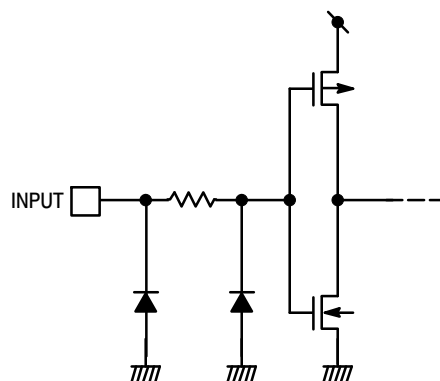


Figure 5. Input Equivalent Circuit

## MC74VHC540

### ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74VHC540DWR2G	VHC540G	SOIC-20 WB	1000 / Tape & Reel
MC74VHC540DTR2G	VHC 540	TSSOP-20	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

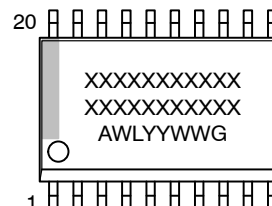


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

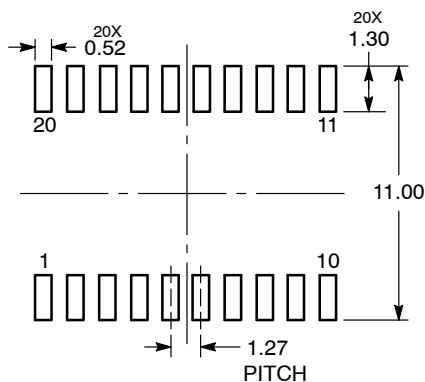
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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