SC1110
Sink and Source DC/DC Controller for Termination Power Supply Applications

POWER MANAGEMENT

Description

The SC1110 is a low-cost, full featured, synchronous voltage-mode controller designed to generate termination voltage in double data rate (DDR) memory systems and other applications where wide data bus need to be actively terminated. Synchronous control of the MOSFET half bridge allows power flowing bi-directionally. The termination voltage can be tightly regulated to track the chipset voltage, i.e. to be exactly 50% of that at all times.

The SC1110 is ideal for low cost implementation of termination voltage supplies. SC1110 features include temperature compensated voltage reference, triangle wave oscillator and current sense comparator circuitry, and allows the use of inexpensive N-channel power MOSFETs.

The SC1110 operates at a fixed 250kHz, providing an optimum compromise between efficiency, transient performance, external component size, and cost.

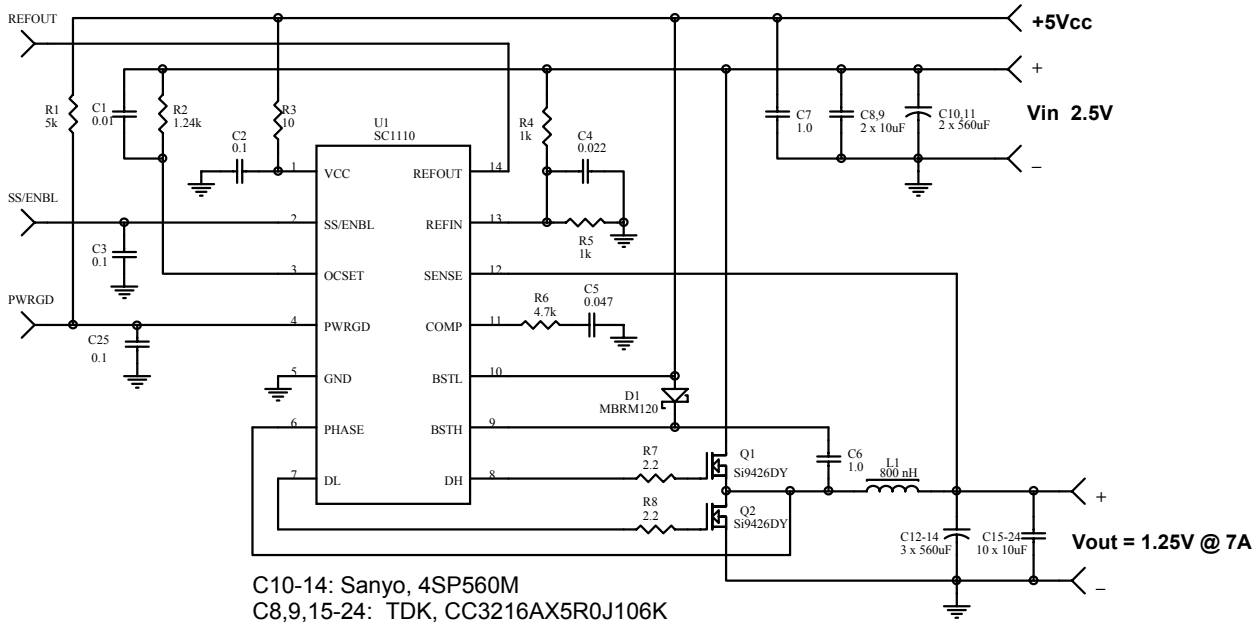
Features

- Generates termination voltages for active termination schemes
- 1% set point accuracy
- For ±7A output current, transient regulation is better than ±80mV
- V_{REFIN} pin available for external 50% resistive divider to allow termination voltage track of the chip set voltage
- Buffered V_{REFOUT} for system usage
- R_{DSON} sensing for over current protection in hiccup mode
- Soft start and logic input enabling
- 250kHz switching for best transient and efficiency performance
- Gate drive capable for 0.5A sourcing and sinking

Applications

- For DDR memory systems
- For active termination schemes in high speed logic systems

Typical Application Circuit



C10-14: Sanyo, 4SP560M
C8,9,15-24: TDK, CC3216AX5R0J106K
L1: Panasonic, ETQP6F0R8L or Falco, QPIP1205-809-3
Q1,Q2 options: Si9426DY, FDS6890A, IRF7401
D1: ON Semi (Motorola)

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
V_{CC}, BSTL to GND	V_{IN}	-0.5 to 14	V
PGND to GND		+0.5	V
PHASE to GND		-0.3 to 18	V
BSTH to PHASE		14	V
Thermal Impedance Junction to Case	θ_{JC}	45	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	115	°C/W
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	V_{ESD}	2	kV

Electrical Characteristics

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Power Supply					
Supply Voltage	V_{CC}	4.4		12.6	V
Supply Current			8	12	mA
Line Regulation	V_O = 2.5V ± 0.5V, V_O = V_{IN}/2 @ 0A		0.5		%
Under Voltage Lockout					
Turn-On Threshold			4.15		V
Turn-Off Threshold			3.95		V
Error Amplifier					
Transconductance			2		mS
Open Loop DC Gain			50		dB
Bandwidth - 3dB	(Unity gain crossover 70MHz)		500		kHz
COMP Source Capability			±250		µA
Input Bias			2	5	µA
Oscillator					
Oscillator Frequency		225	250	275	kHz
Oscillator Max Duty Cycle		90	95		%
Ramp Height			1		V

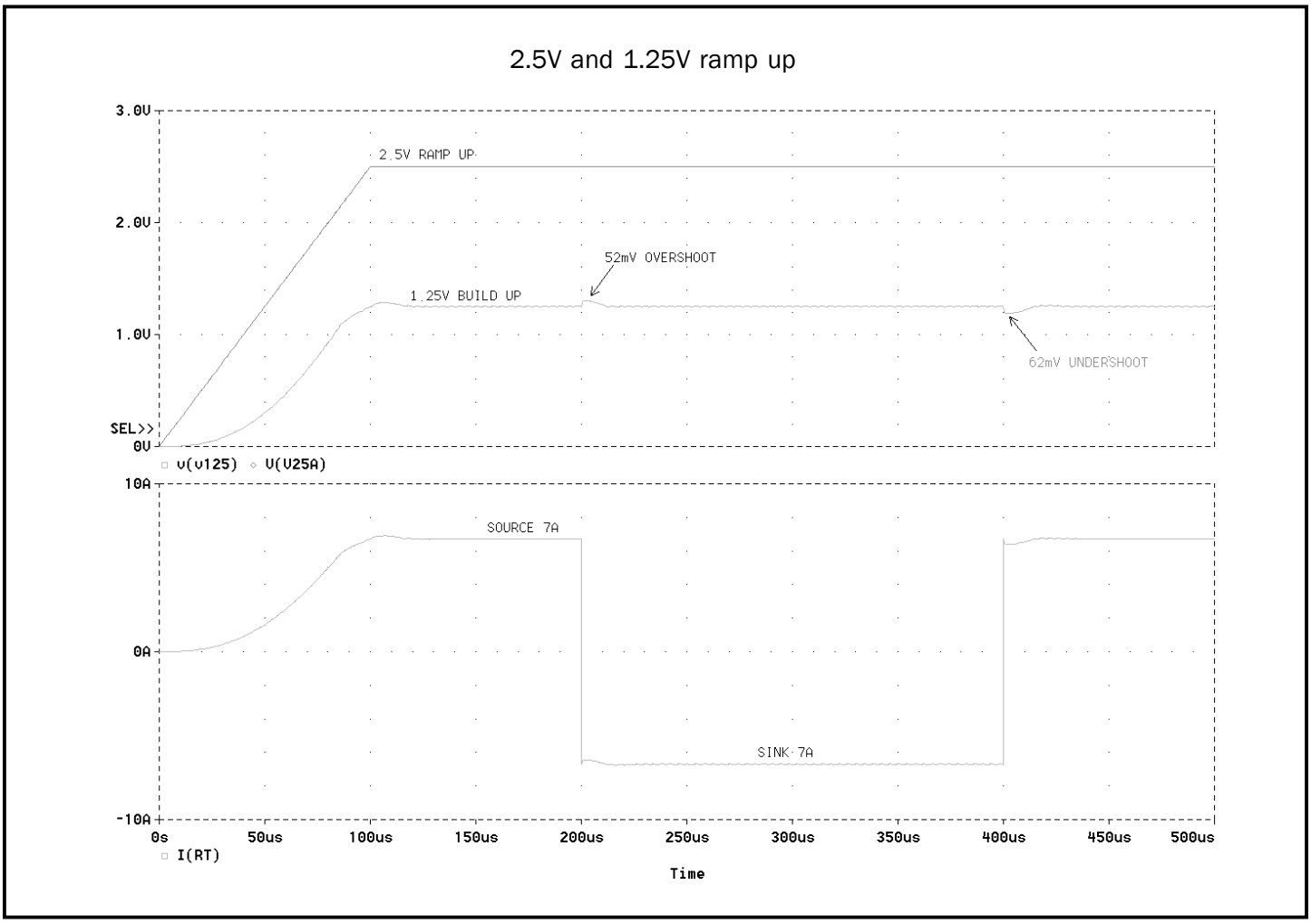
Electrical Characteristics (Cont.)

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Timing					
Minimum Off-Time			200		ns
Dead Time	Guaranteed by characterization	80			ns
MOSFET Drivers					
Peak DH Sink/Source Current	BSTH - DH = 4.5V, DH - PHASE = 3.0V	0.5			A
	DH - PHASE = 1.5V	0.1			
Peak DL Sink/Source Current	BSTL - DL = 4.5V, DL - GND = 3.0V	0.5			A
	DL - GND = 1.5V	0.1			
Protection					
Overcurrent Set Isource	V_{OCSET} = 2.2V	180	200	220	µA
Soft Start					
Charge Current	V_{SS} = 1.5V	8	10	12	µA
Discharge Current	V_{SS} = 1.5V	1	2	3	µA
Power Good					
Upper Threshold			112		%
Lower Threshold			88		%
PWRGD Voltage Low	I_{PWRGD} = 2mA			0.5	V
Reference					
REFOUT Source Current			3		mA
Offset	REF_{IN} = 1.25V	-5		5	mV
Enable					
Threshold		0.55	0.60	0.65	V

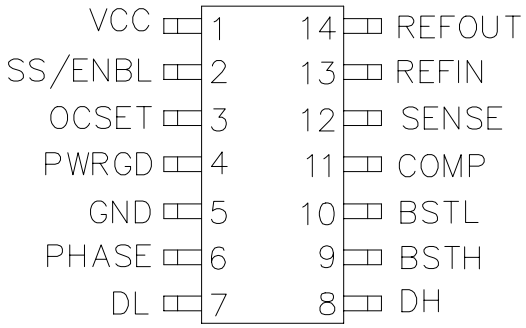
Timing Diagrams

SIMULATION WAVEFORMS



Output current of the VTT supply

Pin Configuration



(14 Pin SOIC or TSSOP)

Ordering Information

Device (1)	Package(1)(2)	Temp Range (T_J)
SC1110CSTRT	SO-14	0° to 125°C
SC1110TSTRT	TSSOP-14	

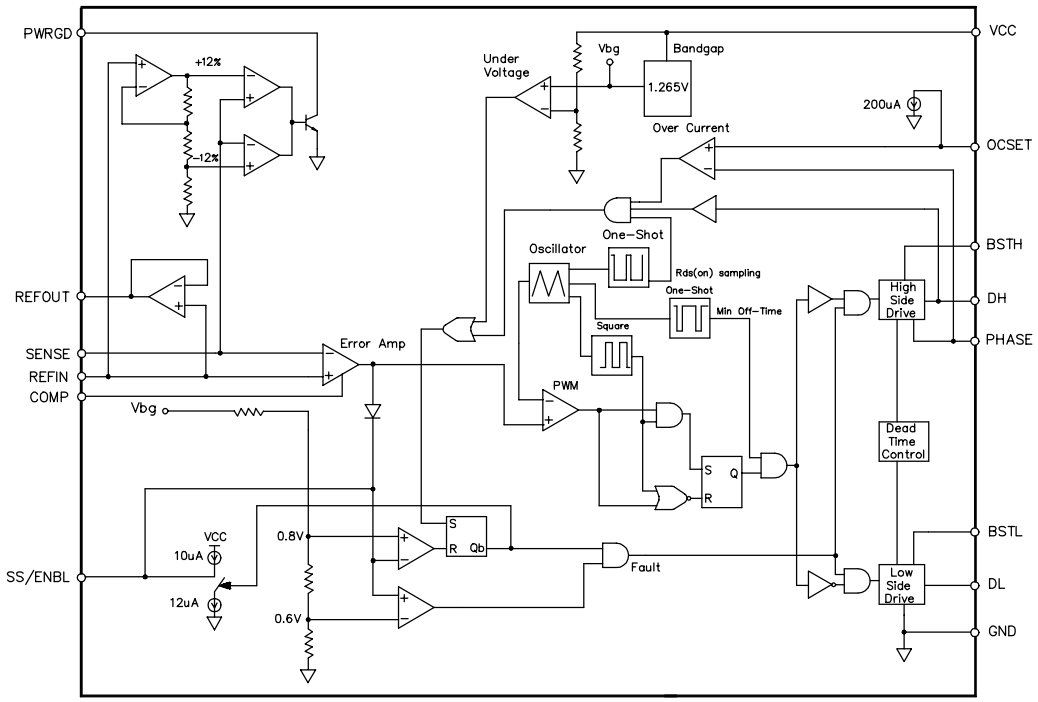
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	VCC	Chip Supply Voltage.
2	SS/ENBL	Soft start/Enable.
3	OCSET	Current limit set point.
4	PWRGD	Logic high indicates correct output.
5	GND	Ground.
6	PHASE	Phase node connection between MOSFETs.
7	DL	Low side driver output.
8	DH	High side driver output.
9	BSTH	High side driver supply.
10	BSTL	Low side driver supply.
11	COMP	Error amplifier output, compensation.
12	SENSE	Error amplifier negative input.
13	REFIN	Error amplifier positive input.
14	REFOUT	Buffered reference voltage.

NOTE:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Applications Information

THEORY OF OPERATION

Synchronous Buck Converter

$V_{TERMINATION}$ power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter for termination of power application.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider generates reference voltage for the error amplifier from the chipset voltage which is usually 2.5V. The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 250kHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the PWM comparator. The non-inverting input of the comparator receives it's input voltage from the error amplifier. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the SC1110 assures that both the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Applications Information

Soft Start

Initially, SS/ENABLE sources 10µA of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on SS/ENABLE. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

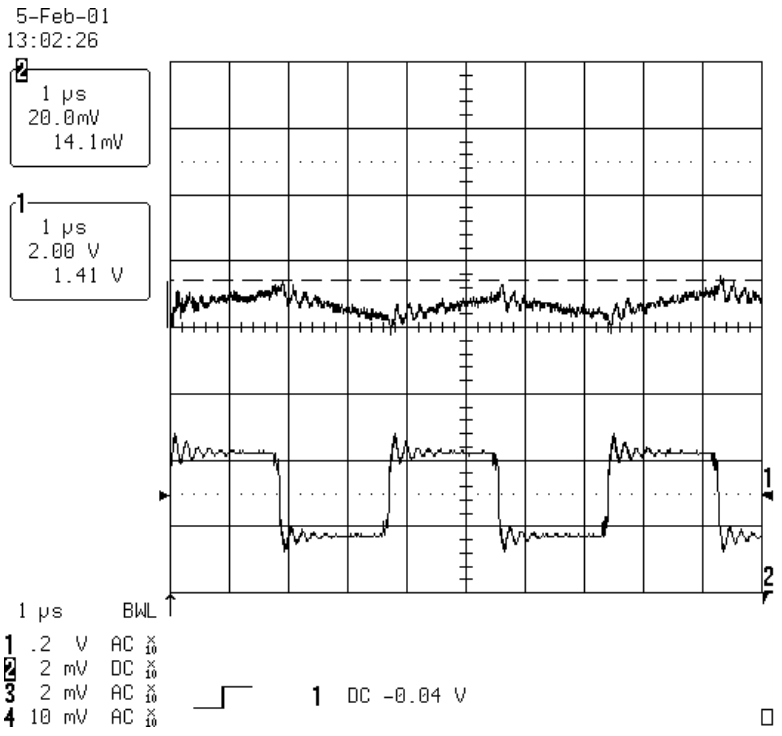
$R_{DS(ON)}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the V_{CC} supply to OCSET. The voltage drop across this resistor is due to the 200µA internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFET's off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switcher turns off and SS/ENABLE starts to sink 2µA. When SS/ENABLE reaches 0.8V, it then starts to source 10µA and a new cycle begins.

Hiccup Mode

During power up, the SS/ENABLE pin is internally pulled low until VCC reaches the undervoltage lockout level of 4.2V. Once V_{CC} has reached 4.2V, the SS/ENABLE pin is released and begins to source 10µA of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of 250 kHz, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about 2.2V.

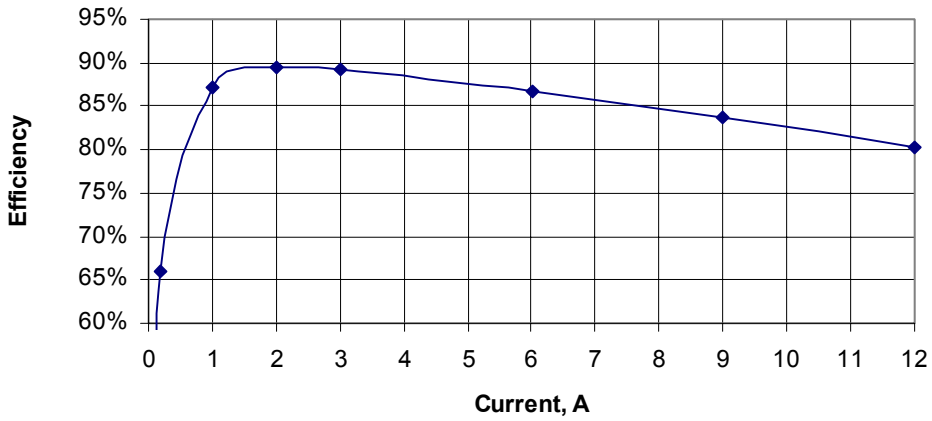
Typical Characteristics

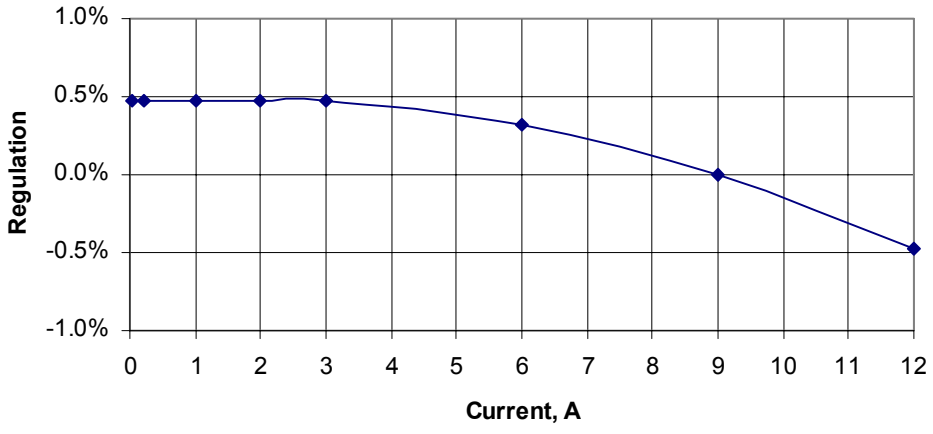


CH1: Vout_ripple

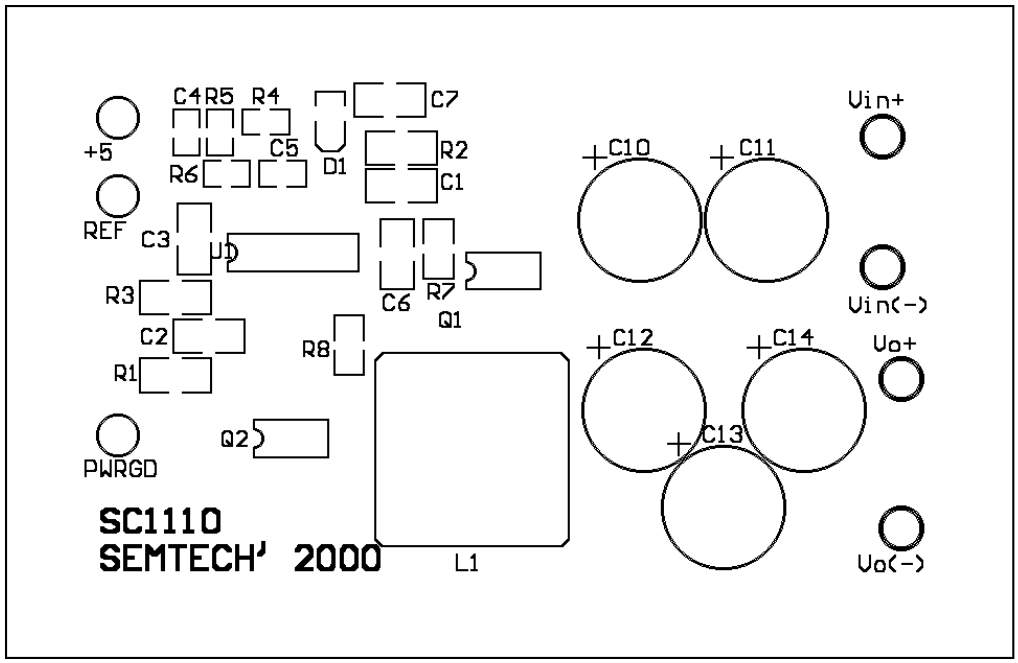
CH2: Phase node

Vin = 2.5V
Vout = 1.25V
Iout = 7A

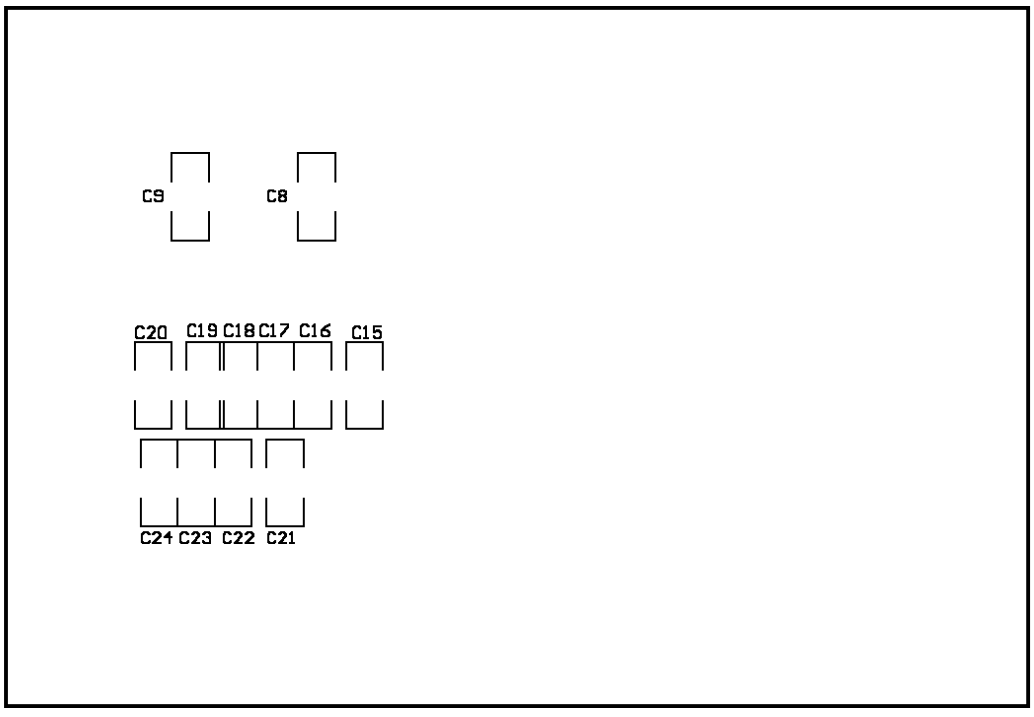




Top View

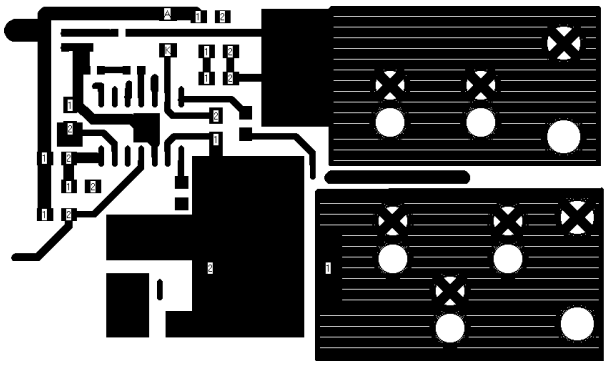


Bottom View

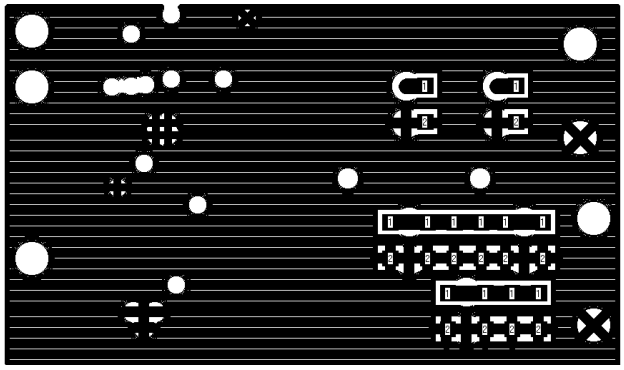


Evaluation Board (Cont.)

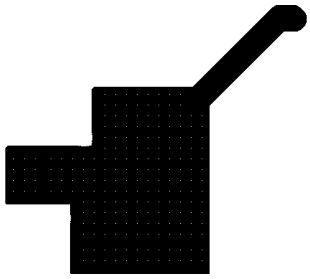
Top Copper



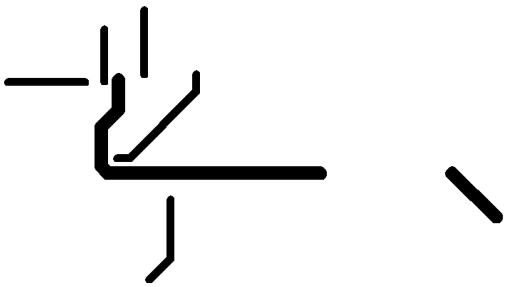
Bottom Copper



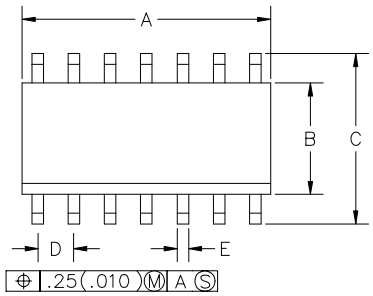
Midlayer 1



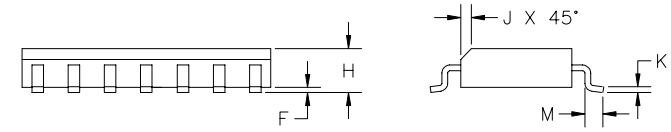
Midlayer 2



Outline Drawing - SO-14



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.337	.344	8.55	8.75	2
B	.150	.158	3.80	4.00	3
C	.228	.244	5.80	6.20	
D	.050 BSC		1.27 BSC		
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.010	.020	0.25	0.50	
K	.007	.010	.19	.25	
M	.016	.050	0.40	1.27	

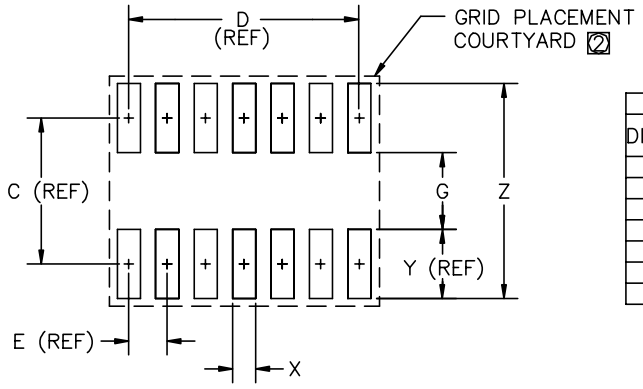


[3] DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.

[2] DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.

[1] CONTROLLING DIMENSION : MILLIMETER

Land Pattern - SO-14

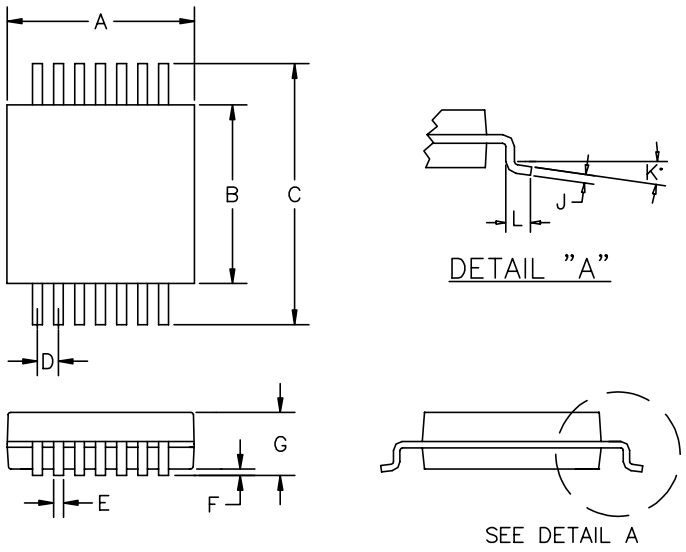


DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.30	–	7.62	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

[2] GRID PLACEMENT COURTYARD IS 20x16 ELEMENTS (10mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

[1] CONTROLLING DIMENSION: MILLIMETERS

Outline Drawing - TSSOP-14



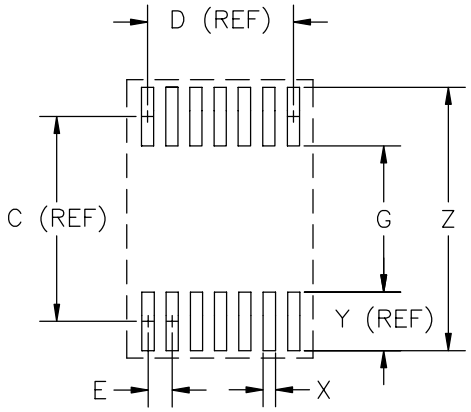
DIMENSIONS (1)					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.193	.201	4.90	5.10	(2)
B	.169	.177	4.30	4.50	(2)
C	.252 BSC		6.40 BSC		–
D	.026 BSC		.65 BSC		–
E	.007	.012	.19	.30	–
F	.002	.006	.05	.15	–
G		.047		1.20	–
J	.004	.008	.09	.20	–
K	0°	8°	0°	8°	–
L	.018	.030	.45	.75	–

JEDEC MO-153AB1

(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-14



DIMENSIONS (1)					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.218	–	5.53	REF
D	–	.156	–	3.96	REF
E	–	.026	–	0.65	BSC
G	.155	–	3.947	–	–
X	–	.013	–	0.323	REF
Y	–	.062	–	1.583	–
Z	–	.280	–	7.113	–

(2) GRID PLACEMENT COURTYARD IS 10 X 15 ELEMENTS (5mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

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