74HC9114; 74HCT9114

Nine wide Schmitt trigger buffer; open drain outputs; inverting

Rev. 5 — 5 August 2024 Product data sheet

1. General description

The 74HC9114; 74HCT9114 is a 9-bit inverter with Schmitt trigger inputs and open drain outputs. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}. Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

2. Features and benefits

- Wide operating voltage 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Unlimited input rise and fall times
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC9114D 74HCT9114D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Functional diagram

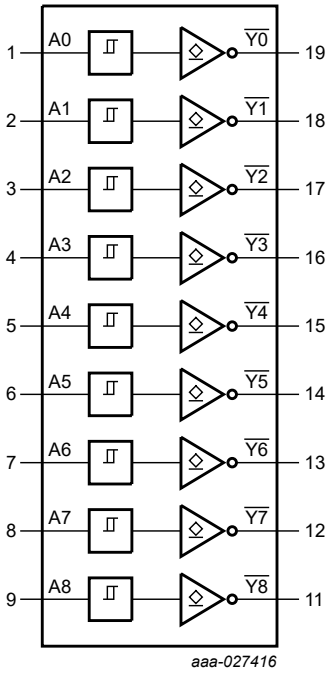


Fig. 1. Logic symbol

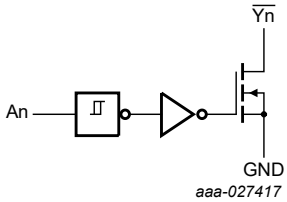
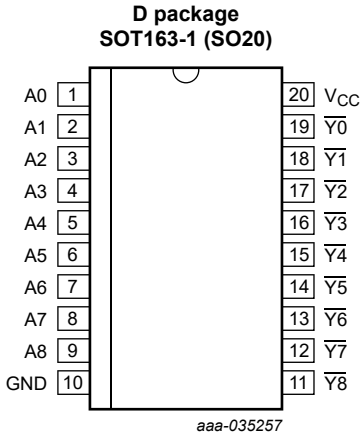


Fig. 2. Logic diagram (one Schmitt trigger)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2, A3, A4, A5, A6, A7, A8	1, 2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
$\overline{Y0}$, $\overline{Y1}$, $\overline{Y2}$, $\overline{Y3}$, $\overline{Y4}$, $\overline{Y5}$, $\overline{Y6}$, $\overline{Y7}$, $\overline{Y8}$	19, 18, 17, 16, 15, 14, 13, 12, 11	data output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Output
An	**$\overline{Yn}$**
L	Z
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5$ V	[1]	-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC9114			74HCT9114			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC9114										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT9114										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 4.5 V								
		I_O = 20 µA;	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA;	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per An input pin; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND	-	30	108	-	135	-	147	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

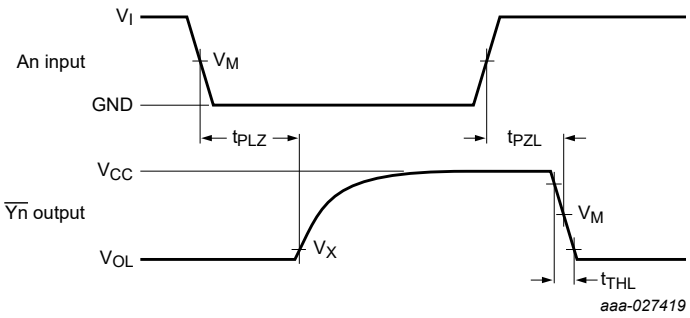
GND = 0 V; C_L = 50 pF; for test circuit see Fig. 4.

Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC9114										
t_{pd}	propagation delay	An to $\overline{Yn}$; see Fig. 3 [1]								
		V_{CC} = 2.0 V	-	36	110	-	140	-	165	ns
		V_{CC} = 4.5 V	-	13	22	-	28	-	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	10	19	-	24	-	28	ns
t_{THL}	HIGH to LOW output transition time	$\overline{Yn}$; see Fig. 3								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [2]	-	5	-	-	-	-	-	pF
74HCT9114										
t_{pd}	propagation delay	An to $\overline{Yn}$; see Fig. 3 [1]								
		V_{CC} = 4.5 V	-	17	31	-	39	-	47	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
t_{THL}	HIGH to LOW output transition time	$\overline{Yn}$; V_{CC} = 4.5 V; see Fig. 3	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} - 1.5 V [2]	-	5	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLZ} and t_{PZL}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



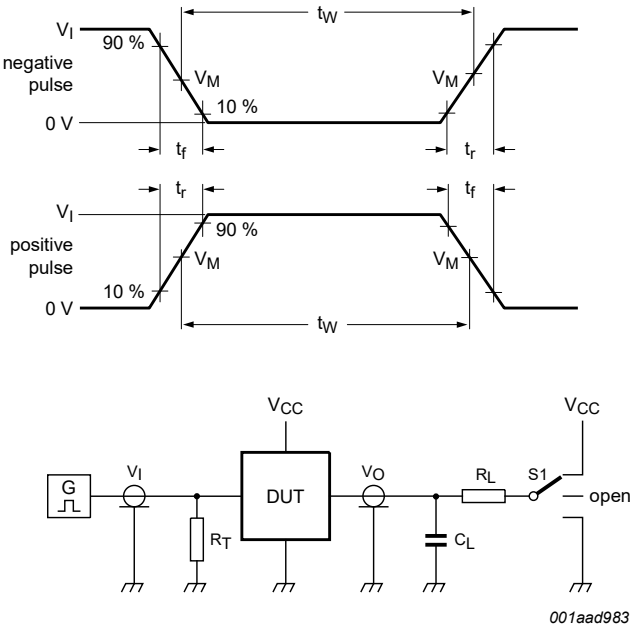
Measurement points are given in Table 8 .

V_{OL} is a typical voltage output level that occurs with the output load.

Fig. 3. Input to output propagation delays and HIGH to LOW output transition time

Table 8. Measurement points

Type	Input	Output	
	V_M	V_M	V_X
74HC9114	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}
74HCT9114	1.3 V	1.3 V	0.1 × V_{CC}



Test data is given in Table 9 .

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

Fig. 4. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position	
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZL}, t_{PLZ}
74HC9114	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	V_{CC}
74HCT9114	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	V_{CC}

11. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC9114										
V_{T+}	positive-going threshold voltage	V_{CC} = 2.0 V	0.70	1.13	1.50	0.70	1.50	0.70	1.50	V
		V_{CC} = 4.5 V	1.75	2.37	3.15	1.75	3.15	1.75	3.15	V
		V_{CC} = 6.0 V	2.30	3.11	4.20	2.30	4.20	2.30	4.20	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.0 V	0.30	0.70	1.10	0.30	1.10	0.30	1.10	V
		V_{CC} = 4.5 V	1.35	1.80	2.40	1.35	2.40	1.35	2.40	V
		V_{CC} = 6.0 V	1.8	2.43	3.30	1.80	3.30	1.80	3.30	V
V_H	hysteresis voltage	V_{CC} = 2.0 V	0.2	0.43	0.80	0.18	0.80	0.15	0.80	V
		V_{CC} = 4.5 V	0.4	0.57	1.00	0.40	1.00	0.40	1.00	V
		V_{CC} = 6.0 V	0.5	0.68	1.10	0.50	1.10	0.50	1.10	V
74HCT9114										
V_{T+}	positive-going threshold voltage	V_{CC} = 4.5 V	0.9	1.50	2.0	0.9	2.0	0.9	2.0	V
		V_{CC} = 5.5 V	1.2	1.70	2.1	1.2	2.1	1.2	2.1	V
V_{T-}	negative-going threshold voltage	V_{CC} = 4.5 V	0.7	1.06	1.4	0.7	1.4	0.7	1.4	V
		V_{CC} = 5.5 V	0.8	1.27	1.7	0.8	1.7	0.8	2.7	V
V_H	hysteresis voltage	V_{CC} = 4.5 V	0.2	0.44	0.8	0.2	0.8	0.2	0.8	V
		V_{CC} = 5.5 V	0.2	0.44	0.8	0.2	0.8	0.2	0.8	V

11.1. Transfer characteristics waveforms

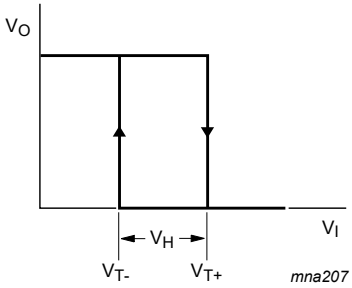


Fig. 5. Transfer characteristics

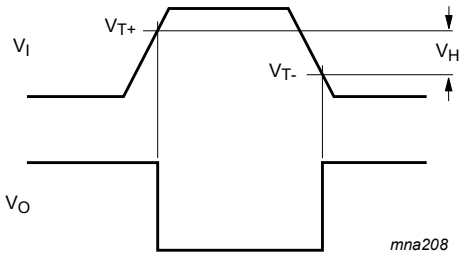
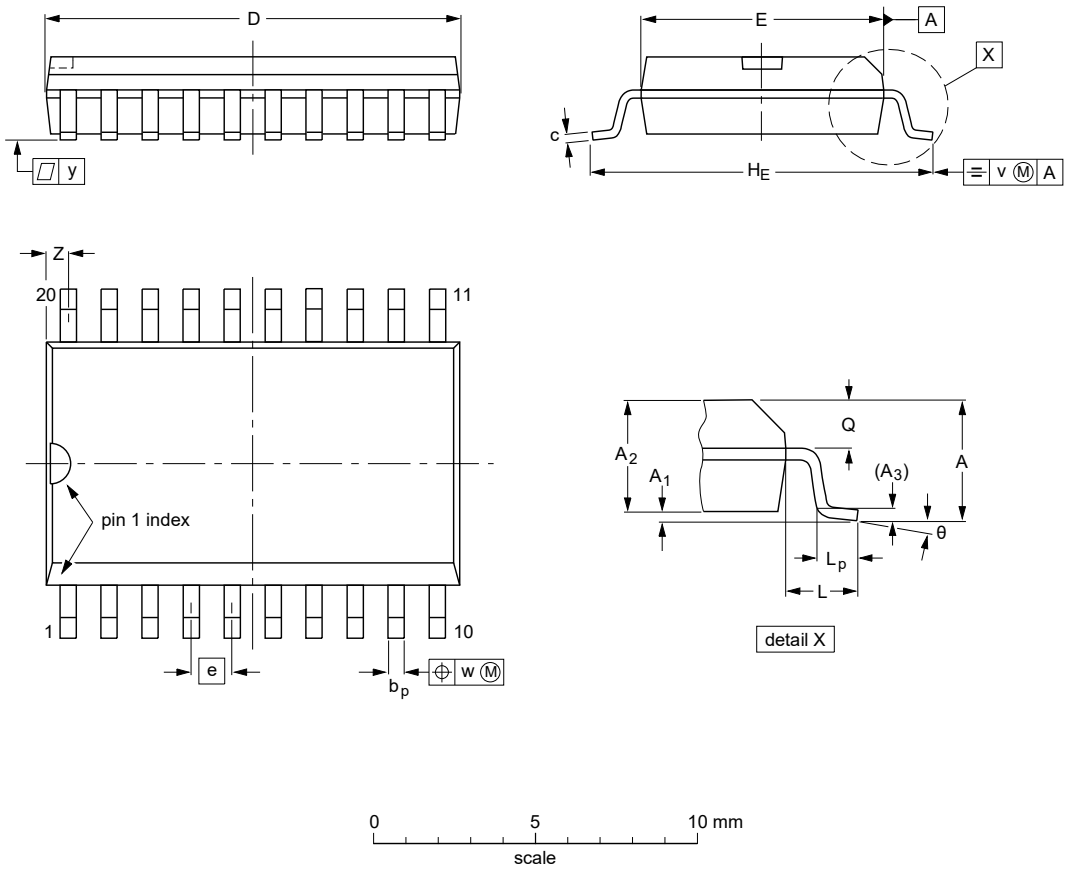


Fig. 6. Transfer characteristics definitions

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT163-1 (SO20)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT9114 v.5	20240805	Product data sheet	-	74HC_HCT9114 v.4
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT9114 v.4	20231109	Product data sheet	-	74HC_HCT9114 v.3
Modifications:	• Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT9114 v.3	20171002	Product data sheet	-	74HC_HCT9114 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT9114 v.2	19901201	Product specification	-	74HC_HCT9114 v.1
74HC_HCT9114 v.1	19880301	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 5 August 2024