

# GTL2008

**12-bit GTL to LVTTL translator with power good control and high-impedance LVTTL and GTL outputs**

Rev. 04 — 19 February 2010

Product data sheet

## 1. General description

The GTL2008 is a customized translator between dual Xeon processors, Platform Health Management, South Bridge and Power Supply LVTTL and GTL signals.

Functionally and footprint identical to the GTL2007, the GTL2008 LVTTL and GTL outputs were changed to put them into a high-impedance state when EN1 and EN2 are LOW, with the exception of 11BO because its normal state is LOW, so it is forced LOW. EN1 and EN2 will remain LOW until  $V_{CC}$  is at normal voltage, the other inputs are in valid states and VREF is at its proper voltage to assure that the outputs will remain high-impedance through power-up.

The GTL2008 has the enable function that disables the error output to the monitoring agent for platforms that monitor the individual error conditions from each processor. This enable function can be used so that false error conditions are not passed to the monitoring agent when the system is unexpectedly powered down. This unexpected power-down could be from a power supply overload, a CPU thermal trip, or some other event of which the monitoring agent is unaware.

A typical implementation would be to connect each enable line to the system power good signal or the individual enables to the VRD power good for each processor.

Typically Xeon processors specify a  $V_{TT}$  of 1.1 V to 1.2 V, as well as a nominal  $V_{ref}$  of 0.73 V to 0.76 V. To allow for future voltage level changes that may extend  $V_{ref}$  to 0.63 or  $V_{TT}$  (minimum of 0.693 V with  $V_{TT}$  of 1.1 V) the GTL2008 allows a minimum  $V_{ref}$  of 0.66 V. Characterization results show that there is little DC or AC performance variation between these  $V_{ref}$  levels.

## 2. Features and benefits

- Operates as a GTL to LVTTL sampling receiver or LVTTL to GTL driver
- Operates at GTL-/GTL/GTL+ signal levels
- EN1 and EN2 disable error output
- All LVTTL and GTL outputs are put in a high-impedance state when EN1 and EN2 are LOW
- 3.0 V to 3.6 V operation
- LVTTL I/O not 5 V tolerant
- Series termination on the LVTTL outputs of  $30\ \Omega$
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101



- Latch-up testing is done to JEDEC Standard JESD78 Class II, Level A which exceeds 500 mA
- Package offered: TSSOP28

### 3. Quick reference data

**Table 1. Quick reference data**

$T_{amb} = 25 \text{ }^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{io}$	input/output capacitance	A port; $V_O = 3.0 \text{ V}$ or $0 \text{ V}$	-	2.5	3.5	pF
		B port; $V_O = V_{TT}$ or $0 \text{ V}$	-	1.5	2.5	pF
<b><math>V_{ref} = 0.73 \text{ V}; V_{TT} = 1.1 \text{ V}</math></b>						
$t_{PLH}$	LOW to HIGH propagation delay	nA to nBI; see <a href="#">Figure 4</a>	1	4	8	ns
		nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a>	2	13	18	ns
$t_{PHL}$	HIGH to LOW propagation delay	nA to nBI; see <a href="#">Figure 4</a>	2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a>	2	4	10	ns
<b><math>V_{ref} = 0.76 \text{ V}; V_{TT} = 1.2 \text{ V}</math></b>						
$t_{PLH}$	LOW to HIGH propagation delay	nA to nBI; see <a href="#">Figure 4</a>	1	4	8	ns
		nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a>	2	13	18	ns
$t_{PHL}$	HIGH to LOW propagation delay	nA to nBI; see <a href="#">Figure 4</a>	2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a>	2	4	10	ns

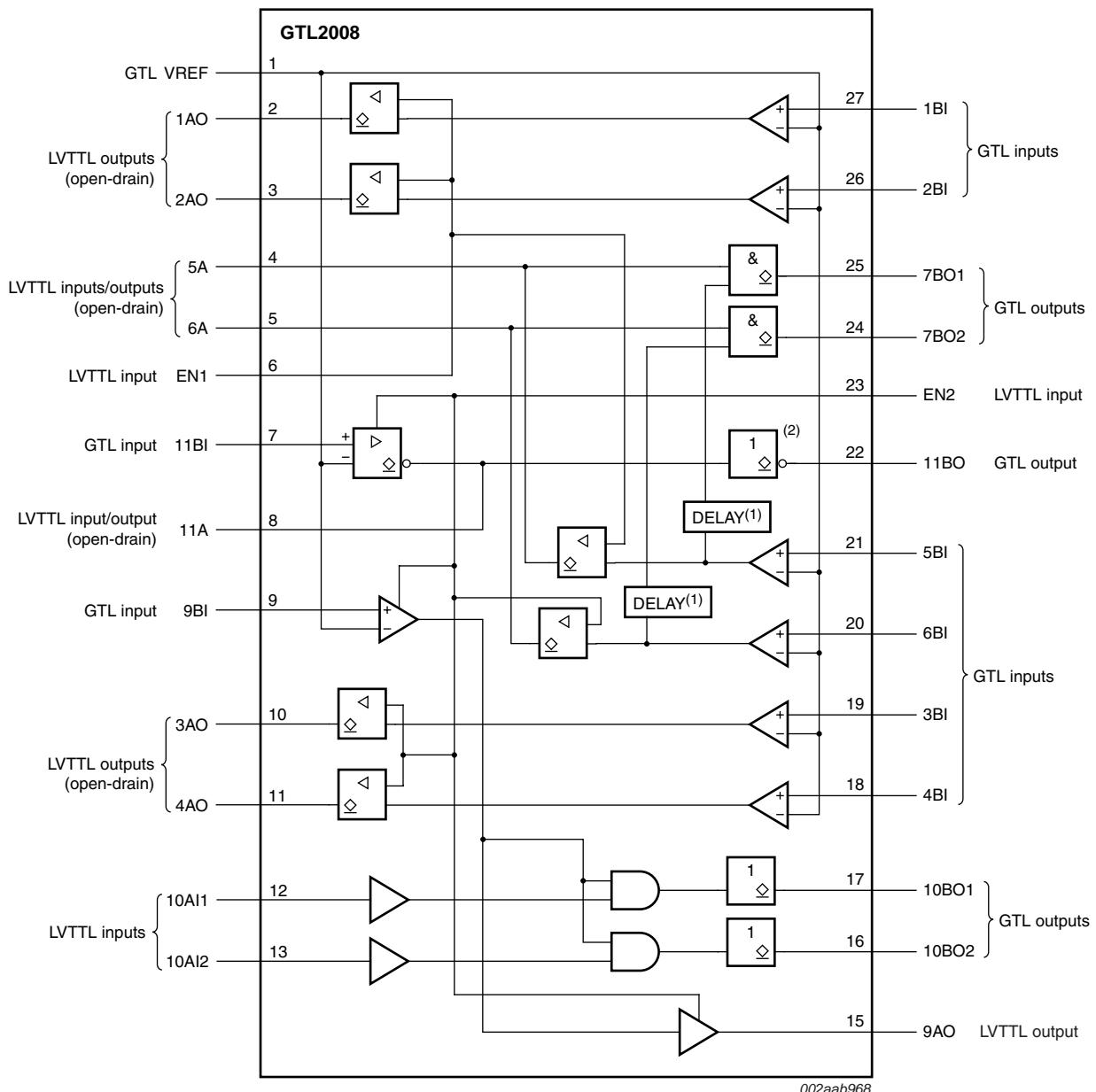
### 4. Ordering information

**Table 2. Ordering information**

$T_{amb} = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$

Type number	Topside mark	Package			Version
		Name	Description		
GTL2008PW	GTL2008	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm		SOT361-1

## 5. Functional diagram

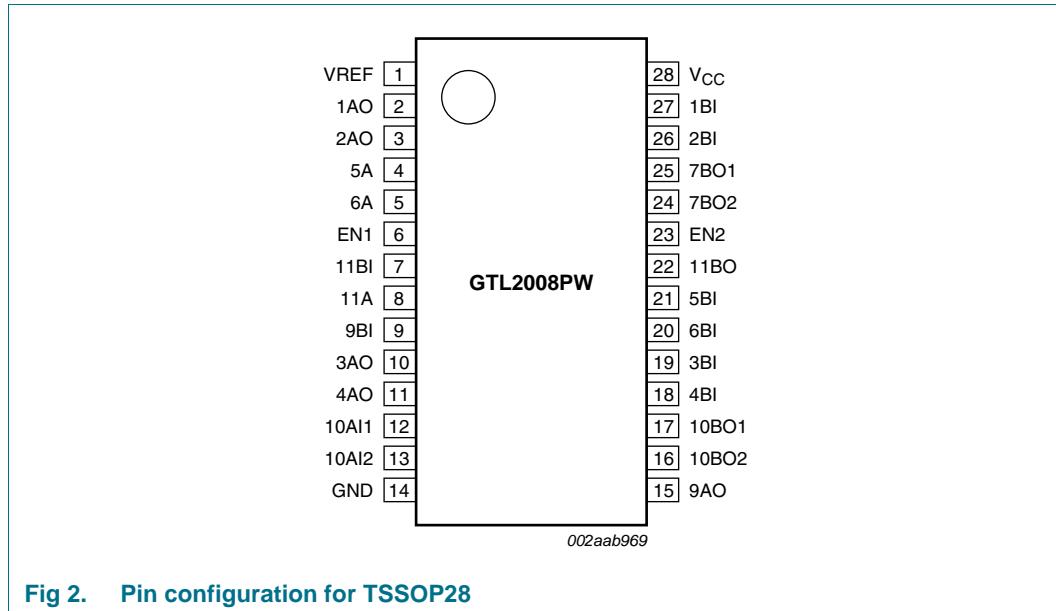


- (1) The enable on 7BO1/7BO2 include a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a LOW glitch on the 7BO1/7BO2 outputs.
- (2) The 11BO output is driven LOW after  $V_{CC}$  is powered up with EN2 LOW to prevent reporting of a fault condition before EN2 goes HIGH.

**Fig 1. Logic diagram of GTL2008**

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VREF	1	GTL reference voltage
1AO	2	data output (LVTTL), open-drain
2AO	3	data output (LVTTL), open-drain
5A	4	data input/output (LVTTL), open-drain
6A	5	data input/output (LVTTL), open-drain
EN1	6	enable input (LVTTL)
11BI	7	data input (GTL)
11A	8	data input/output (LVTTL), open-drain
9BI	9	data input (GTL)
3AO	10	data output (LVTTL), open-drain
4AO	11	data output (LVTTL), open-drain
10AI1	12	data input (LVTTL)
10AI2	13	data input (LVTTL)
GND	14	ground (0 V)
9AO	15	data output (LVTTL), 3-state
10BO2	16	data output (GTL)
10BO1	17	data output (GTL)
4BI	18	data input (GTL)
3BI	19	data input (GTL)

**Table 3. Pin description ...continued**

Symbol	Pin	Description
6BI	20	data input (GTL)
5BI	21	data input (GTL)
11BO	22	data output (GTL)
EN2	23	enable input (LVTTL)
7BO2	24	data output (GTL)
7BO1	25	data output (GTL)
2BI	26	data input (GTL)
1BI	27	data input (GTL)
V <sub>CC</sub>	28	positive supply voltage

## 7. Functional description

Refer to [Figure 1 “Logic diagram of GTL2008”](#).

### 7.1 Function tables

**Table 4. GTL input signals**

*H* = HIGH voltage level; *L* = LOW voltage level.

Input	Output <sup>[1]</sup>
1BI/2BI/3BI/4BI/9BI	1AO/2AO/3AO/4AO/9AO
L	L
H	H

[1] 1AO, 2AO, 3AO, 4AO and 5A/6A condition changed by ENn power good signal as described in [Table 5](#) and [Table 6](#).

**Table 5. EN1 power good signal**

*H* = HIGH voltage level; *L* = LOW voltage level.

<b>EN1</b>	<b>1AO and 2AO</b>	<b>5A</b>
L	1BI and 2BI disconnected (high-Z)	5BI disconnected
H	follows BI	5BI connected

**Table 6. EN2 power good signal**

*H* = HIGH voltage level; *L* = LOW voltage level.

<b>EN2</b>	<b>3AO and 4AO</b>	<b>6A</b>
L	3BI and 4BI disconnected (high-Z)	6BI disconnected
H	follows BI	6BI connected

**Table 7. SMI signals***H = HIGH voltage level; L = LOW voltage level; X = Don't care.*

Inputs			Output
10AI1/10AI2	EN2	9BI	10BO1/10BO2
L	H	L	L
L	H	H	L
H	H	L	L
H	H	H	H
L	L	X	L
H	L	X	H

**Table 8. PROCHOT signals***H = HIGH voltage level; L = LOW voltage level.*

Input	Input/output	Output
5BI/6BI	5A/6A (open-drain)	7BO1/7BO2
L	L	H <sup>[1]</sup>
H	L <sup>[2]</sup>	L
H	H	H

[1] The enable on 7BO1/7BO2 includes a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a low glitch on the 7BO1/7BO2 outputs.

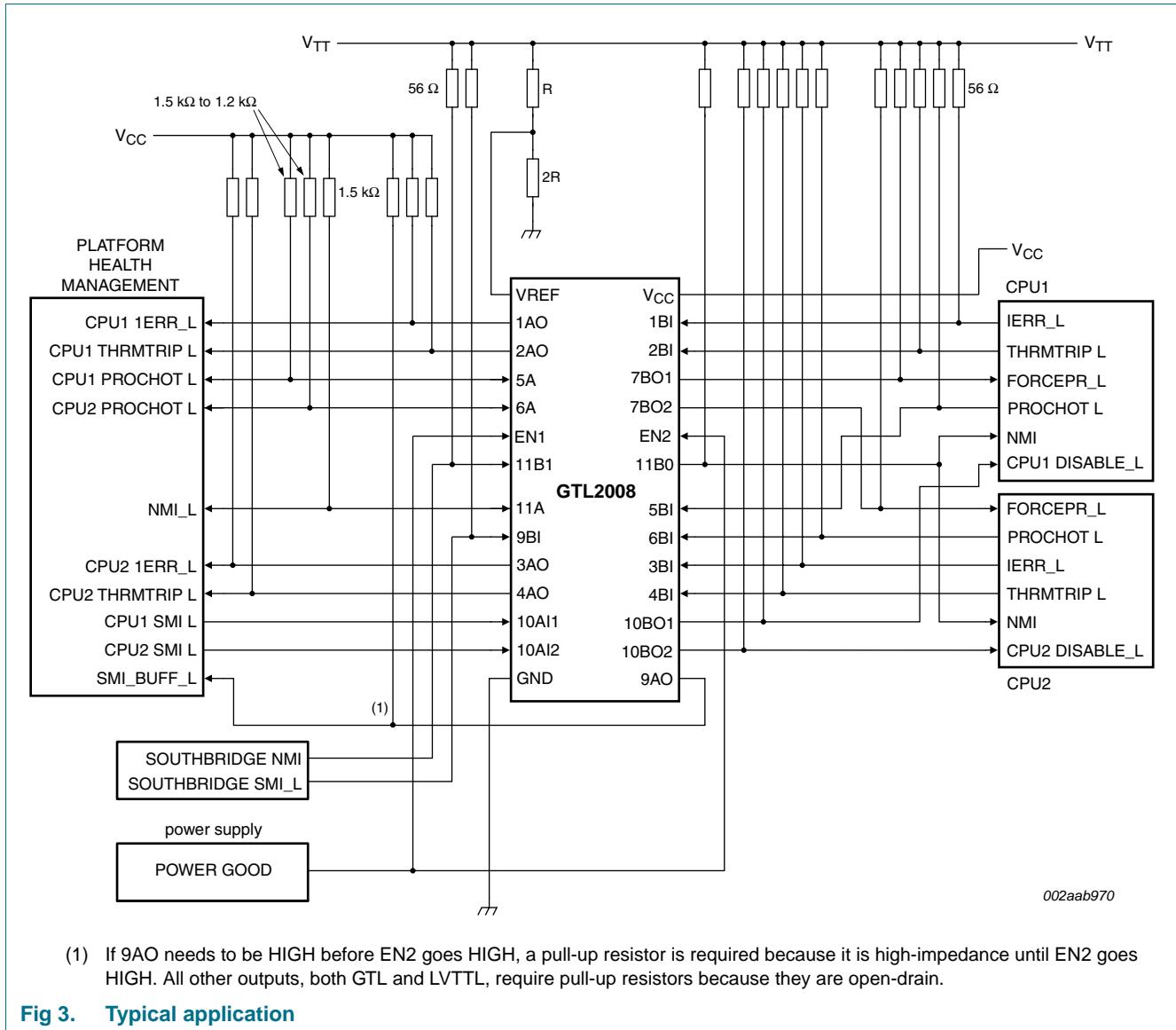
[2] Open-drain input/output terminal is driven to logic LOW state by other driver.

**Table 9. NMI signals***H = HIGH voltage level; L = LOW voltage level; X = Don't care.*

Inputs		Input/output	Output
11BI	EN2	11A (open-drain)	11BO
L	H	H	L
L	H	L <sup>[1]</sup>	H
H	H	L	H
X	L	H	L
X	L	L <sup>[1]</sup>	H

[1] Open-drain input/output terminal is driven to logic LOW state by other driver.

## 8. Application design-in information



**Fig 3. Typical application**

## 9. Limiting values

**Table 10. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).  
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$V_I$	input voltage	A port (LVTTL)	-0.5 <sup>[1]</sup>	+4.6	V
		B port (GTL)	-0.5 <sup>[1]</sup>	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-	-50	mA
$V_O$	output voltage	output in OFF or HIGH state; A port	-0.5 <sup>[1]</sup>	+4.6	V
		output in OFF or HIGH state; B port	-0.5 <sup>[1]</sup>	+4.6	V
$I_{OL}$	LOW-level output current <sup>[2]</sup>	A port	-	32	mA
		B port	-	30	mA
$I_{OH}$	HIGH-level output current <sup>[3]</sup>	A port	-	-32	mA
$T_{stg}$	storage temperature		-60	+150	°C
$T_{j(max)}$	maximum junction temperature		<sup>[4]</sup> -	+125	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] Current into any output in the LOW state.

[3] Current into any output in the HIGH state.

[4] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 10. Recommended operating conditions

**Table 11. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		3.0	3.3	3.6	V
$V_{TT}$	termination voltage	GTL	-	1.2	-	V
$V_{ref}$	reference voltage	GTL	0.64	0.8	1.1	V
$V_I$	input voltage	A port	0	3.3	3.6	V
		B port	0	$V_{TT}$	3.6	V
$V_{IH}$	HIGH-level input voltage	A port and ENn	2	-	-	V
		B port	$V_{ref} + 0.050$	-	-	V
$V_{IL}$	LOW-level input voltage	A port and ENn	-	-	0.8	V
		B port	-	-	$V_{ref} - 0.050$	V
$I_{OH}$	HIGH-level output current	A port	-	-	-16	mA
$I_{OL}$	LOW-level output current	A port	-	-	16	mA
		B port	-	-	15	mA
$T_{amb}$	ambient temperature	operating in free-air	-40	-	+85	°C

## 11. Static characteristics

**Table 12. Static characteristics**

Recommended operating conditions; voltages are referenced to GND (ground = 0 V).  $T_{amb} = -40$  °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{OH}$	HIGH-level output voltage	9AO; $V_{CC} = 3.0$ V to 3.6 V; $I_{OH} = -100$ $\mu$ A	[2] $V_{CC} - 0.2$	3.0	-	V
		9AO; $V_{CC} = 3.0$ V; $I_{OH} = -16$ mA	[2] 2.1	2.3	-	V
$V_{OL}$	LOW-level output voltage	A port; $V_{CC} = 3.0$ V; $I_{OL} = 4$ mA	[2] -	0.15	0.4	V
		A port; $V_{CC} = 3.0$ V; $I_{OL} = 8$ mA	[2] -	0.3	0.55	V
		A port; $V_{CC} = 3.0$ V; $I_{OL} = 16$ mA	[2] -	0.6	0.8	V
		B port; $V_{CC} = 3.0$ V; $I_{OL} = 15$ mA	[2] -	0.13	0.4	V
$I_{OH}$	HIGH-level output current	open-drain outputs; A port other than 9AO; $V_O = V_{CC}$ ; $V_{CC} = 3.6$ V	-	-	$\pm 1$	$\mu$ A
$I_I$	input current	A port; $V_{CC} = 3.6$ V; $V_I = V_{CC}$	-	-	$\pm 1$	$\mu$ A
		A port; $V_{CC} = 3.6$ V; $V_I = 0$ V	-	-	$\pm 1$	$\mu$ A
		B port; $V_{CC} = 3.6$ V; $V_I = V_{TT}$ or GND	-	-	$\pm 1$	$\mu$ A
$I_{CC}$	supply current	A or B port; $V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ mA	-	8	12	mA
$\Delta I_{CC}$ <sup>[3]</sup>	additional supply current	per input; A port or control inputs; $V_{CC} = 3.6$ V; $V_I = V_{CC} - 0.6$ V	-	-	500	$\mu$ A
$C_{io}$	input/output capacitance	A port; $V_O = 3.0$ V or 0 V	-	2.5	3.5	pF
		B port; $V_O = V_{TT}$ or 0 V	-	1.5	2.5	pF

[1] All typical values are measured at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than  $V_{CC}$  or GND.

## 12. Dynamic characteristics

**Table 13. Dynamic characteristics**

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
<b><math>V_{ref} = 0.73 \text{ V}; V_{TT} = 1.1 \text{ V}</math></b>							
$t_{PLH}$	LOW to HIGH propagation delay	nA to nBI; see <a href="#">Figure 4</a>	1	4	8	ns	
		9BI to 9AO; see <a href="#">Figure 5</a>	2	5.5	10	ns	
		nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a>	2	13	18	ns	
		9BI to 10BOn	2	6	11	ns	
		11A to 11BO; see <a href="#">Figure 10</a>	1	4	8	ns	
		11BI to 11A; see <a href="#">Figure 9</a>	2	7.5	11	ns	
		11BI to 11BO	2	8	13	ns	
$t_{PHL}$	HIGH to LOW propagation delay	5BI to 7BO1 or 6BI to 7BO2; see <a href="#">Figure 7</a>	4	7	12	ns	
		nA to nBI; see <a href="#">Figure 4</a>	2	5.5	10	ns	
		9BI to 9AO; see <a href="#">Figure 5</a>	2	5.5	10	ns	
		nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a>	2	4	10	ns	
		9BI to 10BOn	2	6	11	ns	
		11A to 11BO; see <a href="#">Figure 10</a>	1	5.5	10	ns	
		11BI to 11A; see <a href="#">Figure 9</a>	2	8.5	13	ns	
$t_{PLZ}$	LOW to OFF-state propagation delay	11BI to 11BO	[2]	2	14	21	ns
		5BI to 7BO1 or 6BI to 7BO2; see <a href="#">Figure 7</a>		100	205	350	ns
$t_{PZL}$	OFF-state to LOW propagation delay	EN1 to nAO or EN2 to nAO; see <a href="#">Figure 8</a>	1	3	10	ns	
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see <a href="#">Figure 8</a>	1	3	7	ns	
$t_{PHZ}$	HIGH to OFF-state propagation delay	EN1 to nAO or EN2 to nAO; see <a href="#">Figure 8</a>	2	7	10	ns	
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see <a href="#">Figure 8</a>	2	7	10	ns	
$t_{PZH}$	OFF-state to HIGH propagation delay	EN2 to 9AO; see <a href="#">Figure 11</a>	2	5	10	ns	

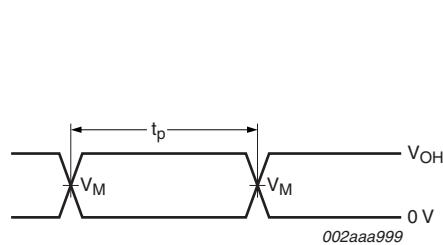
**Table 13. Dynamic characteristics ...continued** $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b><math>V_{ref} = 0.76 \text{ V}</math>; <math>V_{TT} = 1.2 \text{ V}</math></b>						
$t_{PLH}$	LOW to HIGH propagation delay	nA to nBI; see <a href="#">Figure 4</a> 9BI to 9AO; see <a href="#">Figure 5</a> nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a> 9BI to 10BOn 11A to 11BO; see <a href="#">Figure 10</a> 11BI to 11A; see <a href="#">Figure 9</a> 11BI to 11BO 5BI to 7BO1 or 6BI to 7BO2; see <a href="#">Figure 7</a>	1 2 2 2 1 2 2 4	4 5.5 13 6 8 7.5 8 7	8 10 18 11 8 11 13 12	ns ns ns ns ns ns ns ns
$t_{PHL}$	HIGH to LOW propagation delay	nA to nBI; see <a href="#">Figure 4</a> 9BI to 9AO; see <a href="#">Figure 5</a> nBI to nA or nAO (open-drain outputs); see <a href="#">Figure 14</a> 9BI to 10BOn 11A to 11BO; see <a href="#">Figure 10</a> 11BI to 11A; see <a href="#">Figure 9</a> 11BI to 11BO 5BI to 7BO1 or 6BI to 7BO2; see <a href="#">Figure 7</a>	2 2 2 2 1 2 2 100	5.5 5.5 4 6 5.5 8.5 14 205	10 10 10 11 10 13 21 350	ns ns ns ns ns ns ns ns
$t_{PLZ}$	LOW to OFF-state propagation delay	EN1 to nAO or EN2 to nAO; see <a href="#">Figure 8</a> EN1 to 5A (I/O) or EN2 to 6A (I/O); see <a href="#">Figure 8</a>	1 1	3 3	10 7	ns ns
$t_{PZL}$	OFF-state to LOW propagation delay	EN1 to nAO or EN2 to nAO; see <a href="#">Figure 8</a> EN1 to 5A (I/O) or EN2 to 6A (I/O); see <a href="#">Figure 8</a>	2 2	7 7	10 10	ns ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	EN2 to 9AO; see <a href="#">Figure 11</a>	2	5	10	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	EN2 to 9AO; see <a href="#">Figure 11</a>	2	4	10	ns

[1] All typical values are at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .[2] Includes ~7.6 ns RC rise time of test load pull-up on 11A, 1.5 k $\Omega$  pull-up and 21 pF load on 11A has about 23 ns RC rise time.

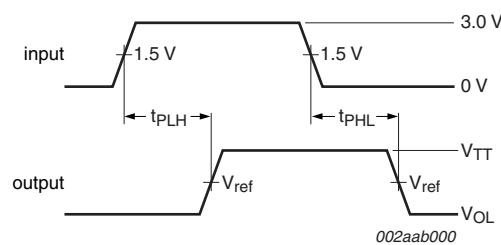
## 12.1 Waveforms

$V_M = 1.5$  V at  $V_{CC} \geq 3.0$  V for A ports;  $V_M = V_{ref}$  for B ports.



$V_M = 1.5$  V for A port and  $V_{ref}$  for B port

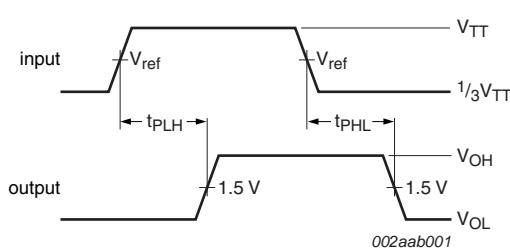
a. Pulse duration



A port to B port

b. Propagation delay times

Fig 4. Voltage waveforms



$PRR \leq 10$  MHz;  $Z_0 = 50 \Omega$ ;  $t_r \leq 2.5$  ns;  $t_f \leq 2.5$  ns

Fig 5. Propagation delay, 9BI to 9AO

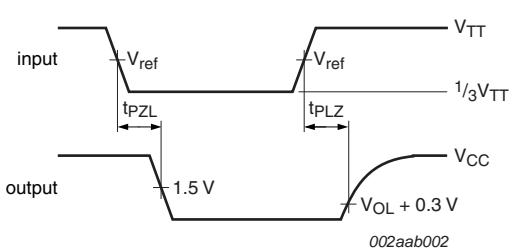


Fig 6. nBI to nAO (I/O) or nBI to nAO open-drain outputs

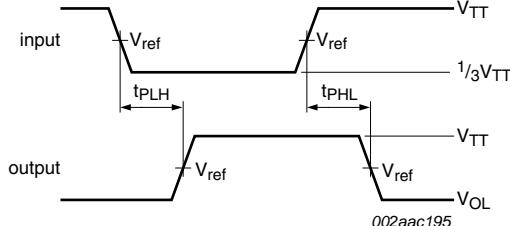


Fig 7. 5BI to 7BO1 or 6BI to 7BO2

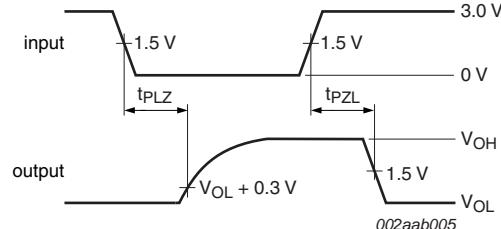


Fig 8. EN1 to 5A (I/O) or EN2 to 6A (I/O) or EN1 to nAO or EN2 to nAO

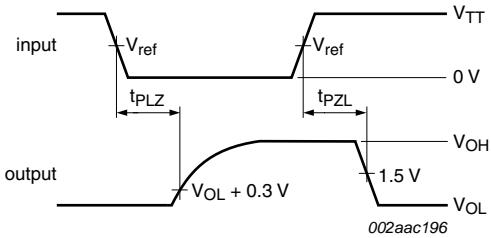


Fig 9. 11BI to 11A

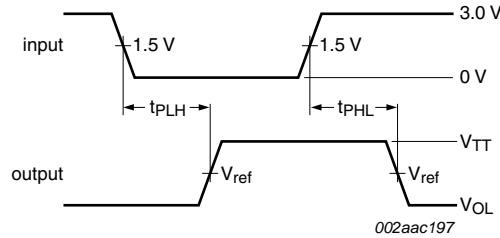


Fig 10. 11A to 11BO

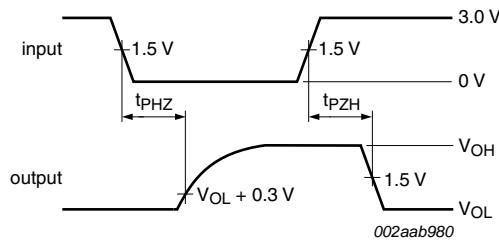
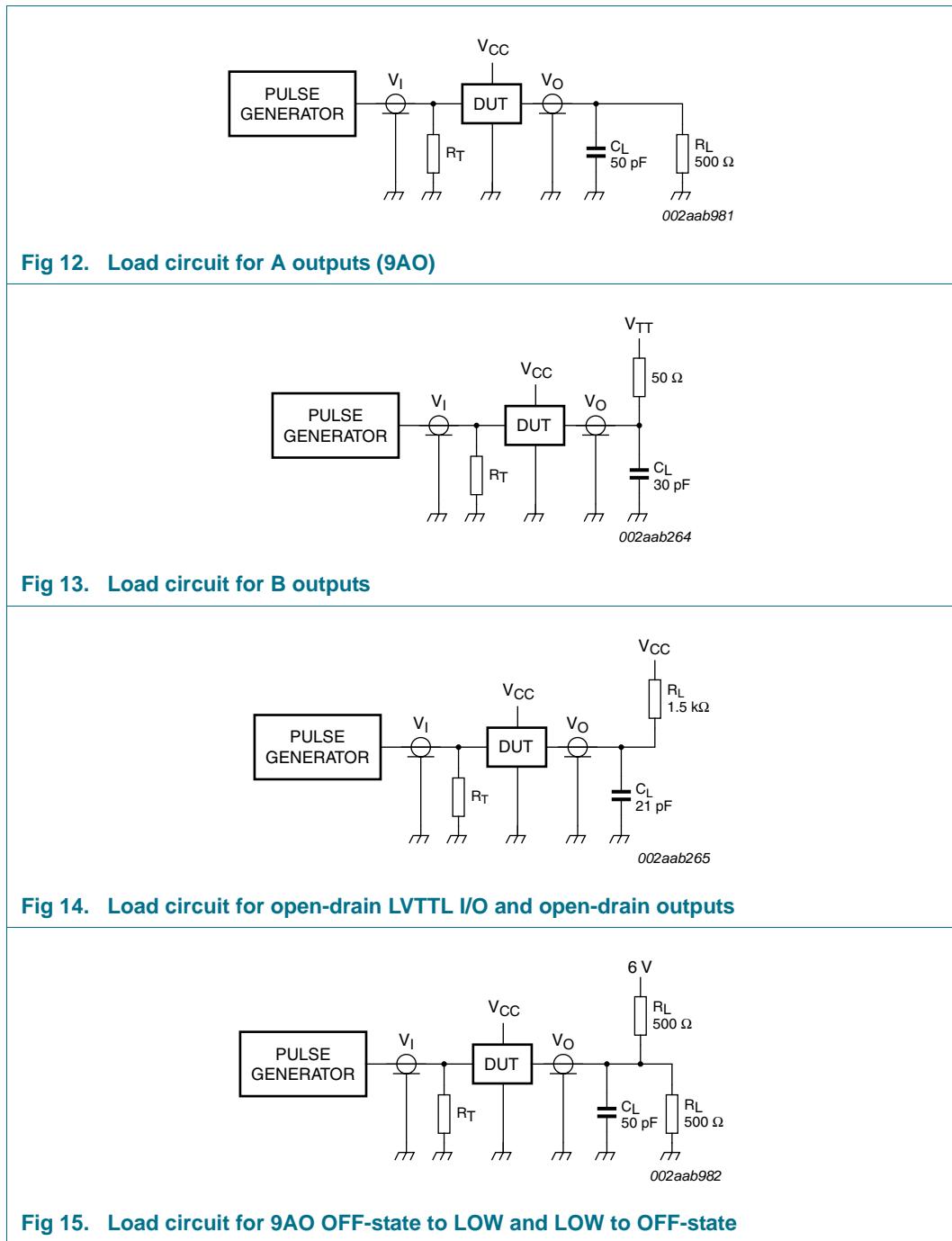


Fig 11. EN2 to 9AO

## 13. Test information



$R_L$  — Load resistor

$C_L$  — Load capacitance; includes jig and probe capacitance

$R_T$  — Termination resistance; should be equal to  $Z_0$  of pulse generators.

## 14. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1

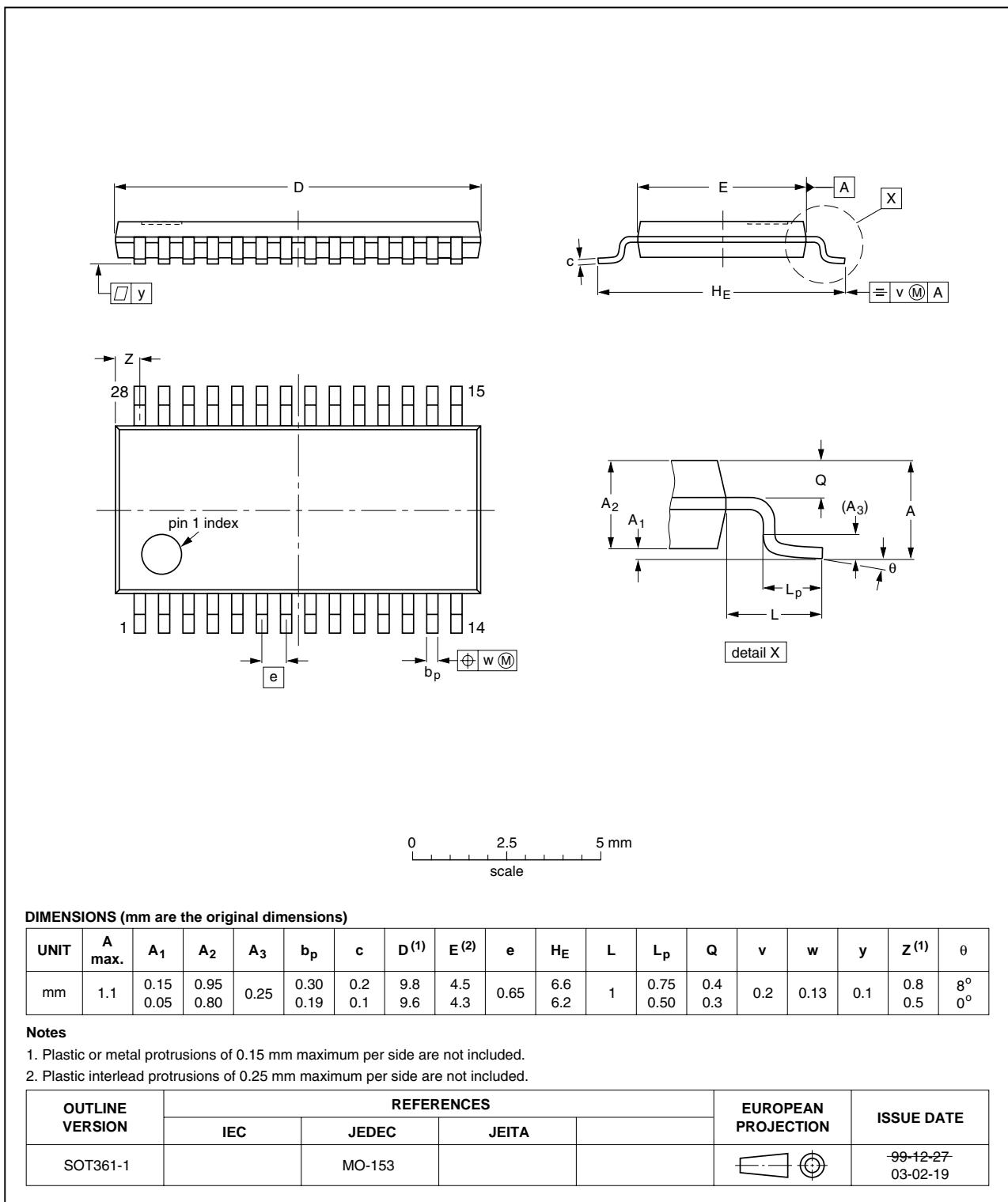


Fig 16. Package outline SOT361-1 (TSSOP28)

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 17](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [15](#)

**Table 14. SnPb eutectic process (from J-STD-020C)**

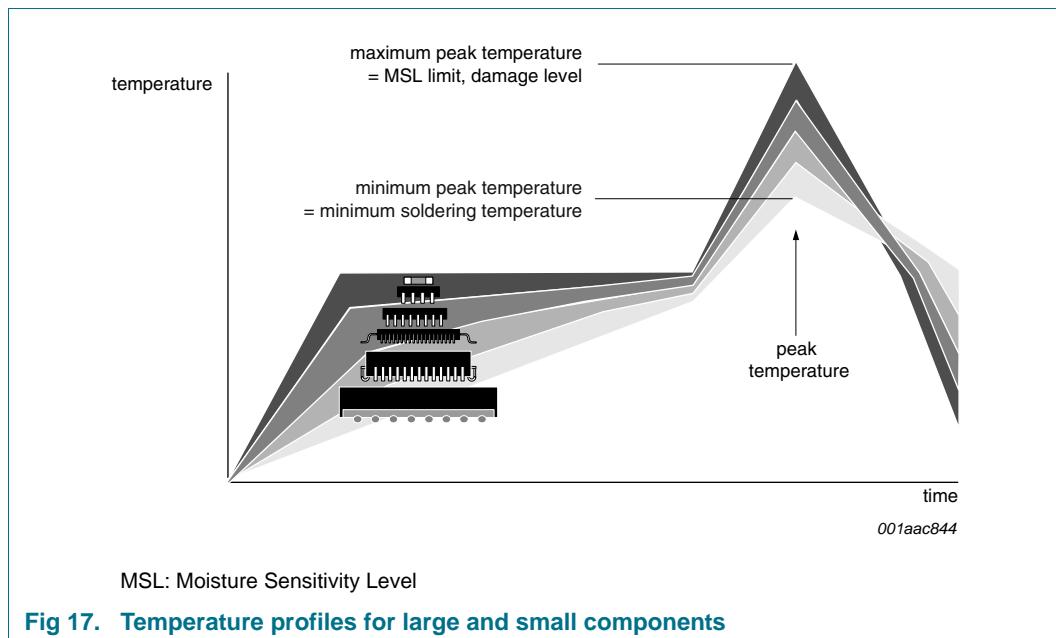
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 15. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 17](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

## 16. Abbreviations

**Table 16. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic
VRD	Voltage Regulator Down

## 17. Revision history

**Table 17. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2008_4	20100219	Product data sheet	-	GTL2008_3
Modifications:		<ul style="list-style-type: none"><li>• <a href="#">Section 2 “Features and benefits”</a>, 8<sup>th</sup> bullet item: corrected from “200 V MM per JESD22-A115” to “150 V MM per JESD22-A115”</li></ul>		
GTL2008_3	20070201	Product data sheet	-	GTL2008_GTL2107_2
GTL2008_GTL2107_2	20060926	Product data sheet	-	GTL2008_1
GTL2008_1	20060502	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

malfuction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Non-automotive qualified products** — Unless the data sheet of an NXP Semiconductors product expressly states that the product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

### 18.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any

liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

#### 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

### 19. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 20. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Quick reference data</b> .....	<b>2</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>3</b>
<b>6</b>	<b>Pinning information</b> .....	<b>4</b>
6.1	Pinning .....	4
6.2	Pin description .....	4
<b>7</b>	<b>Functional description</b> .....	<b>5</b>
7.1	Function tables .....	5
<b>8</b>	<b>Application design-in information</b> .....	<b>7</b>
<b>9</b>	<b>Limiting values</b> .....	<b>8</b>
<b>10</b>	<b>Recommended operating conditions</b> .....	<b>8</b>
<b>11</b>	<b>Static characteristics</b> .....	<b>9</b>
<b>12</b>	<b>Dynamic characteristics</b> .....	<b>10</b>
12.1	Waveforms .....	12
<b>13</b>	<b>Test information</b> .....	<b>14</b>
<b>14</b>	<b>Package outline</b> .....	<b>15</b>
<b>15</b>	<b>Soldering of SMD packages</b> .....	<b>16</b>
15.1	Introduction to soldering .....	16
15.2	Wave and reflow soldering .....	16
15.3	Wave soldering .....	16
15.4	Reflow soldering .....	17
<b>16</b>	<b>Abbreviations</b> .....	<b>18</b>
<b>17</b>	<b>Revision history</b> .....	<b>19</b>
<b>18</b>	<b>Legal information</b> .....	<b>20</b>
18.1	Data sheet status .....	20
18.2	Definitions .....	20
18.3	Disclaimers .....	20
18.4	Trademarks .....	21
<b>19</b>	<b>Contact information</b> .....	<b>21</b>
<b>20</b>	<b>Contents</b> .....	<b>22</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 19 February 2010

Document identifier: GTL2008\_4

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP](#):

[GTL2008PW](#) [GTL2008PW-T](#)