# NetSilicon® NS9360

## NS9360 272-Pin BGA, Lead-Free, RoHS Compliant

USB Host JTAG Test USB Device ARM926EJ-S Real-Time 177, 155 or 103 MHz Clock 8 kB I-Cache Serial 10/100 Modul X4 16 GPIO Distributed DMA MII/RMII 88.5, 77.5 or 51.5 MHz AHB B 3PIO (50 32 b-D, 32 b-A LCD Controller 8 x Timers/Counters

**NET+ARM Processors** 

- 32-bit, 177, 155, 103 MHz NET+ARM processor
- 0.13 µm CMOS process
- 10/100Base-T Ethernet
- Extensive on-chip peripherals
- Comprehensive networking software



#### Features/Benefits

- > High performance 32-pit processor with rich set of peripherals
- > 177 MHz ARM9 core (ARM926EJ-S)
- > Harvard architecture with 8 kB/4 kB instruction/data cache
- > DSP instruction set extensions
- > Jazelle® Java byte-code accelerator
- > Full-duplex 10/100Base-T Ethernet MAC
- > 88.5 MHz memory/peripherals controller
- > AM and PM color and monochrome LCD controller
- > USB 2.0 Full-Speed OHCI host and 13-EP device
- > Four multi-function serial ports; UART or SPI (master or slave)
- > I2C port (master or slave)
- > Programmable timers/counters/PWM
- > 73 General Purpose I/O (GPIO) pins
- > Highly configurable power management
- > Supported by the comprehensive and integrated NET+Works development suite
- > Complete Windows CE 5.0 Board Support Package (BSP) available
- > Royalty-free Linux 2.6 kernel distribution available (LxNETES)

### Overview

The NetSilicon NS9360 is the third ARM9 processor in our award-winning family of NET+ARM 32-bit processors. It is targeted at network-enabling embedded electronic equipment that requires a rich set of peripherals. The NS9360 provides full duplex 10/100Base-T Ethernet functionality with additional processing performance and bandwidth to handle sophisticated embedded applications.

The NS9360 is based on the ARM926EJ-S, ARM's most powerful ARM9 core, which contains both DSP and Java byte code instructions. It operates at up to 177 MHz and contains a broad set of industry standard peripherals, including 10/100Base-T Ethernet, USB, I<sup>2</sup>C, 1284, serial ports and a highly configurable LCD controller.

Like all of our processors, the NS9360 is supported by the royalty-fre NET+Works® software development tool suite. The integrated NET+Works package contains either Green Hills® MULTI® or Microcross GNU X-Tools™, MAJIC™ debugger, Express Logic's ThreadX® real-time operating system, a TCP/IP stack, networking applications, software, utilities and numerous networking applications examples. Support and Development kits for Linux and Microsoft® Windows® CE are also available.

Please contact us at 1-877-OEM-DIGI or 952-912-3444 for additional information or to discuss your specific application requirements.



www.digi.com





#### 32-BIT ARM926EJ-S RISC PROCESSOR

- 103, 155, 177 MHz
- 5-stage pipeline
- Harvard architecture
- 8 kB I-cache and 4 kB D-cache
- 32-bit ARM and 16-bit Thumb instruction sets, can be mixed for performance/code density tradeoffs
- MMU to support virtual memory based OS's such as Linux, WinCE/Pocket PC, VxWorks, etc.
- DSP instruction extensions: improved divide, single cycle multiply accumulate
- ARM Jazelle, 1060 CM (Caffeine Marks) Java Accelerator
- · Embedded ICE-RT debug unit
- JTAG boundary scan support
- Clock-gated processor for decreased power dissipation



#### EXTERNAL SYSTEM BUS INTERFACE

- 32-bit data bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- Up to 256 MB SDRAM, up to 2 GB DIMM
- 4 static and 4 dynamic chip selects
- 0-63 wait states per chip select
- Self-refresh during system sleep
- Automatic dynamic bus sizing to 8-bits, 16-bits, 32-bits
- Burst-mode support with automatic data width adjustment
- 2 external DMA channels for external peripheral support



#### OPTIMIZED 10/100 ETHERNET MAC

- MII or RMII PHY interfaces
- Full or half duplex
- Station, broadcast, multicast address filtering
- 2 kB Rx FIFO
- 256 B Tx FIFO with on-chip buffer descriptor ring (eliminates underruns and decreases bus traffic)
- Separate Tx and Rx DMA channels
- Intelligent receive-side buffer size selection
- Support for full statistics gathering
- Support for external CAM filtering



#### SERIAL PORTS

- 4 serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 1.8
  Mbps: asynchronous x8 mode
- Max bit rates for synchronous mode are:
- 1/16 CPU speed for SPI master
- 1/32 CPU speed for SPI slave
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7 or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support for synchronous mode
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 total
- 32 B Tx FIFO and 32 B Rx FIFO per module



## CONTROLLER

FLEXIBLE LCD

- Supports commercially available displays up to SVGA
- Active-matrix color TFT displays
- Up to 18 bpp; 256K colors
- Single and dual-panel color passive-matrix displays
  - Up to 16 bpp 4:4:4 RGB;
    3375 colors
- Single and dual-panel monochrome STN displays
- 1, 2, 4 bpp palletized grayscale
- Formats image data and generates timing control signals
- Internal programmable palette-LUT and grayscaler support different color techniques
- Programmable panel-clock frequency



#### I<sup>2</sup>C PORT

- I<sup>2</sup>C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes



#### SYSTEM BOOT

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)



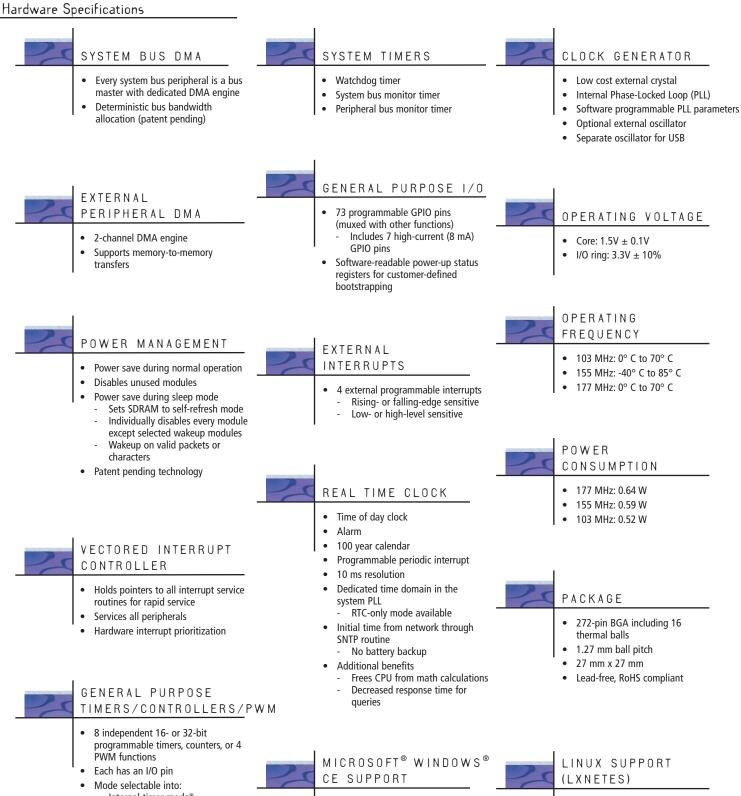
#### USB PORTS

- USB v.2.0 Full Speed (12 Mbps) and low speed (1.5 Mbps)
- OHCI host and 11 end points device
- Single PHY can be used with either host or device
- Interface to external PHY for simultaneous host and device operation
- USB host is a bus master
- Each USB device endpoint is supported by a dedicated DMA channel, 13 total
- 20 B Rx FIFO and 20 B Tx FIFO



### 1284 PARALLEL PERIPHERAL-TO-HOST PORT

- All standard modes:
  - ECP, Byte, Nibble, Compatibility
- RLE (Run Length Encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz
- 4 dedicated DMA channels
  - 2 for data and 2 for control
- Microsoft Plug-and-Play, no Windows driver needed



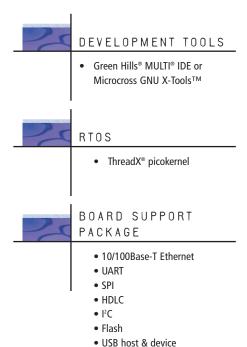
- Internal timer mode®

  - External gated timer mode
  - External event counter
- Timers/counters can be concatenated
- Minute-range events measurable
- Source clock selectable
- Internal clock or external pulse event
- Individually enabled/disabled

- Complete Windows CE 5.0 Board Support Package (BSP)
- Custom-developed drivers to support peripherals, modules and **Development Kits**
- Exclusive software to provide debugging channel via Ethernet connection
- Based on Linux 2.6.x kernel
- Complete GNU ToolSuite of compilers and debuggers
- Bootloader for managing and installing software updates

### **NET+Works Integrated Development Package**

NET+ARM network-attached processors are the core of the NET+Works family of solutions that add intelligence and connectivity to electronic devices. We offer extensive networking software to support industrial automation, building automation, point-of-sale, office automation and other enterprise applications.





#### NETWORKING PROTOCOLS

- TCP/IP stack
- TCP and UDP Sockets API
- **ICMP**
- **IGMP**
- PPP for serial communications
- Address Configuration Executive (ACE):
  - ARP
  - RARP
  - Ping ARP
  - AutoIP
  - **DHCP** client
  - BootP
- Fast IP
- Fast sockets
- SSL, TLS



#### UTILITIES

- HTML compilation
- MIB compilation
- Download of Flash images
- Bootloader
- Code builds
- Integrated flash file system
- Code Profiler
- **Boundary Scan Description** Language (BSDL)



#### TECHNICAL SUPPORT

One year of software maintenance and technical support



#### NETWORKING SERVICES

- FTP server/client; TFTP
- LDAPv3 agent, for access to network information services
- HTTP APIs for serving basic and advanced web pages
- HTTPS for security
- Email (POP3 and SMTP)
- SNMP v1/MIBII for remote management
- SNTP
- DNS
- Telnet
- Multi-homing



#### DEVELOPMENT BOARD

NS9360 development board and JTAG debugger



• LCD

• 1284 peripheral Power save

#### MODEL.....PART NUMBERS

Worldwide

NS9360B-0-C177

#### Model

103 MHz, 0° C to 70° C operation 155 MHz, -40° C to 85° C operation 177 MHz, 0° C to 70° C operation

NS9360B-0-C103 NS9360B-0-I155

#### DIGI SERVICE AND SUPPORT

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