

TC7MP245FK

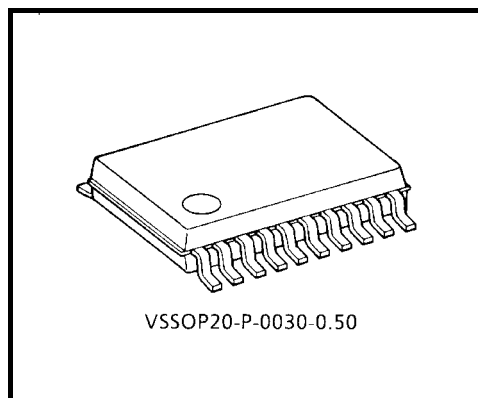
Low-Voltage/Low-Power Octal Bus Transceiver with Bus-hold

The TC7MP245FK is a high-performance CMOS octal bus transceiver. By a low power consumption circuit, power consumption has been reduced when a bus terminal is disable state ($\overline{OE}$ =High).

The direction of data transmission is determined by the level of the DIR input. The $\overline{OE}$ input can be used to disable the device so that the busses are effectively isolated.

But, bus of a B bus side at floating state is maintained in an appropriate logic level due to a bus hold circuit to a B bus. Moreover, the bus-hold circuit which is added to a B bus is off when $\overline{OE}$ is low.

All inputs are equipped with protection circuits against static discharge.



VSSOP20-P-0030-0.50

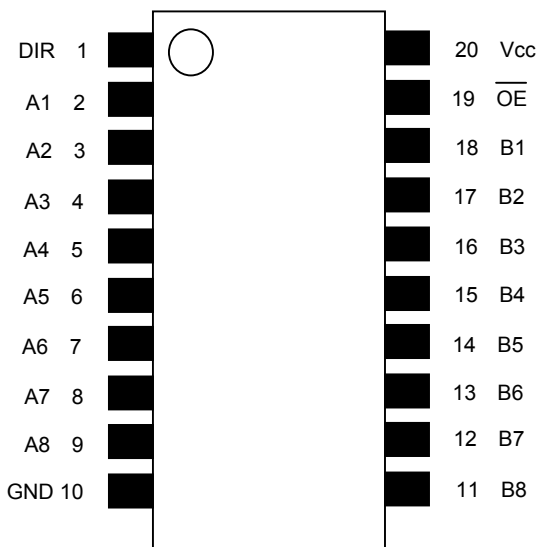
Weight: 0.03 g (typ.)

Features

- Low-voltage operation : $V_{CC} = 1.65$ to 3.6 V
- Low power current consumption : By a new input circuit, power consumption in $\overline{OE}=H$ is reduced largely.
It is most suitable for battery drive products such as personal digital assistant or a cellular phone.
- Quiescent supply current : $I_{CC} = 5 \mu A$ (max) ($V_{CC}=3.6V$)
- High-speed operation : $t_{pd}=3.0ns$ (max) ($V_{CC}=3.3\pm 0.3V$)
 $t_{pd}=4.6ns$ (max) ($V_{CC}=2.5\pm 0.2V$)
 $t_{pd}=10.0ns$ (max) ($V_{CC}=1.8\pm 0.15V$)
- Output current : I_{OHA}/I_{OLA} (A bus) $=\pm 12mA$ (min) ($V_{CC}=3.0V$)
 I_{OHB}/I_{OLB} (B bus) $=\pm 24mA$ (min) ($V_{CC}=3.0V$)
- Latch-up performance : $\pm 300mA$
- ESD performance : Machine model $> \pm 200V$
Human body model $> \pm 2000V$
- Ultra-small package : VSSOP (US20)
- Bus hold circuit is built in only the B bus side. (Only in $\overline{OE}=H$, a former state is maintained.)
- Floating of A-bus and B-bus are permitted.(When $\overline{OE}=H$)
- Gate IC for control(TC7MP01FK) of DIR and $\overline{OE}$ terminal are prepared.
- 3.6V tolerant function provided on A-bus terminal, DIR and $\overline{OE}$ terminal.

Note: At the time bus terminal is enable state, please do not give a signal from the outside.

Pin Assignment (top view)



Truth Table

Input		Bus state	Bus hold circuit (B bus)
DIR	$\overline{\text{OE}}$		
L	L	$B \rightarrow A (B=A)$	OFF
H	L	$A \rightarrow B (A=B)$	OFF
X	H	Z	ON*

X: Don't care

Z: High impedance

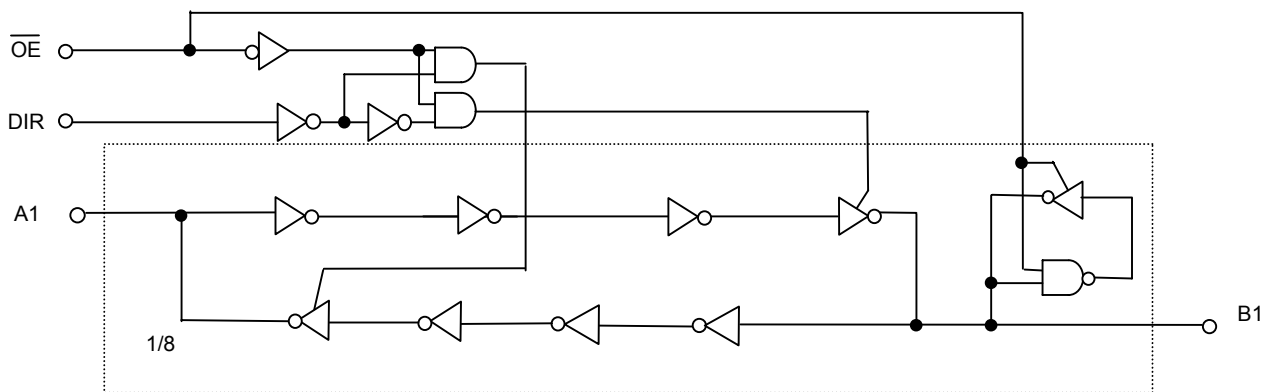
*: Logic state just before becoming disable is maintained.

Note: When a bus input is in "H" state ,and an output is switched to "enable" to "disable",

Glitch such as "L" state during about 1 to 3ns occurs in an output.

It is not generated when a bus input is in "L" state.

System Diagram



Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{CC}	−0.5 to 4.6	V
DC input voltage (DIR, $\overline{\text{OE}}$)	V _{IN}	−0.5 to 4.6	V
DC input/output voltage(A bus)	V _{I/OA}	−0.5 to 4.6 (Note 1)	V
		−0.5 to V _{CC} +0.5 (Note 2)	
DC input/output voltage(B bus)	V _{I/OB}	−0.5 to V _{CC} +0.5	V
Input diode current(DIR, $\overline{\text{OE}}$)	I _{IHK}	−50	mA
Input/Output diode current	I _{I/OK}	±50	mA
Output current	I _{OUT}	±50	mA
DC VCC/ground current	I _{CC} /I _{GND}	±100	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	−65 to 150	°C

 Note 1: V_{CC}=0V, or output off state.

 Note 2: $\overline{\text{OE}}$ ="L", DIR="L"

Recommended Operating Range

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.65 to 3.6	V
		1.2 to 3.6(Note 3)	
DC input voltage (DIR, $\overline{\text{OE}}$)	V _{IN}	−0.3 to 3.6	V
DC input/output voltage(A bus)	V _{I/OA}	0 to 3.6(Note 4)	V
		0 to V _{CC} (Note 5)	
DC input/output voltage(B bus)	V _{I/OB}	0 to V _{CC}	V
Output current (A bus)	I _{OHA} /I _{OLA}	±12(Note 6)	mA
		±9(Note 7)	
		±2(Note 8)	
Output current(B bus)	I _{OHB} /I _{OLB}	±24(Note 6)	mA
		±18(Note 7)	
		±4(Note 8)	
Operating temperature	T _{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10(Note 9)	ns/V

Note 3: Data retention only

 Note 4: V_{CC}=0V, or output off state

 Note 5: $\overline{\text{OE}}$ ="L", DIR="L"

 Note 6: V_{CC}=3.0 to 3.6V

 Note 7: V_{CC}=2.3 to 2.7V

 Note 8: V_{CC}=1.65 to 1.95V

 Note 9: V_{IN}=0.8 to 2.0V, V_{CC}=3.0V

Electrical Characteristics

DC Characteristics (Ta=-40 to 85°C, 2.7V < Vcc ≤ 3.6V)

Parameter		Symbol	Test Condition		Vcc(V)	Min	Max	Unit
DC input voltage	H-level	V _{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V _{IL}	—		2.7 to 3.6	—	0.8	
Output voltage (A bus)	H-level	V _{OHA}	V _{IN} = V _{IH}	I _{OHA} =-100uA	2.7 to 3.6	Vcc-0.2	—	V
				I _{OH} =-6mA	2.7	2.2	—	
				I _{OH} =-9mA	3.0	2.4	—	
				I _{OH} =-12mA	3.0	2.2	—	
	L-level	V _{OLA}	V _{IN} = V _{IL}	I _{OLA} =100uA	2.7 to 3.6	—	0.2	
				I _{OL} =6mA	2.7	—	0.4	
				I _{OL} =9mA	3.0	—	0.4	
				I _{OL} =12mA	3.0	—	0.55	
Output voltage (B bus)	H-level	V _{OHB}	V _{IN} = V _{IH}	I _{OHB} =-100uA	2.7 to 3.6	Vcc-0.2	—	V
				I _{OHB} =-12mA	2.7	2.2	—	
				I _{OHB} =-18mA	3.0	2.4	—	
				I _{OHB} =-24mA	3.0	2.2	—	
	L-level	V _{OLB}	V _{IN} = V _{IL}	I _{OLB} =100uA	2.7 to 3.6	—	0.2	
				I _{OLB} =12mA	2.7	—	0.4	
				I _{OLB} =18mA	3.0	—	0.4	
				I _{OLB} =24mA	3.0	—	0.55	
Input leakage current(DIR, /OE)		I _{IN}	V _{IN} =0 to 3.6V		2.7 to 3.6	—	±5.0	μ A
Power off leakage current		I _{OFF}	A, DIR, /OE=0 to 3.6V		0	—	5.0	μ A
3-state output off-state current		I _{OZA}	V _{INA} =V _{IH} or V _{IL} Vout=0 to 3.6V		2.7 to 3.6	—	±5.0	μ A
		I _{OZB}	V _{INB} =V _{IH} or V _{IL} Vout=0 or V _{CC}		2.7 to 3.6	—	±5.0	μ A
Quiescent supply current		I _{CC}	V _{IN} =V _{CC} or GND,		2.7 to 3.6	—	5.0	μ A
Increase in ICC per input		Δ I _{CC}	V _{IN} =V _{CC} -0.6V (per input)		2.7 to 3.6	—	750	μ A
Bushold input minimum drive hold current		I _{IHOLD}	V _{IN} =0.8V		3.0	75	—	μ A
			V _{IN} =2.0V			-75	—	
Bushold input over-drive current to change state		I _{IOD}	(Note 10)		3.6	—	550	μ A
			(Note 11)			—	-550	

Note 10: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 11: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta=-40 to 85°C, 2.3V ≤ Vcc ≤ 2.7V)

Parameter		Symbol	Test Condition		Vcc(V)	Min	Max	Unit
DC input voltage	H-level	V _{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V _{IL}	—		2.3 to 2.7	—	0.7	
Output voltage (A bus)	H-level	V _{OHA}	V _{IN} = V _{IH}	I _{OHA} =-100uA	2.3 to 2.7	V _{CC} -0.2	—	V
				I _{OHA} =-3mA	2.3	2.0	—	
				I _{OHA} =-6mA	2.3	1.8	—	
				I _{OHA} =-9mA	2.3	1.7	—	
	L-level	V _{OLA}	V _{IN} = V _{IL}	I _{OLA} =100uA	2.3 to 2.7	—	0.2	
				I _{OLA} =6mA	2.3	—	0.4	
				I _{OLA} =9mA	2.3	—	0.6	
Output voltage (B bus)	H-level	V _{OHB}	V _{IN} = V _{IH}	I _{OHB} =-100uA	2.3 to 2.7	V _{CC} -0.2	—	V
				I _{OHB} =-6mA	2.3	2.0	—	
				I _{OHB} =-12mA	2.3	1.8	—	
				I _{OHB} =-18mA	2.3	1.7	—	
	L-level	V _{OLB}	V _{IN} = V _{IL}	I _{OLB} =100uA	2.3 to 2.7	—	0.2	
				I _{OLB} =12mA	2.3	—	0.4	
				I _{OLB} =18mA	2.3	—	0.6	
Input leakage current(DIR,/OE)		I _{IN}	V _{IN} =0 to 3.6V		2.3 to 2.7	—	±5.0	μA
Power off leakage current		I _{OFF}	A,DIR,/OE=0 to 3.6V		0	—	5.0	μA
3-state output off-state current		I _{OZA}	V _{INA} =V _{IH} or V _{IL} Vout=0 to 3.6V		2.3 to 2.7	—	±5.0	μA
		I _{OZB}	V _{INB} =V _{IH} or V _{IL} Vout=0 or V _{CC}		2.3 to 2.7	—	±5.0	μA
Quiescent supply current		I _{CC}	V _{IN} =V _{CC} or GND,		2.3 to 2.7	—	5.0	μA
Bushold input minimum drive hold current		I _{IHOLD}	V _{IN} =0.7V		2.3	45	—	μA
			V _{IN} =1.6V			-45	—	
Bushold input over-drive current to change state		I _{IOD}	(Note 12)		2.7	—	400	μA
			(Note 13)			—	-400	

Note 12: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 13: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta=-40 to 85°C, 1.65V ≤ Vcc < 2.3V)

Parameter		Symbol	Test Condition		Vcc(V)	Min	Max	Unit
DC input voltage	H-level	V _{IH}	—		1.65 to 2.3	0.7 × V _{CC}	—	V
	L-level	V _{IL}	—		1.65 to 2.3	—	0.2 × V _{CC}	
Output voltage (A bus)	H-level	V _{OHA}	V _{IN} = V _{IH}	I _{OHA} =-100uA	1.65	V _{CC} -0.2	—	V
				I _{OHA} =-2mA	1.65	1.3	—	
	L-level	V _{OLA}	V _{IN} = V _{IL}	I _{OLA} =2mA	1.65	—	0.2	
Output voltage (B bus)	H-level	V _{OHB}	V _{IN} = V _{IH}	I _{OHB} =-100uA	1.65	V _{CC} -0.2	—	V
				I _{OHB} =-4mA	1.65	1.3	—	
	L-level	V _{OLB}	V _{IN} = V _{IL}	I _{OLB} =4mA	1.65	—	0.2	
Input leakage current(DIR,/OE)		I _{IN}	V _{IN} =0 to 3.6V		1.65 to 2.3	—	±5.0	μA
Power off leakage current		I _{OFF}	A,DIR,/OE=0 to 3.6V		0	—	5.0	μA
3-state output off-state current		I _{OZA}	V _{INA} =V _{IH} or V _{IL} Vout=0 to 3.6V		1.65 to 2.3	—	±5.0	μA
		I _{OZB}	V _{INB} =V _{IH} or V _{IL} Vout=0 or V _{CC}		1.65 to 2.3	—	±5.0	μA
Quiescent supply current		I _{CC}	V _{IN} =V _{CC} or GND,		1.65 to 2.3	—	5.0	μA
Bushold input minimum drive hold current		I _{I(HOLD)}	V _{IN} =0.33V		1.65	20	—	μA
			V _{IN} =1.16V			-20	—	
Bushold input over-drive current to change state		I _{I(OD)}	(Note 14)		1.95	—	300	μA
			(Note 15)			—	-300	

Note 14: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 15: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Characteristics (Ta=-40 to 85°C, Input: tr=tf=2.0ns, CL=30pF, RL=500Ω)

Parameter	Symbol	Test Condition	Vcc(V)	Min	Max	Unit
Propagation delay time	tpLH tpHL	Figure 1, Figure 2	1.8±0.15	1.0	10.0	ns
			2.5±0.2	0.8	4.6	
			3.3±0.3	0.6	3.0	
3-state output enable time	tpZL tpZH	Figure 1, Figure 3	1.8±0.15	1.0	15.0	ns
			2.5±0.2	0.8	7.8	
			3.3±0.3	0.6	5.6	
3-state output disable time	tpLZ tpHZ	Figure 1, Figure 3	1.8±0.15	1.0	6.5	ns
			2.5±0.2	0.8	4.3	
			3.3±0.3	0.6	3.9	
Output to output skew	tosLH tosHL	(Note 16)	1.8±0.15	—	0.5	ns
			2.5±0.2	—	0.5	
			3.3±0.3	—	0.5	

For CL=50pF, add approximately 300ps to the AC maximum specification.

Note 16: Parameter guaranteed by design.

$$(\text{tosLH} = |t_{\text{pLHm}} - t_{\text{pLHn}}|, \text{tosHL} = |t_{\text{pHLm}} - t_{\text{pHLn}}|)$$

Capacitive Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Vcc(V)	Typ.	Unit
Input capacitance	CIN		1.8,2.5,3.3	6	pF
Bus I/O capacitance	C I/O		1.8,2.5,3.3	7	pF
Power dissipation capacitance	CPDA	$\overline{\text{OE}} = \text{"L"} , f_{\text{inA}} = 100\text{MHz}$ Table 1 (Note 17)	1.8,2.5,3.3	20	pF
		$\overline{\text{OE}} = \text{"H"} , f_{\text{inA}} = 100\text{MHz}$ Table 1 (Note 17)		0	pF
Power dissipation capacitance	CPDB	$\overline{\text{OE}} = \text{"L"} , f_{\text{inB}} = 100\text{MHz}$ Table 1 (Note 17)	1.8,2.5,3.3	16	pF
		$\overline{\text{OE}} = \text{"H"} , f_{\text{inB}} = 100\text{MHz}$ Table 1 (Note 17)		1	pF

Note17: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

$$I_{\text{CC(opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot V_{\text{IN}} + I_{\text{CC}}/8(\text{per bit})$$

Table1 C_{PD} Test Condition

Function	Pin																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A bus /OE= "L"	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	C	L	V
A bus /OE= "H"	H	P	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	H	V
B bus /OE= "L"	L	C	O	O	O	O	O	O	O	G	X	X	X	X	X	X	X	P	L	V
B bus /OE= "H"	L	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	P	H	V

—Symbol explanation—

- V=V_{CC}(+3.3V)

G=GND(0V)

H=Logic1(V_{CC})

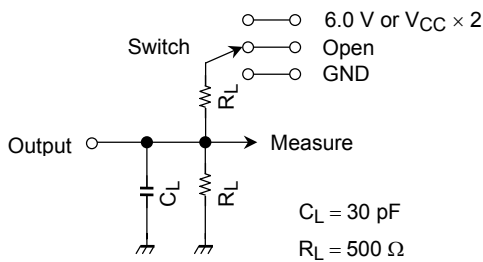
L=Logic0(GND)
- X=Don't care(Fixed to V_{CC} or GND)

O=Open

C=Connect a condenser(30pF) between output terminal and GND.

P=Input pulse with 50% duty cycle.

AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V @V _{CC} = 3.3 ± 0.3 V V _{CC} × 2 @V _{CC} = 2.5 ± 0.2 V @V _{CC} = 1.8 ± 0.15 V
t _{pHZ} , t _{pZH}	GND

Figure 1

AC Waveform

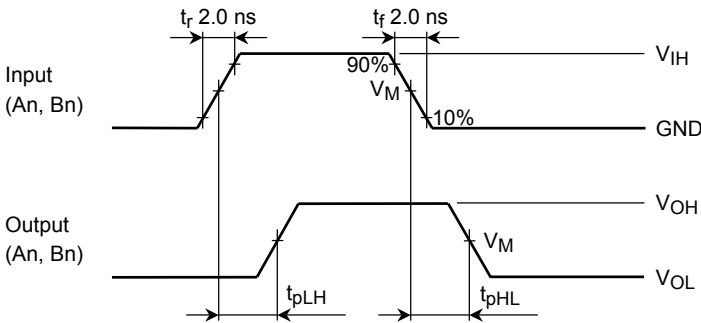


Figure 2 t_{pLH}, t_{pHL}

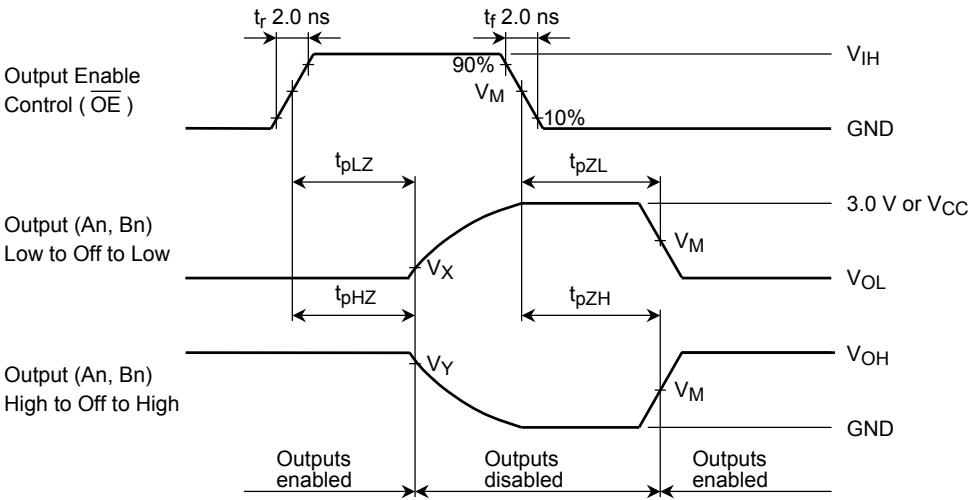


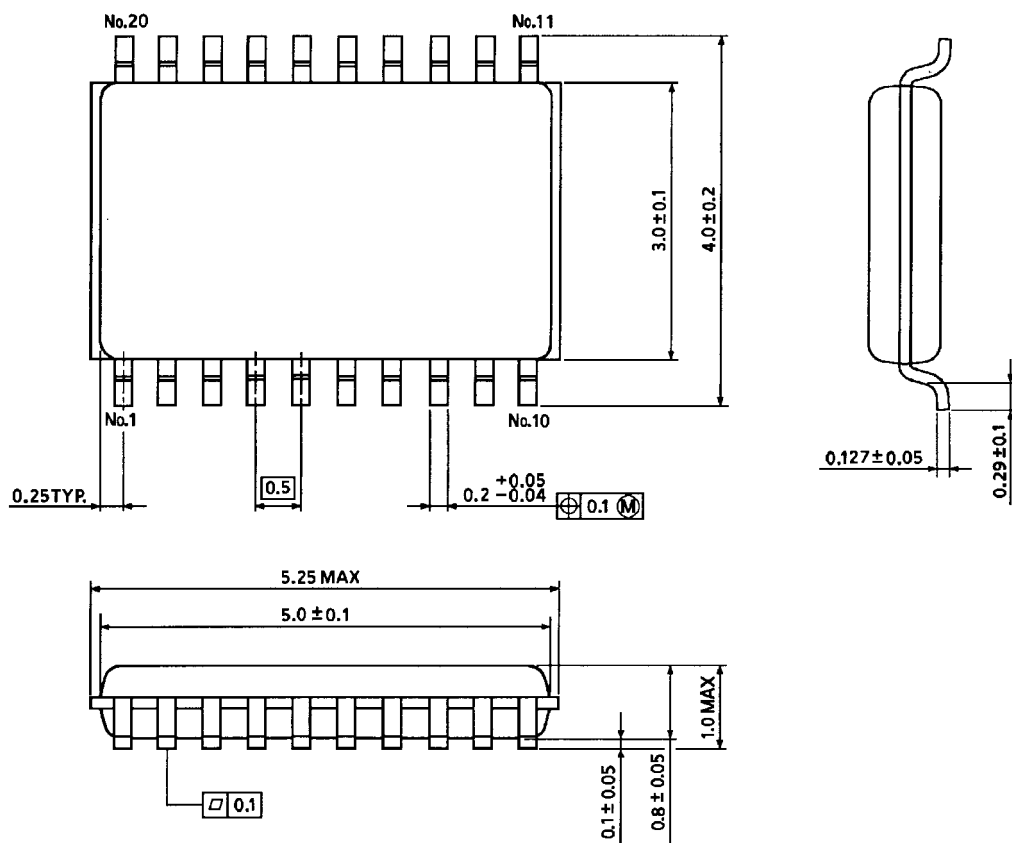
Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Symbol	V_{CC}		
	$3.3 \pm 0.3\text{ V}$	$2.5 \pm 0.2\text{ V}$	$1.8 \pm 0.15\text{ V}$
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.15\text{ V}$	$V_{OL} + 0.15\text{ V}$
V_Y	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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