DECEMBER 1972-REVISED MARCH 1988

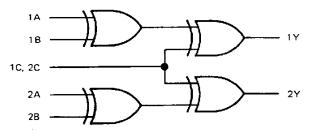
- Fully Compatible with Most TTL and TTL MSI Circuits
- Fully Schottky Clamping Reduces Delay Times . . . 8 ns Typical
- Can Operate as Exclusive-OR Gate (C Input Low) or as Exclusive-NOR Gate (C Input High)

FUNCTION TABLE

	INPUTS	OUTPUT	
Α	В	С	Y
L	L	L	L
L	Н	L	н
Н	L	L	н
Н	Н	L	L
L	L	н	н
L	н	Н	L
Н	L	Н	L
Н	Н	Н	H

H = high level, L = low level

logic diagram (one half)



(TOP VIEW) 1A 1 16 VCC 1B 2 15 4B 1Y 3 14 4A 1C,2C 4 13 4Y 2A 5 12 3C,4C 2B 6 11 3B

2Y 🛮 7

GND 8

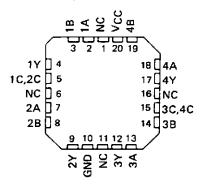
SN54S135 . . . J OR W PACKAGE

SN74S135 . . . D OR N PACKAGE

SN54S135 . . . FK PACKAGE (TOP VIEW)

10 🗌 3A

9 🗌 3Y

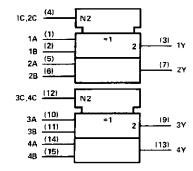


NC - No internal connection

positive logic

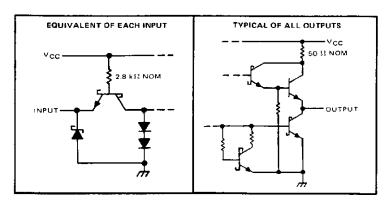
$$Y = A \oplus B \oplus C = AB\overline{C} + \overline{A}B\overline{C} - \overline{A}B\overline{C} + ABC$$

logic symbol†

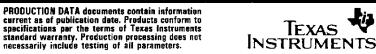


[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers are for D. J. N. and W packages.

schematics of inputs and outputs



Resistor values shown are nominal.



SN54S135, SN74S135 QUADRUPLE EXCLUSIVE OR/NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)												7 V
Input voltage		,									-	5,5 V
Operating free-air temperature range: SN54S135					,							–55°C to 125°C
SN74S135												0°C to 70°C
Storage temperature range						_	_	 _	_			-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	\	SN54S135					
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-1			-1	mΑ
Low-level output current, IOL			20			20	mA
Operating free-air temperature, TA	-65		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
VIK	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.2	v
VOH	High-level output voltage	VCC = MIN, VIH = 2 V, SN	V54S'	2.5	3.4		
		V ₁ L = 0.8 V, I _{OH} = -1 mA SN	V745'	2.7	3.4		V
VOL	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V,			0.5		T.,
*UL	Low-level output vortage	V _{IL} = 0.8 V, I _{OL} = 20 mA				0.5	\ \ \
lj .	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V				1	mΑ
Ιн	High-level input current	V _{CC} = MAX, V _I = 2.7 V				50	μА
ΊL	Low-level input current	V _{CC} = MAX, V ₁ = 0.5 V			-	2	mΑ
los	Short-circuit output current §	V _{CC} = MAX		-40		-100	mΑ
1 _{CC}	Supply current	V _{CC} = MAX, See Note 2			65	99	mΑ

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. $^{+}_{2}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TEST CON	MIN	TYP	MAX	UNIT	
tPLH	A or B	B A - I O - I			8.5	13	
[†] PHL		B or A = L, C = L	1		11	15	ns
^t PLH	A or B	B or A = H, C = L	†		8	12	
^t PHL	7	BUTA = H, C = L			9	13.5	ns
tPLH	A or B	D == A = 1	1,		10	15	
^t PHL		B or A = L, C = H	C _L = 15 pF,		6.5	10	ns
tPLH	A or B	D - A II O II	RL ≈ 280 Ω,		8.5	12	ns
t _{PHL}	7 4018	B or A = H, C = H	See Note 3	\vdash	7	13	
tPLH	С	4 - 0	7		8	12	
^t PHL	1	A = 8			9.5	14.5	ns
tPLH	С	A 4 B	1		7.5	11.5	
^t PHL	7	A ≠ B			-8	12	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: $I_{\mbox{\footnotesize{CC}}}$ is measured with the inputs grounded and the outputs open.

ww.ti.com 7-Jun-2010

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN54S135J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN74S135N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SN74S135N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54S135J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54S135J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54S135W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54S135W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	Samples Not Available

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54S135, SN74S135:



PACKAGE OPTION ADDENDUM

7-Jun-2010

● Catalog: SN74S135

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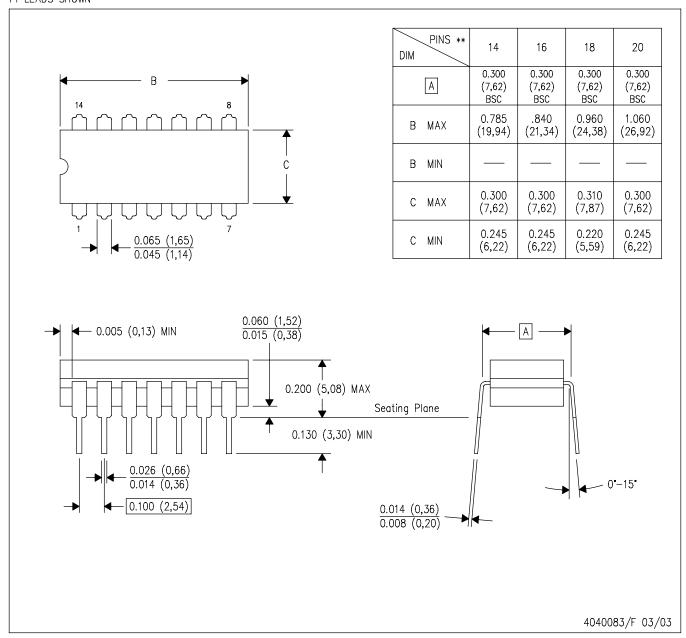
Military: SN54S135

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

14 LEADS SHOWN

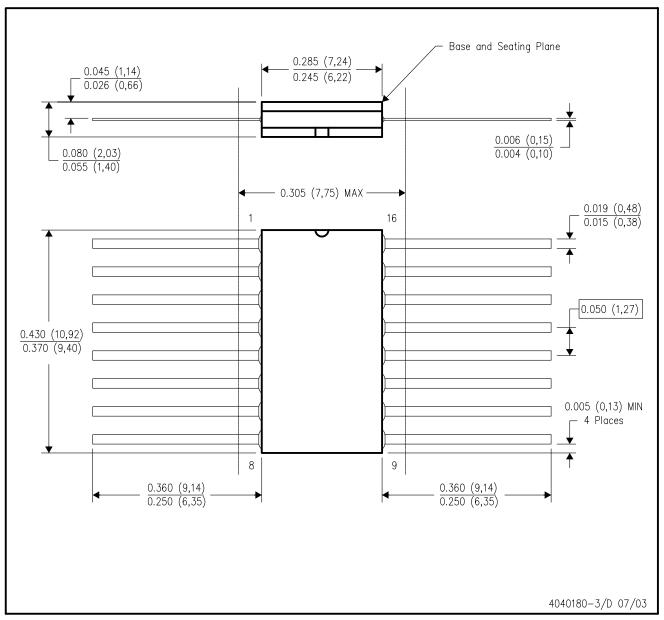


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



NOTES:

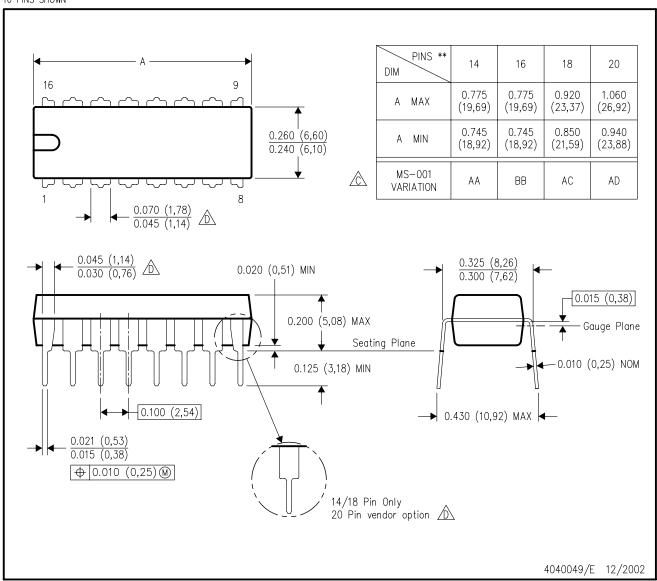
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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