

KA79L05A

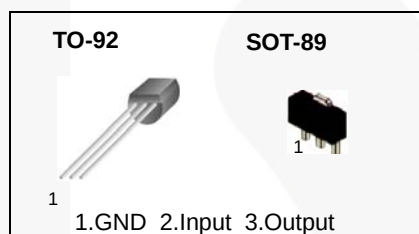
3-Terminal 0.1 A Negative Voltage Regulator

Features

- Output Current up to 100 mA
- No External Components
- Internal Thermal Over load Protection
- Internal Short-Circuit Current Limiting
- Output Voltage Offered in $\pm 5\%$ Tolerance
- Output Voltage: -5 V

Description

These regulators employ internal current limiting and thermal shutdown.



Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
KA79L05AMTF	0 ~ +125°C	9A	SOT-89	Tape and Reel
KA79L05AZTA		KA79L05AZ	TO-92	Ammo

Block Diagram

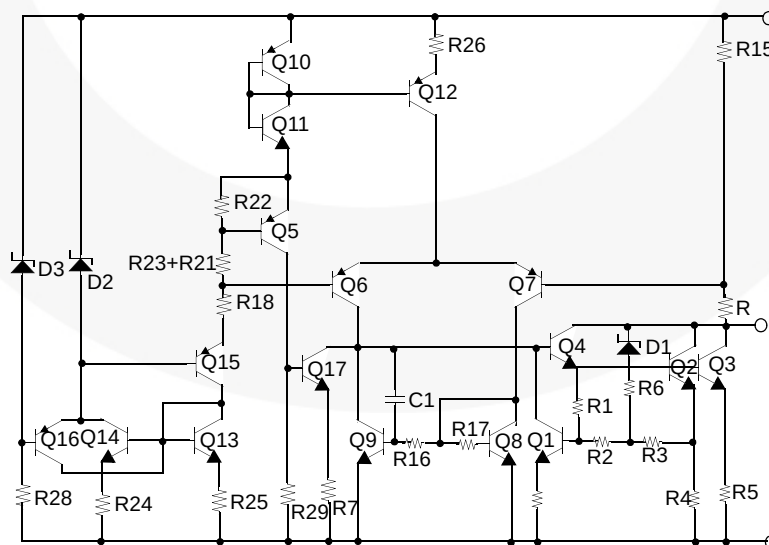


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_I	Input Voltage	-30	V
T_{OPR}	Operating Temperature Range	0 ~ +125	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-65 ~ +150	$^\circ\text{C}$

Electrical Characteristics

$V_I = -10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	$T_J = +25^\circ\text{C}$	-4.8	-5.0	-5.2	V
ΔV_O	Line Regulation ⁽¹⁾	$T_J = +25^\circ\text{C}$		15	150	mV
		$-7.0\text{ V} \geq V_I \geq -20\text{ V}$			100	mV
		$-8\text{ V} \geq V_I \geq -20\text{ V}$			100	mV
ΔV_O	Load Regulation ⁽¹⁾	$T_J = +25^\circ\text{C}$		20	60	mV
		$1.0\text{ mA} \leq I_O \leq 100\text{ mA}$		10	30	mV
		$1.0\text{ mA} \leq I_O \leq 40\text{ mA}$				mV
V_O	Output Voltage	$-7.0\text{ V} \geq V_I \geq -20\text{ V}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	-4.75		-5.25	V
		$V_I = -10\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	-4.75		-5.25	V
I_Q	Quiescent Current	$T_J = +25^\circ\text{C}$		2.0	5.5	mA
		$T_J = +125^\circ\text{C}$			6.0	mA
ΔI_Q	Quiescent Current Change	With Line			1.5	mA
ΔI_Q		With Load			0.1	mA
V_N	Output Noise Voltage	$T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		30		μV
RR	Ripple Rejection	$f = 120\text{ Hz}$, $-8\text{ V} \geq V_I \geq -18\text{ V}$, $T_J = +25^\circ\text{C}$	41	60		dB
V_D	Dropout Voltage	$T_J = +25^\circ\text{C}$		1.7		V

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Application

Design Considerations

The KA79L05A fixed voltage-regulator is designed with thermal overload protection that shuts down the circuit when subjected to an excessive power overload condition. Internal short-circuit protection limits the maximum current the circuit will pass. In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to ensure stable operation under all load conditions. A $0.33\ \mu\text{F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

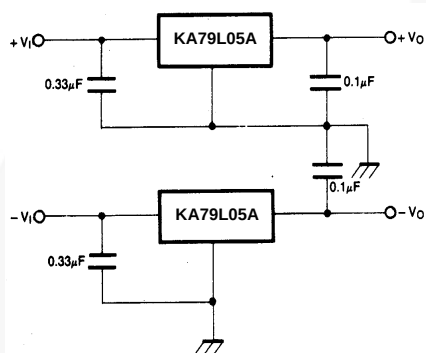


Figure 2. Positive and Negative Regulator

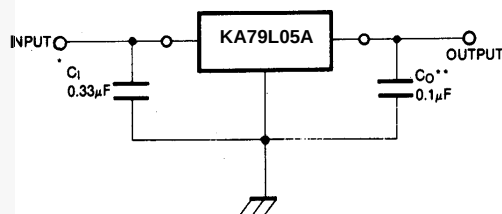


Figure 3. Typical Application

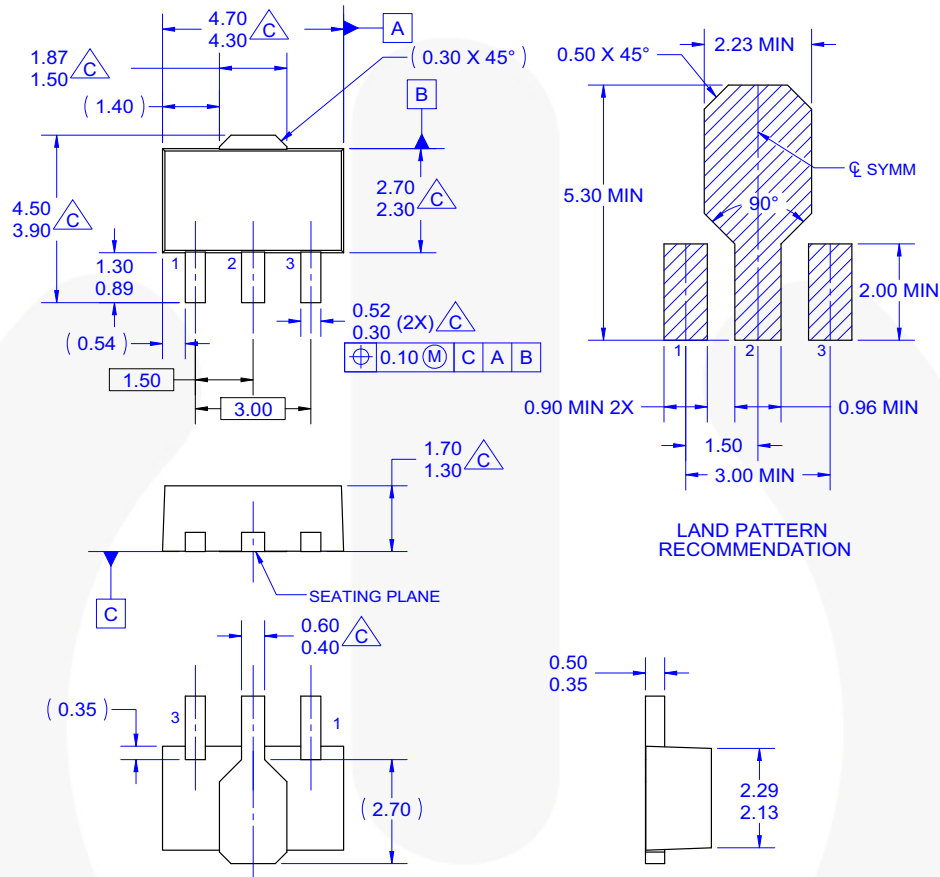
A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage, even during the low point on the input ripple voltage.

* C_I is required if regulator is located an appreciable distance from power supply filter.

** C_O improves stability and transient response.

Physical Dimensions

SOT-89



NOTES: UNLESS OTHERWISE SPECIFIED.

A. REFERENCE TO JEDEC TO-243 VARIATION AA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

$\triangle C$ DOES NOT COMPLY JEDEC STANDARD VALUE.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME
Y14.5-1994.
F. DRAWING FILE NAME: MA03CREV2

Figure 4. 3-Lead, SOT-89, JEDEC TO-243, Option AA

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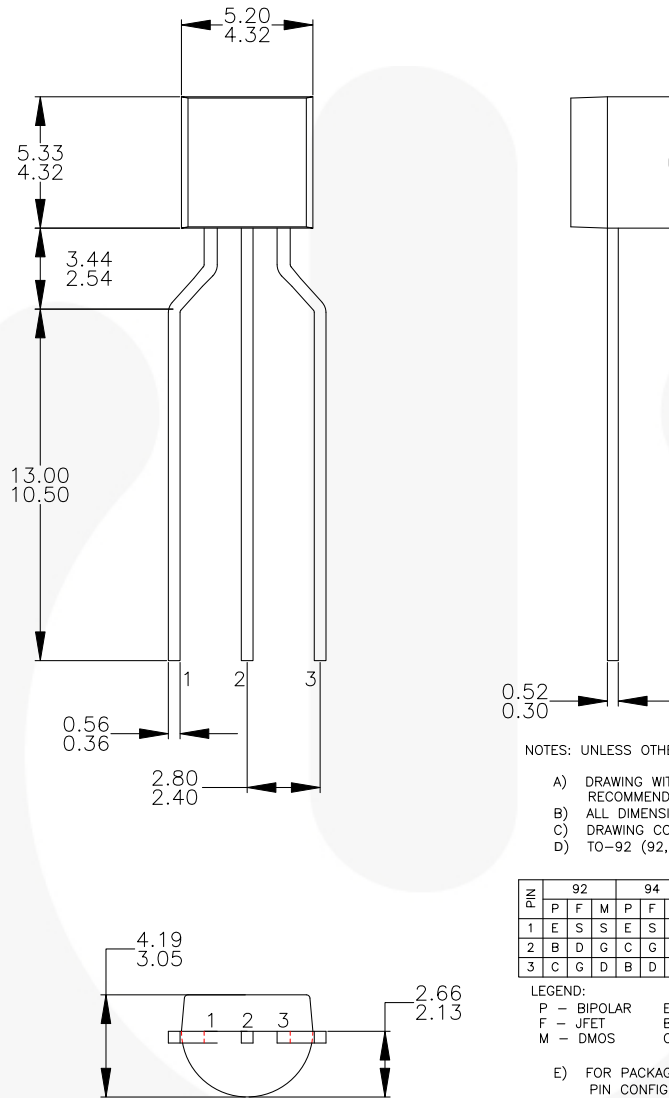
<http://www.fairchildsemi.com/packaging/>.

For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:

http://www.fairchildsemi.com/products/discrete/pdf/sot89_tr.pdf.

Physical Dimensions (Continued)

TO-92 Ammo Type



0.52
0.30

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DRAWING CONFORMS TO ASME Y14.5M-1994.
 D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR E - EMITTER D - DRAIN
 F - JFET B - BASE S - SOURCE
 M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98:
 PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
 ARE INTERCHANGEABLE AT JFET "F" OPTION.
 F) DRAWING FILENAME: MKT-ZA03FREV2.

Figure 5. 3-Lead, TO-92, Molded, 0.200 in Line Spacing Lead Form

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For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:

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