

## MM74HC139 Dual 2-To-4 Line Decoder

### General Description

The MM74HC139 decoder utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM74HC139 contain two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1, and B1 or A2, and B2) cause one of the four normally high outputs to go LOW.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally as well as pin

equivalent to the 74LS139. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

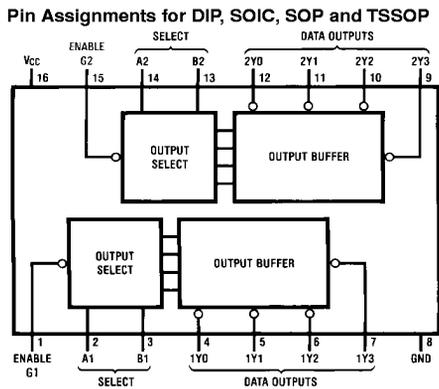
- Typical propagation delays —
  - Select to outputs (4 delays): 18 ns
  - Select to output (5 delays): 28 ns
  - Enable to output: 20 ns
- Low power: 40  $\mu$ W quiescent supply power
- Fanout of 10 LS-TTL devices
- Input current maximum 1  $\mu$ A, typical 10 pA

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC139M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC139SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC139MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP) JEDEC MO-153, 4.4mm Wide
MM74HC139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

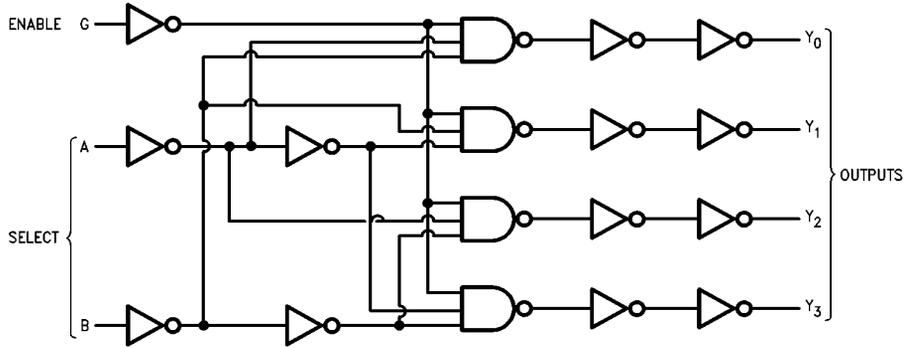


### Truth Table

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level  
L = LOW Level  
X = Don't Care

Logic Diagram



(1 of 2)

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions		Min	Max	Units
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V	Supply Voltage ( $V_{CC}$ )		2	6	V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$	DC Input or Output Voltage	( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$	Operating Temperature Range ( $T_A$ )		-40	+85	°C
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA	Input Rise or Fall Times	( $t_r, t_f$ ) $V_{CC} = 2.0V$		1000	ns
DC Output Current, per pin ( $I_{OUT}$ )	±25 mA		$V_{CC} = 4.5V$		500	ns
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±50 mA		$V_{CC} = 6.0V$		400	ns
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	<b>Note 1:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.				
Power Dissipation ( $P_D$ )		<b>Note 2:</b> Unless otherwise specified all voltages are referenced to ground.				
(Note 3)	600 mW	<b>Note 3:</b> Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.				
S.O. Package only	500 mW					
Lead Temperature ( $T_L$ )						
(Soldering 10 seconds)	260°C					

DC Electrical Characteristics (Note 4)				$T_A = 25^\circ C$	$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	Units	
Symbol	Parameter	Conditions	$V_{CC}$	Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC} \text{ or } GND$	6.0V		±0.1	±1.0	±1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC} \text{ or } GND$ $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics					
$V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$					
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Binary Select to any Output 4 levels of delay		18	30	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Binary Select to any Output 5 levels of delay		28	38	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Enable to any Output		19	30	ns

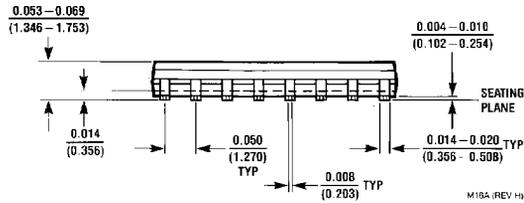
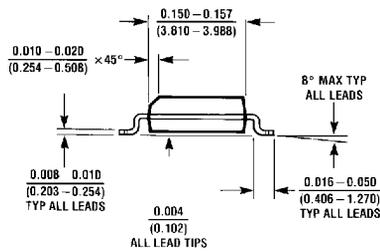
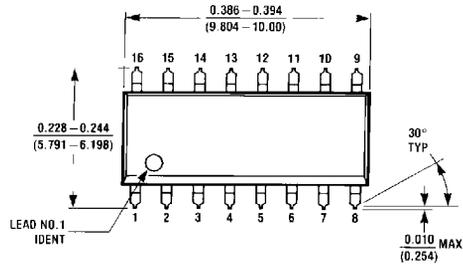
AC Electrical Characteristics								
$C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)								
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	Units
				Typ	Guaranteed Limits			
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Binary Select to any Output 4 levels of delay	(Note 5)	2.0V	110	175	219	254	ns
			4.5V	22	35	44	51	ns
			6.0V	18	30	38	44	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Binary Select to any Output 5 levels of delay	(Note 6)	2.0V	165	220	275	320	ns
			4.5V	33	44	55	64	ns
			6.0V	28	38	47	54	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Enable to any Output		2.0V	115	175	219	254	ns
			4.5V	23	35	44	51	ns
			6.0V	19	30	38	44	ns
$t_{TLH}, t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{IN}$	Maximum Input Capacitance			3	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (Note 7)	(Note 7)		75				pF

**Note 5:** 4 levels of delay are A to Y1, Y3 and B to Y2, Y3.

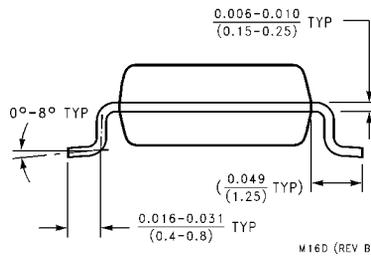
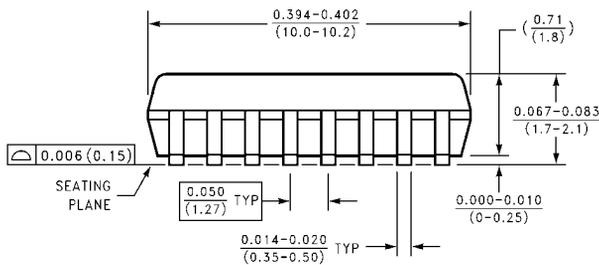
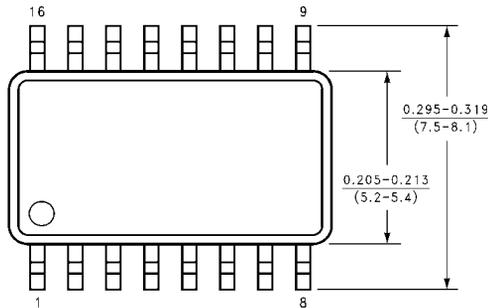
**Note 6:** 5 levels of delay are A to Y0, Y2 and B to Y0, Y1.

**Note 7:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

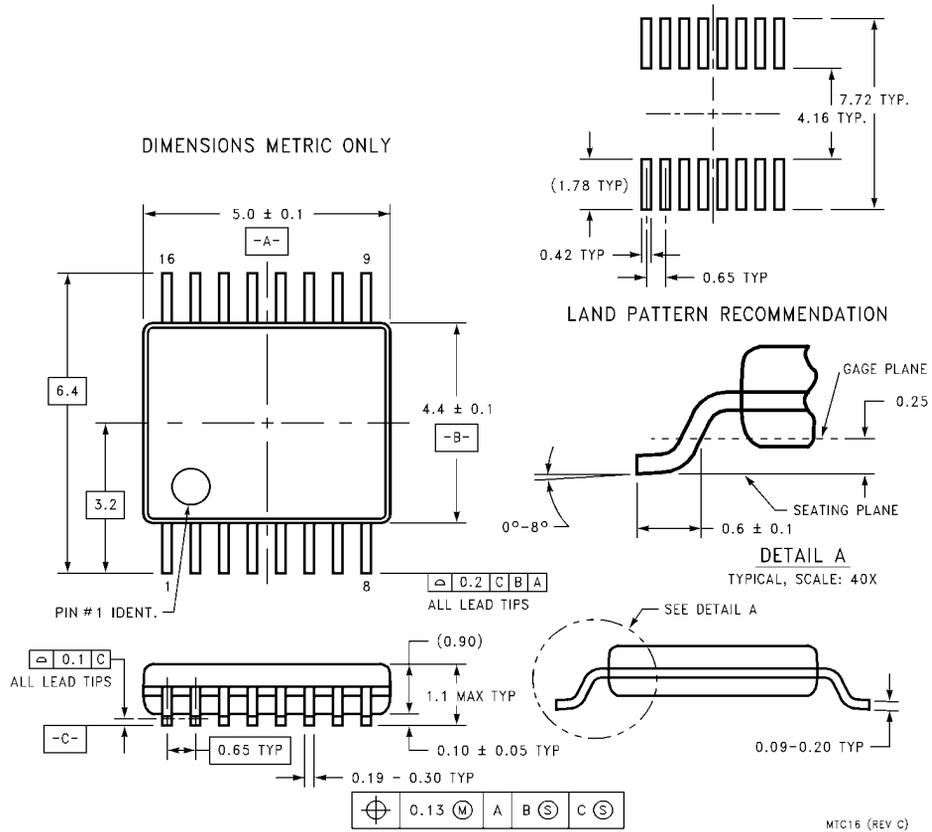


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



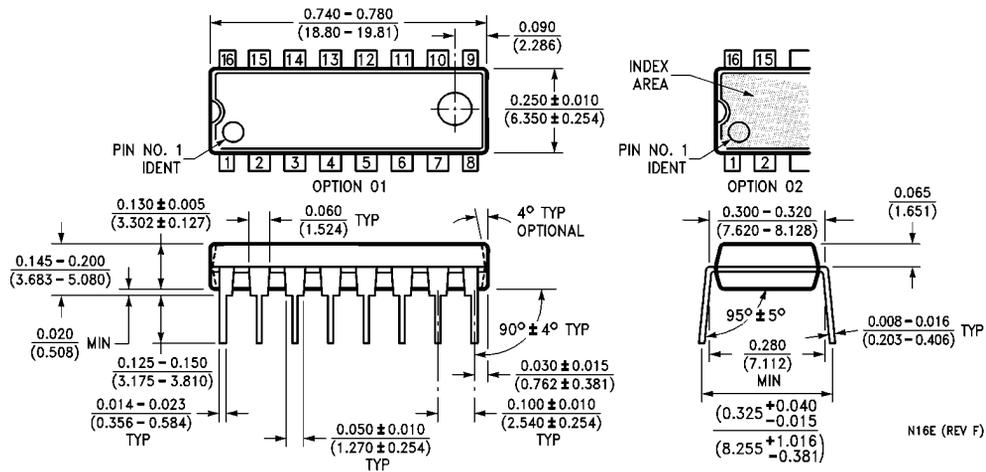
**16-Lead Small Outline Package (SOP) EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

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