

MC74LVX244

Octal Bus Buffer

With 5V-Tolerant Inputs

The MC74LVX244 is an advanced high speed CMOS non-inverting 3-state octal bus buffer and has two active low output enables. It is also designed to work with 3-state memory address drivers, etc. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

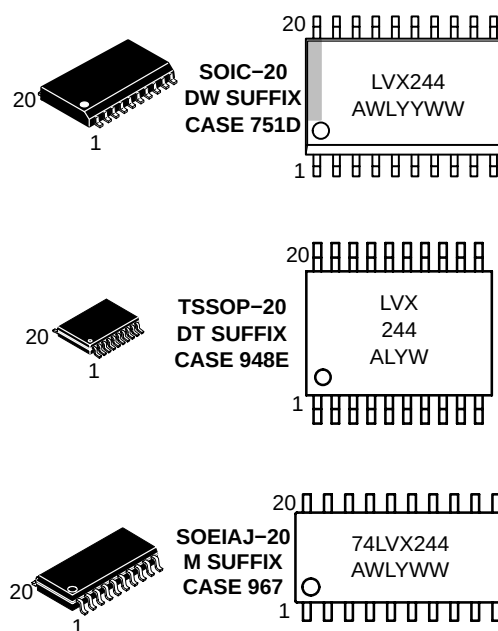
- High Speed: $t_{PD} = 4.7$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Pb-Free Packages are Available*



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MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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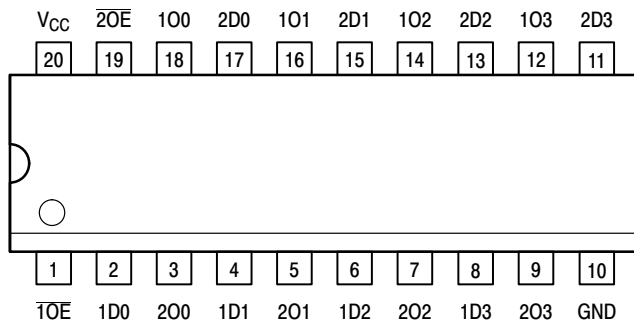


Figure 1. 20-Lead Pinout (Top View)

PIN NAMES

Pins	Function
$\overline{1OE}$, $\overline{2OE}$	Output Enable Inputs
1Dn, 2Dn	Data Inputs
1On, 2On	3-State Outputs

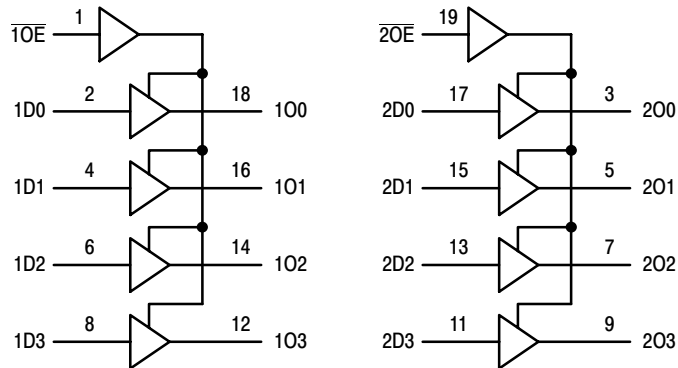


Figure 2. Logic Diagram

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{1OE}$, $\overline{2OE}$	1Dn, 2Dn	1On, 2On
L	L	L
L	H	H
H	X	Z

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX244DWR2	SOIC-20	1000 Tape & Reel
MC74LVX244DWR2G	SOIC-20 (Pb-Free)	1000 Tape & Reel
MC74LVX244DT	TSSOP-20*	50 Units / Rail
MC74LVX244DTR2	TSSOP-20*	2500 Tape & Reel
MC74LVX244M	SOEIAJ-20	50 Units / Rail
MC74LVX244MEL	SOEIAJ-20	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{in}	DC Input Voltage	-0.5 to +7.0	V
V_{out}	DC Output Voltage	-0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OH} = -50\mu\text{A}$ $I_{OH} = -50\mu\text{A}$ $I_{OH} = -4\text{mA}$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OL} = 50\mu\text{A}$ $I_{OL} = 50\mu\text{A}$ $I_{OL} = 4\text{mA}$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	$V_{in} = 5.5\text{V}$ or GND	3.6			±0.1		±1.0	μA
I_{OZ}	Maximum 3-State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	3.6			±0.2 5		±2.5	μA
I_{CC}	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		6.1 8.6	11.4 14.9	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		4.7 7.2	7.1 10.6	1.0 1.0	8.5 12.0	
t_{PZL} , t_{PZH}	Output Enable Time to High and Low Level	$V_{CC} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		7.1 9.6	13.8 17.3	1.0 1.0	16.5 20.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.5 8.0	8.8 12.3	1.0 1.0	10.5 14.0	
t_{PLZ} , t_{PHZ}	Output Disable Time From High and Low Level	$V_{CC} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		11.6	16.0	1.0	19.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		9.7	11.4	1.0	13.0	
t_{OSHL} , t_{OSLH}	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ $C_L = 50\text{pF}$			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three-State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		19				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 3.3\text{V}$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.5	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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SWITCHING WAVEFORMS

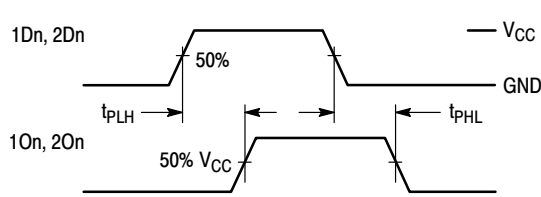


Figure 3.

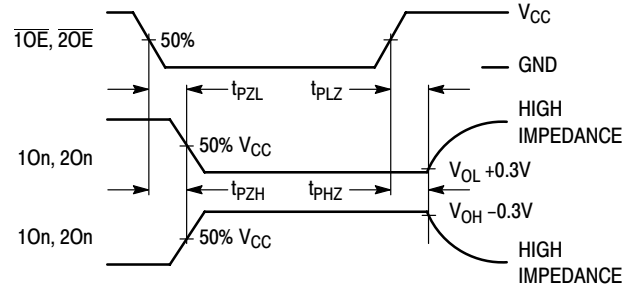
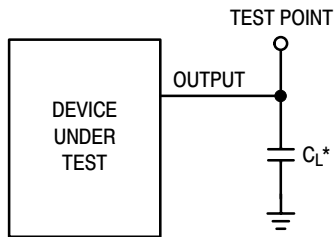


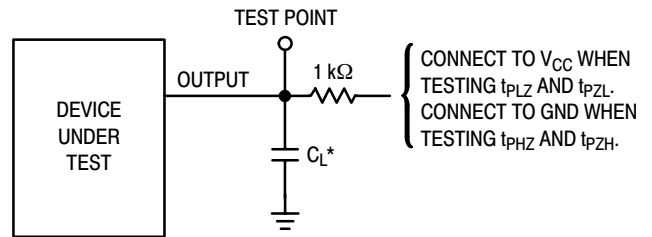
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



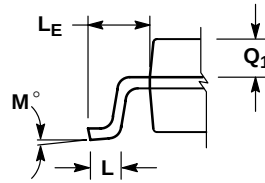
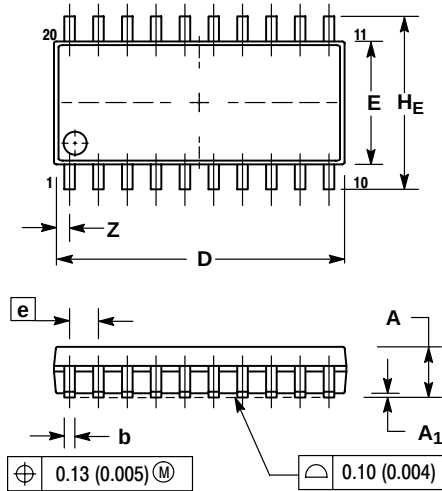
*Includes all probe and jig capacitance

Figure 6. Three-State Test Circuit

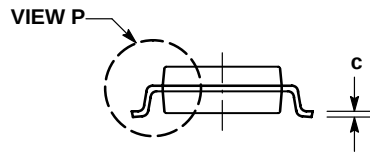
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PACKAGE DIMENSIONS

SOEIAJ-20
M SUFFIX
CASE 967-01
ISSUE O



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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