

## Features

- 2X CLK\_IN on CLK\_OUT
- High-Performance Phase-Locked-Loop Clock Distribution for Networking, ATM, 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter  $\pm 100\text{ps}$  max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V<sub>CC</sub>
- Wide range of Clock Frequencies
- Packaging (Pb-free & Green available):  
- 8-pin SOIC Package (W)

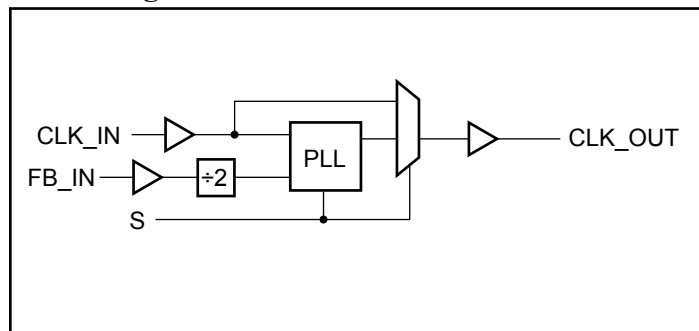
## Description

The PI6C2402 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the feedback CLK\_OUT output to the feedback FB\_IN input, the propagation delay from the CLK\_IN input to any clock output will be nearly zero. The PI6C2402 provides 2X CLK\_IN on CLK\_OUT output.

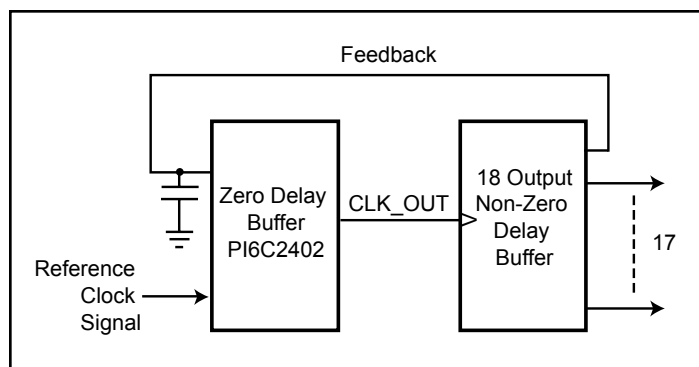
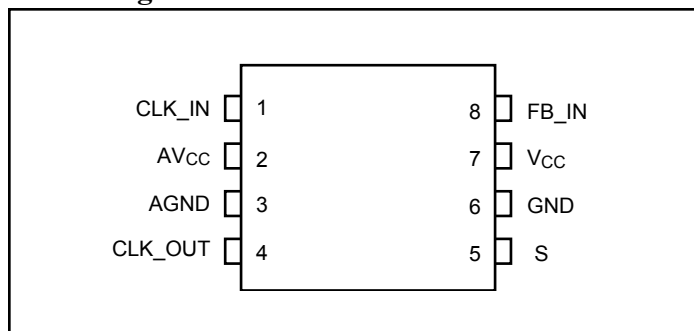
## Applications

If the system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as PI6C2509, and PI6C2510, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

## Block Diagram



## Pin Configuration



**Figure 1. This Combination Provides Zero-Delay Between the Reference Clocks Signal and 17 Outputs**

## Control Input

S	Outputs Source	PLL Shutdown
1	PLL	N
0	CLK_IN	Y

**Pin Functions**

Name	Number	Type	Description
CLK_IN	1	I	Reference Clock input, CLK_IN allows spread spectrum clock input
AVCC	2	Power	Analog Power
AGND	3	Ground	Analog Ground
CLK_OUT	4	O	Clock Output. The output provides low-skew copies of CLK_IN and has an embedded series-damping resistor.
S	5	I	Control Input S. S is used to bypass the PLL for test purposes. When S is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs
GND	6	Ground	Ground
VCC	7	Power	Power Supply
FB_IN	8	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.

**Absolute Maximum Ratings** (Over operating free-air temperature range<sup>(1)</sup>)

Symbol	Test Conditions	Min.	Max.	Units
V <sub>I</sub>	Input voltage range	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range	-0.5	V <sub>CC</sub> + 0.5	
V <sub>I</sub> _DC	DC input voltage	-0.5	5.0	
I <sub>O</sub> _DC	DC output current		100	mA
Power	Maximum power dissipation at TA = 55°C in still air		1.0	W
T <sub>STG</sub>	Storage temperature	-65	150	°C

**Note:**

1. Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

**Recommended Operating Conditions**

Symbol	Test Conditions	Temperature	Min.	Max.	Units
V <sub>CC</sub>	Supply Voltage	Commercial	3.0	3.6	V
		Industrial	3.135	3.465	
V <sub>IH</sub>	High Level input voltage		2.0		
V <sub>IL</sub>	Low Level input voltage			0.8	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	
T <sub>A</sub>	Operating free-air temperature	Commercial	0	70	°C
		Industrial	-40	85	

### Electrical Characteristics

(Over recommended operating free-air temperature range)

Symbol	Test Conditions	Temperature	V <sub>CC</sub>	Min.	Typ.	Max.	Units
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 <sup>(1)</sup>	Commercial	3.6V			10	μA
		Industrial	3.465V			10	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3V		4		pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3V		6		
I <sub>OH</sub>	V <sub>OUT</sub> = 2.4V					-12	mA
	V <sub>OUT</sub> = 2.0V					-18	
I <sub>OL</sub>	V <sub>OUT</sub> = 0.8V			18			
	V <sub>OUT</sub> = 0.55V			12			

**Notes:**

1. Continuous Output Current

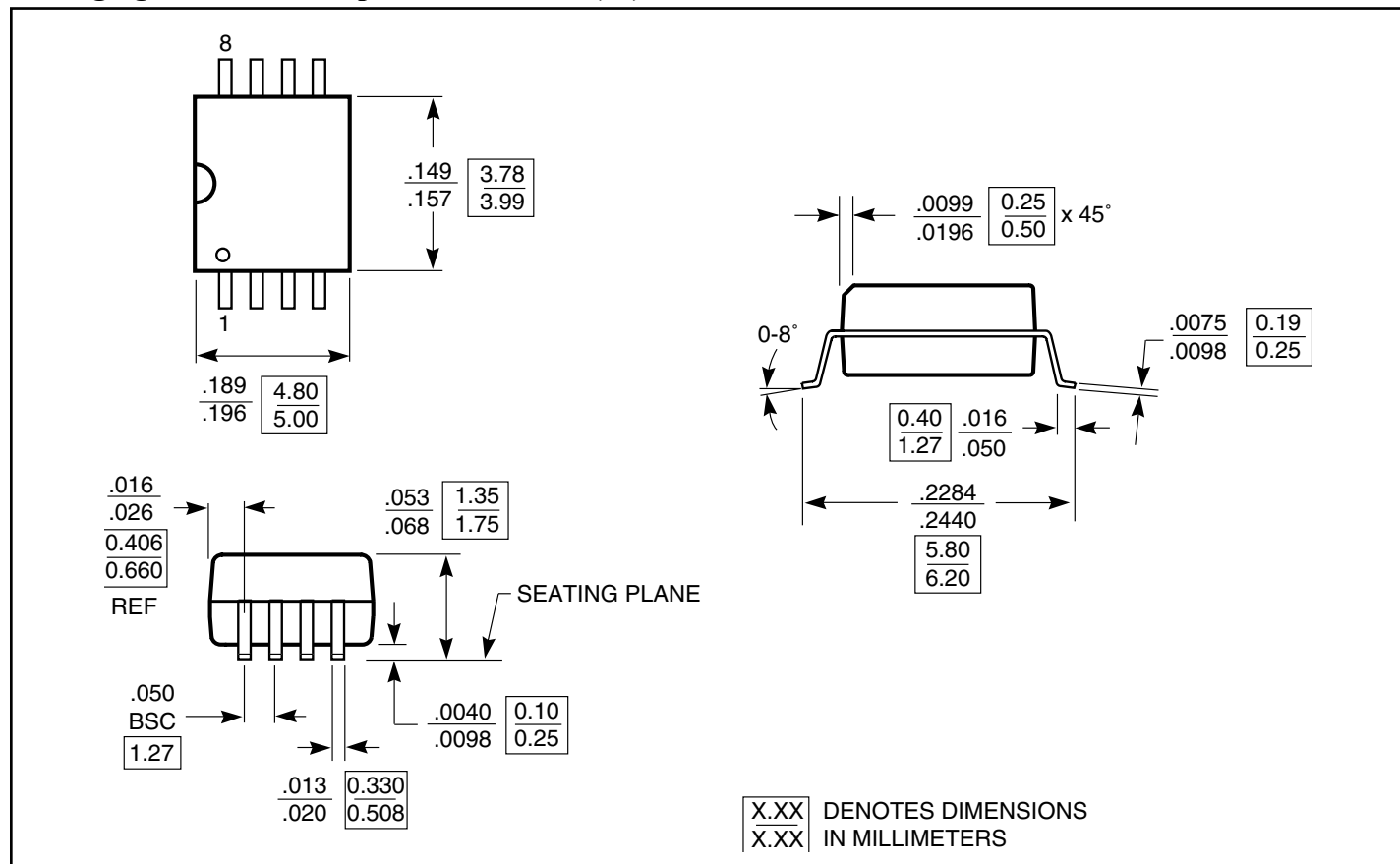
### AC Specifications Timing Requirements

(Over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 25pF)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
F <sub>CLOCK</sub>	Clock Frequency	Commercial	25		134	MHz
		Industrial	25		100	
D <sub>CYI</sub>	Input clock duty cycle		40		60	%
	Stabilization time after power up				1	ms
t <sub>p</sub>	Phase error without jitter <sup>(1)</sup>	CLK_IN↑ at 100MHz and 66MHz	-150		150	ps
t <sub>j</sub>	Jitter, cycle-to-cycle	At 100MHz and 66MHz	-100		100	
	Duty Cycle		45		55	%
t <sub>r</sub>	Rise-time 0.4V to 2.0V			1.0		ns
t <sub>f</sub>	Fall-time 2.0V to 0.4V			1.1		

**Notes:**

1. This switching parameter is guaranteed by design.

**Packaging Mechanical: 8-pin Plastic SOIC (W)**

**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C2402W	W	8-pin, 150-mil SOIC
PI6C2402WE	W	Pb-free & Green, 8-pin, 150-mil SOIC

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. Number of Transistors = TBD