

# Smart Dual Current Sense Switch

## Basic Features

- Overload Protection
- DMOS Overtemperature protection
- Overvoltage protection
- Open load detection
- Current limitation
- Low quiescent current mode
- 3,3V  $\mu$ C compatible input
- **Electrostatic discharge (ESD) protection**

## Product Summary

|                      |              |               |
|----------------------|--------------|---------------|
| Supply voltage       | $V_S$        | 4.5 – 5.5 V   |
| Drain source voltage | $V_{DS(AZ)}$ | 48 - 60 V     |
| On resistance        | $R_{ON}$     | 0.18 $\Omega$ |

## Specific Features

- Proportional load current sense
- IC Overtemperature warning
- 8-Bit SPI (for diagnosis and control)
- Short to GND detection
- Programmable overload behaviour

## P-DSO-12-4

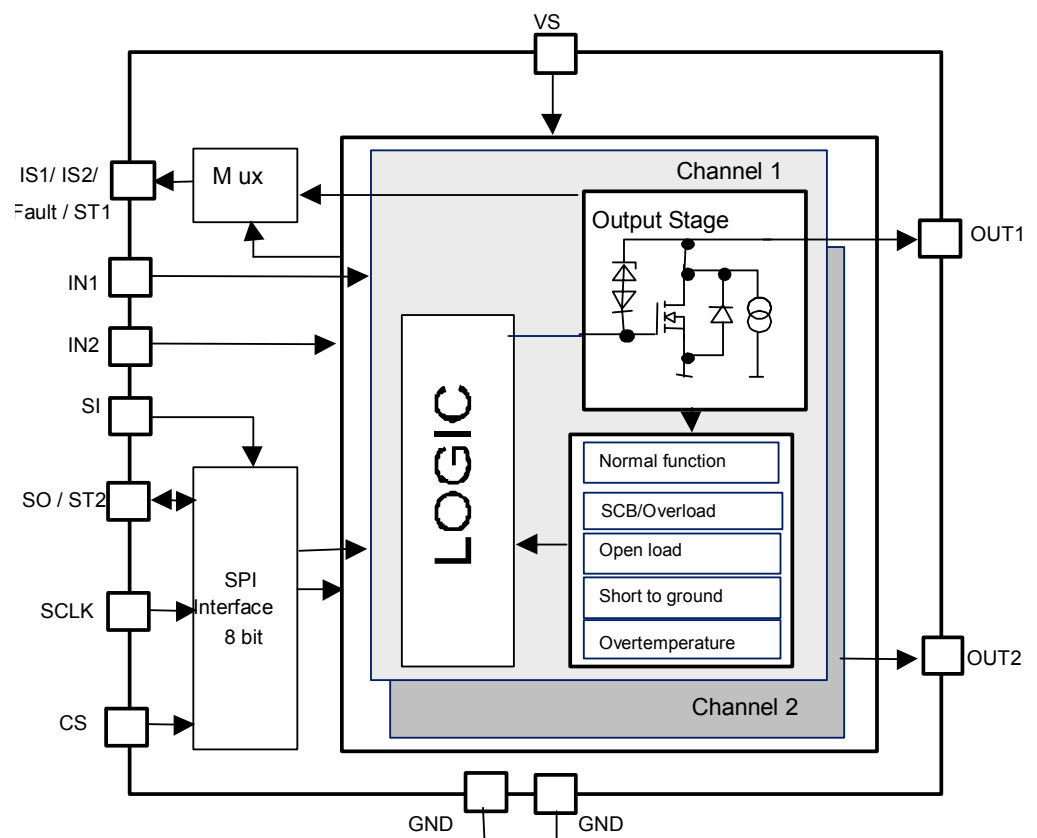


Ordering Code :  
Q67007-A9698

## General Description

Dual Current Sense Low-Side Switch in Smart Power Technology (SPT) with two open drain DMOS output stages. The TLE 6214 L is protected by embedded protection functions and designed for automotive applications. The output stages can be controlled directly by parallel inputs for PWM applications (e.g. Oxygen Probe Heater, Stepper Motor) or by SPI. All output stages can provide a load current proportional sense signal. Diagnosis is done by an 8 bit SPI or by one status output per channel.

## Block Diagram



**Pin Description**

| Pin | Symbol | Function                               |
|-----|--------|----------------------------------------|
| 1   | IN2    | Input Channel 2                        |
| 2   | SI     | SPI Signal In                          |
| 3   | OUT2   | Power Output Channel 2                 |
| 4   | CO1    | Current Sense 1/2 / Fault / Status Ch1 |
| 5   | SCLK   | SPI Clock                              |
| 6   | GND    | Ground                                 |
| 7   | IN1    | Input Channel 1                        |
| 8   | CS     | SPI Chip Select                        |
| 9   | OUT1   | Power Output Channel 1                 |
| 10  | VS     | Supply Voltage                         |
| 11  | CO2    | SPI Signal Out / Status Ch2            |
| 12  | GND    | Ground                                 |

**Pin Configuration (Top view)**

|      |   |    |      |
|------|---|----|------|
| IN 2 | 1 | 12 | GND  |
| SI   | 2 | 11 | CO 2 |
| OUT2 | 3 | 10 | VS   |
| CO 1 | 4 | 9  | OUT1 |
| SCLK | 5 | 8  | CS   |
| GND  | 6 | 7  | IN 1 |

Power P-DSO -12

Both GND pins and heat sink must be connected to GND externally.

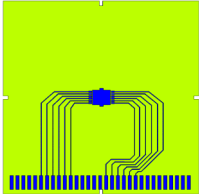
**Maximum Ratings for  $T_j = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$** 

| Parameter                                                                                                                                                           | Symbol           | Values                       | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------------------|------|
| Supply Voltage                                                                                                                                                      | $V_S$            | -0.3 ... +7                  | V    |
| Continuous Drain Source Voltage (OUT1...OUT2)                                                                                                                       | $V_{DS}$         | -0.3 ... +48                 | V    |
| Input Voltage, All Inputs and Data outputs, Sense Lines                                                                                                             | $V_{IN}$         | - 0.3 ... + 7                | V    |
| Output Current per Channel <sup>1)</sup>                                                                                                                            | $I_D$            | $I_{D(lim1,2) \text{ min.}}$ | A    |
| Reverse Current per channel                                                                                                                                         | $I_{rev}$        | -3                           | A    |
| Output Clamping Energy (single event); linear decreasing current<br>$I_D = 2\text{A}$ , $T_{J \text{ start}} = 150^{\circ}\text{C}$ ; max. 100 cycles over lifetime | $E_{AS}$         | 75                           | mJ   |
| Maximum Voltage for short circuit Protection (single event) <sup>2)</sup>                                                                                           | $V_{SC, single}$ | 48                           | V    |
| Current Limit 2, slew rate 1 (default setting)                                                                                                                      |                  | 32                           |      |
| Current Limit 2, slew rate 2                                                                                                                                        |                  | 18                           |      |
| Current Limit 1, slew rate 1 / 2                                                                                                                                    |                  |                              |      |
| <b>Electrostatic Discharge Voltage</b> (human body model)<br>according to EIA/JESD22-A114-E                                                                         | $V_{ESD}$        |                              |      |
| Output Pins                                                                                                                                                         |                  | 4000                         | V    |
| All other Pins                                                                                                                                                      |                  | 2000                         | V    |
| DIN Humidity Category, DIN 40 040                                                                                                                                   |                  | E                            |      |
| IEC Climatic Category, DIN IEC 68-1                                                                                                                                 |                  | 40/150/56                    |      |

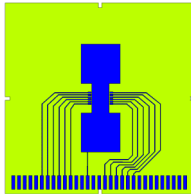
<sup>1)</sup> Output current rating as long as maximum junction temperature is not exceeded. The maximum output current has to be calculated using  $R_{thJA}$  according mounting conditions.

<sup>2)</sup> Device mounted on PCB (50mm x 50mm x 1,5mm epoxy, FR4) with 6cm<sup>2</sup> copper heatsink area (one layer, 70µm thick); PCB in test chamber with blown air

|                                                                  |            |     |     |
|------------------------------------------------------------------|------------|-----|-----|
| Thermal resistance                                               |            |     |     |
| junction - case                                                  | $R_{thJC}$ | 2   | K/W |
| junction - ambient @ min. footprint                              | $R_{thJA}$ | 105 | K/W |
| junction - ambient @ 6 cm <sup>2</sup> cooling area <sup>1</sup> |            | 45  | K/W |



PCB with min footprint


 PCB with 6 cm<sup>2</sup> copper cooling area

## Electrical Characteristics

| Parameter and Conditions<br>$V_S = 4.5V - 5.5V$ ; $T_J = -40^\circ C$ to $+150^\circ C$<br>(unless otherwise specified) | Symbol | Values |     |     | Unit |
|-------------------------------------------------------------------------------------------------------------------------|--------|--------|-----|-----|------|
|                                                                                                                         |        | min    | typ | max |      |

### 1. Power Supply

|                                              |                |     |    |     |    |
|----------------------------------------------|----------------|-----|----|-----|----|
| Supply Voltage                               | $V_S$          | 4.5 | -- | 5.5 | V  |
| Supply Current                               | $I_S$          | --  |    | 5   | mA |
| Supply Current in Sleep Mode (CS = H)        | $I_{S(sleep)}$ | --  | -- | 10  | μA |
| Wake up Time (after sleep mode) <sup>2</sup> | $t_{wake}$     |     |    | 100 | μs |

### 2. Power Outputs

|                                            |                                               |               |    |      |      |    |
|--------------------------------------------|-----------------------------------------------|---------------|----|------|------|----|
| ON Resistance $V_S = 5V$ ; $I_D = 2A$      | $T_J = 25^\circ C$                            | $R_{DS(ON)}$  | -- | 0.18 | 0.22 | Ω  |
|                                            | $T_J = 125^\circ C$                           |               | -- | 0.27 | 0.32 |    |
|                                            | $T_J = 150^\circ C$                           |               | -- | 0.3  | 0.36 |    |
|                                            |                                               |               |    |      |      |    |
| Output Clamping Voltage                    | output OFF                                    | $V_{DS(AZ)}$  | 48 | --   | 60   | V  |
| Current Limit 1: Current limitation        |                                               | $I_{D(lim1)}$ | 5  | 6.5  | 8    | A  |
| Current Limit 2 :Overload switch off       | $V_S \geq 5V$                                 | $I_{D(lim2)}$ | 9  | 10,5 | 12   | A  |
|                                            | $V_S < 5V$ , $T_J \leq 125^\circ C$           |               | 9  |      | 12   |    |
|                                            | $V_S < 5V$ , $T_J > 125^\circ C$ <sup>2</sup> |               | 8  |      | 12   |    |
|                                            |                                               |               |    |      |      |    |
| Reverse Current per channel <sup>2,3</sup> |                                               | $I_{rev}$     |    |      | 2    | A  |
| Output Leakage Current                     | Sleep mode active                             | $I_{D(Ikg)}$  | -- | --   | 5    | μA |
| Turn-On Time 1                             | $I_D = 2A$ , resistive load                   | $t_{ON}$      | -- | 5    | 10   | μs |
| Turn-On Time 2                             | $I_D = 2A$ , resistive load                   |               |    | 20   | 50   |    |
| Turn-Off Time 1                            | $I_D = 2A$ , resistive load                   | $t_{OFF}$     | -- | 5    | 10   | μs |
| Turn-Off Time 2                            | $I_D = 2A$ , resistive load                   |               |    | 20   | 50   |    |

<sup>1</sup> Device mounted on PCB (50mm x 50mm x 1,5mm epoxy, FR4) with 6cm<sup>2</sup> copper heatsink area (one layer, 70μm thick); PCB in test chamber with blown air

<sup>2</sup> This parameter is not subject to production test

<sup>3</sup> without loss of function, supply current can be  $I_S > 5mA$

|                    |                                      |           |   |   |    |           |
|--------------------|--------------------------------------|-----------|---|---|----|-----------|
| Turn On slew rate  | $U_{DS}$ 80% to 30%, $V_{bat} = 14V$ | $S_{ON}$  |   |   |    | $V/\mu s$ |
| Slew rate 1        | $I_D = 2 A$ , resistive load         |           | 1 | 5 | 20 |           |
| Slew rate 2        | $I_D = 2 A$ , resistive load         |           |   | 1 | 5  |           |
| Turn Off slew rate | $U_{DS}$ 30% to 80%, $V_{bat} = 14V$ | $S_{OFF}$ |   |   |    | $V/\mu s$ |
| Slew rate 1        | $I_D = 2 A$ , resistive load         |           | 1 | 5 | 20 |           |
| Slew rate 2        | $I_D = 2 A$ , resistive load         |           |   | 1 | 5  |           |

### 3. Digital Inputs

|                                       |                   |     |     |     |         |
|---------------------------------------|-------------------|-----|-----|-----|---------|
| Input Low Voltage                     | $V_{INL}$         | --  | --  | 1.0 | V       |
| Input High Voltage                    | $V_{INH}$         | 2.0 | --  | --  | V       |
| Input Voltage Hysteresis <sup>2</sup> | $V_{INHys}$       | 100 | 200 | 400 | mV      |
| Input Pull Down Current (IN1 ... IN2) | $I_{IN(1..2)}$    | 20  | 50  | 100 | $\mu A$ |
| Input Pull Down Current (SI, SCLK)    | $I_{IN(SI,SCLK)}$ | 10  | 20  | 50  | $\mu A$ |
| Input Pull Up Current (CS)            | $I_{IN(CS)}$      | 10  | 20  | 50  | $\mu A$ |

### 4. Digital Outputs (SO, $\overline{FAULT}$ , Status 1/2)

|                                  |                                  |              |             |    |     |         |
|----------------------------------|----------------------------------|--------------|-------------|----|-----|---------|
| SO High State Output Voltage     | $I_{SOH} = 2 mA$                 | $V_{SOH}$    | $V_S - 0.4$ | -- | --  | V       |
| SO Low State Output Voltage      | $I_{SOL} = 2.5 mA$               | $V_{SOL}$    | --          | -- | 0.4 | V       |
| Output Tri-state Leakage Current | CS = H, $0 \leq V_{SO} \leq V_S$ | $I_{SOLkg}$  | -10         | 0  | 10  | $\mu A$ |
| FAULT Output Low Voltage         | $I_{FAULT} = 1.6 mA$             | $V_{FAULTL}$ | --          | -- | 0.4 | V       |
| Status Output Low Voltage        | $I_{ST} = 1.6 mA$                | $V_{ST}$     |             |    | 0.4 | V       |

### 5. SPI

|                                                                         |                         |             |     |     |     |    |
|-------------------------------------------------------------------------|-------------------------|-------------|-----|-----|-----|----|
| Serial Clock Frequency (depending on SO load)                           | $f_{SCK}$               | DC          | --  | 5   | MHz |    |
| Serial Clock Period (1/fsclock)                                         | $t_{p(SCK)}$            | 200         | --  | --  | ns  |    |
| Serial Clock High Time                                                  | $t_{SCKH}$              | 80          | --  | --  | ns  |    |
| Serial Clock Low Time                                                   | $t_{SCKL}$              | 80          | --  | --  | ns  |    |
| Enable Lead Time (falling edge of CS to rising edge of SCLK)            | $t_{lead}$              | 200         | --  | --  | ns  |    |
| Enable Lag Time (falling edge of SCLK to rising edge of CS)             | $t_{lag}$               | 200         | --- | --  | ns  |    |
| Data Setup Time (required time SI to falling of SCLK)                   | $t_{su}$                | 20          | --  | --  | ns  |    |
| Data Hold Time (falling edge of SCLK to SI)                             | $t_{H}$                 | 20          | --  | --  | ns  |    |
| Disable Time <sup>2</sup>                                               | $t_{DIS}$               | --          | --  | 150 | ns  |    |
| Transfer Delay Time <sup>1</sup><br>(CS high time between two accesses) | $t_{dt}$                | 300         | --  | --  | ns  |    |
| Data Valid Time                                                         | $C_L = 50\text{ pF}^2$  | $t_{valid}$ | --  | --  | 120 | ns |
|                                                                         | $C_L = 100\text{ pF}^2$ |             | --  | --  | 150 |    |

### 6. Diagnostic Functions

|                                           |              |               |               |               |   |
|-------------------------------------------|--------------|---------------|---------------|---------------|---|
| Open Load Detection Voltage (Channel OFF) | $V_{DS(OL)}$ | 0.5*<br>$V_S$ | 0.6*<br>$V_S$ | 0.7*<br>$V_S$ | V |
|-------------------------------------------|--------------|---------------|---------------|---------------|---|

<sup>1</sup> This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time  $t_{d(fault)max} = 200\mu s$ .

<sup>2</sup> This parameter is not subject to production test

|                                                       |                |                                  |               |               |            |
|-------------------------------------------------------|----------------|----------------------------------|---------------|---------------|------------|
| Output Pull Down Current (Channel OFF)                | $I_{PD(OL)}$   | 25                               | 50            | 100           | $\mu A$    |
| Fault Filtering Time                                  | $t_{d(fault)}$ | 50                               | 100           | 200           | $\mu s$    |
| Overload switch off delay time (only current limit 2) | $T_{d(off)}$   |                                  |               |               | $\mu s$    |
| Slew rate 1                                           |                | 10                               |               | 50            |            |
| Slew rate 2                                           |                | 10                               |               | 150           |            |
| Short to Ground Detection Voltage                     | $V_{DS(SHG)}$  | 0.3*<br>$V_S$                    | 0.4*<br>$V_S$ | 0.5*<br>$V_S$ | V          |
| Output Pull Up Current (Channel OFF)                  | $I_{PU(SHG)}$  | -50                              | -100          | -150          | $\mu A$    |
| Under Current Detection Threshold (Channel ON)        | $I_{D(OL)}$    | 100                              | 170           | 300           | mA         |
| Current Limit1; Overload Threshold Current1           | $I_{D(lim1)}$  | 5                                | 6.5           | 8             | A          |
| Current Limit2; Overload Threshold Current2           | $I_{D(lim2)}$  |                                  |               |               | A          |
|                                                       |                | $V_S \geq 5V$                    | 9             | 10,5          | 12         |
|                                                       |                | $V_S < 5V, T_J \leq 125^\circ C$ | 9             |               | 12         |
|                                                       |                | $V_S < 5V, T_J > 125^\circ C^2$  | 8             |               | 12         |
| IC Overtemperature Warning <sup>2</sup>               | $T_w$          | 155                              | --            | 185           | $^\circ C$ |
| Hysteresis <sup>2</sup>                               | $T_{(w) hys}$  | --                               | 10            | --            | K          |
| Channel Overtemperature Shutdown <sup>2</sup>         | $T_{th(sd)}$   | 170                              | --            | 200           | $^\circ C$ |
| Hysteresis <sup>2</sup>                               | $T_{(sd) hys}$ | --                               | 10            | --            | K          |

## 7. Analog Current Sense Output (IS1 / IS2)

|                                                                                                                 |             |     |                           |     |           |
|-----------------------------------------------------------------------------------------------------------------|-------------|-----|---------------------------|-----|-----------|
| Current Sense Precision (single channel) <sup>1</sup> $I_{FB} / I_{OUT}$<br>$I_D = 200mA - 1A; U_{CO1} \geq 2V$ | $P_{IS}$    | 0.8 | 1.0                       | 1.2 | mA<br>/ A |
| Current Sense Precision (single channel) <sup>1</sup> $I_{FB} / I_{OUT}$<br>$I_D = 1A - 5A; U_{CO1} \geq 2V$    | $P_{IS}$    | 0.9 | 1.0                       | 1.1 | mA<br>/ A |
| Current Sense Temperature Deviation <sup>2</sup><br>$V_S = 5V; I_D = 200mA \text{ to } 5A; U_{CO1} \geq 2V$     | $IS_{temp}$ | -10 | $P_{IS(25^\circ C, I_D)}$ | +10 | %         |
| Current Sense Settle time <sup>2</sup><br>$U_{CO1} \geq 2V, R_{sense} = 2,5k\Omega (I_{D max} = 1A)$            | $t_{IS}$    |     |                           | 4   | $\mu s$   |
| Current Sense Settle time <sup>2</sup><br>$U_{CO1} \geq 2V, R_{sense} = 500\Omega (I_{D max} = 5A)$             | $t_{IS}$    |     |                           | 2   | $\mu s$   |

<sup>1</sup> If the summed current is sensed the tolerances of the single channels are added.

<sup>2</sup> This parameter is not subject to production test

## Functional Description

The TLE 6214 L is a dual-low-side power switch which has two parallel inputs to control the 2 power DMOS switches, as well as by an 8-Bit SPI for control and diagnostic feedback. The power transistors are protected<sup>1)</sup> against short circuit, overload (current limitation), overtemperature and against overvoltage by an active zener clamp. The IC has a load current proportional current output for current control applications.

The diagnostic logic recognises a fault condition which can be read out via the SPI or the parallel status outputs (depending on the IC configuration).

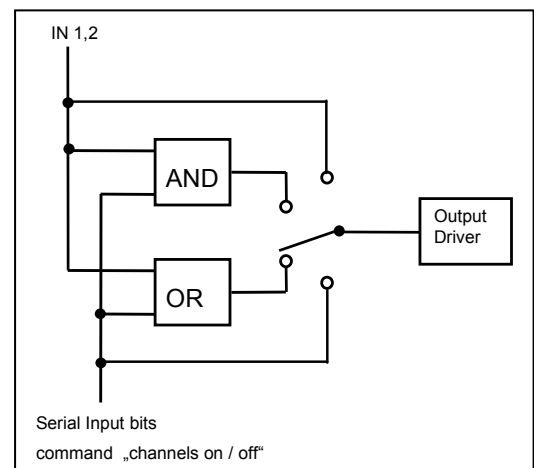
### Output Stage Control: Parallel Control or SPI Control

The Output stages can be controlled by parallel Inputs or by SPI command. The IC can be programmed (by SPI) to switch the outputs according to the parallel input signal, to the corresponding SPI command bit or to a combination of these two signals.

Both, parallel inputs and respective SPI databits are high active.

Truth table for Output control

| Input control signal Channel n |         | Output Channel n |                |          |           |
|--------------------------------|---------|------------------|----------------|----------|-----------|
| parallel Input                 | SPI Bit | parallel control | serial control | logic OR | logic AND |
| 0                              | 0       | off              | off            | off      | off       |
| 0                              | 1       | off              | on             | on       | off       |
| 1                              | 0       | on               | off            | on       | off       |
| 1                              | 1       | on               | on             | on       | on        |



Each output is independently controlled by an output latch. A logic high input 'data bit' turns the respective output channel ON, a logic low 'data bit' turns it OFF.

### Switching speed / Slew rate:

The switching speed / slew rate of both channels can be configured by SPI for slow or fast switching speed (1:5) for each channel individually.

### Overtemperature Behaviour:

Each channel has an overtemperature sensor and is individually protected against overtemperature. As soon as overtemperature occurs the channel is immediately turned off (without fault filtering time) and the overtemperature information is reported by diagnosis. In this case there are two different behaviours of the affected channel that can be selected by SPI (for all channels generally).

**Autorestart:** as long as the input signal of the channel remains on (e.g. parallel input high) the channel turns automatically on again after cooling down.

**Latching:** After overtemperature shutdown the channel stays off until the overtemperature latch is reset by a new L→H transition of the input signal.

Note: The overtemperature sensors of the output channels are only active if the channel is turned on.

As soon as the IC temperature (Temperature of the whole IC) reaches a specified level an overtemperature warning will be indicated.

**Low Quiescent current mode (Sleep mode) :** By SPI Command the device can be set to Sleep mode. In this mode all outputs are turned off, the diagnosis and biasing is disabled, the diagnosis and

<sup>1)</sup> The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently.

the on/off register are reseted and the current consumption drastically reduced. A wake up is done by sending a wake up command by SPI. A specified time ( $t_{wake}$ ) after this command the IC is fully functional. The configuraton register (exception channel on/off register) values are not influenced by the sleep mode. After wake up the outputs are Off, except the outputs are controlled by parallel inputs.

**Overload Protection:** The IC can be programmed to react in different ways to overload.

**Current limit 1:** In this mode the IC active limits the current to the specified "Current Limit 1". If the current limitation is active for longer than the fault filtering time this fault is reported and stored in the Fault register.

**Current limit 2:** If this current limit is active for more than the specified "Overload switch off delay time" the affected channel is turned off and the fault is reported and stored in the fault register. To turn on the channel again this overload latch has to be reset before with an L → H transition of the input signal (parallel /SPI depending on the programmed operation).

The two operation modes can be changed during operation of the channel.

## Pin description:

**OUTPUT 1,2** – Drain pins of the two channels. Output pins and connected to the load.

**GND** – Ground pins.

**IN 1,2** – Parallel Input Pins of the two channels

**IS / Fault / ST1** –Configurable output pin. Depending on the configuration (done by SPI command) it has three basic functions:

- a) General Fault pin. This is a general fault pin (open drain) which shows a high to low transition as soon as an error is latched into the diagnosis register. When the diagnosis register is cleared this flag is also reset (high state). This fault indication can be used to generate a  $\mu C$  interrupt.
- b) Sense Function. In this configuration the analog output signal represents the value of the load current:
  - Sense Current proportional load current channel 1
  - Sense Current proportional load current channel 2
  - Sense Current proportional load current of both channels ( $I_{D1} + I_{D2}$ )
- c) Status Output for channel 1: The Status output shows the same level as the input signal of channel 1 as long as there is no error and the inverted input signal when any kind of error occurs at channel 1

**VS** – Logic Supply pin. Used to supply the integrated circuitry.

**CS** – Chip Select of the SPI (low active)

**SO / ST2** – Configurable output pin. Depending on the configuration (done by SPI command) it has two functions:

- a) Signal Output of the **S**erial **P**eripheral Interface
- b) Status Output for channel 2: The Status output shows the same level as the input signal of channel 2 as long as there is no error and the inverted input signal when any kind of error occurs at channel 2

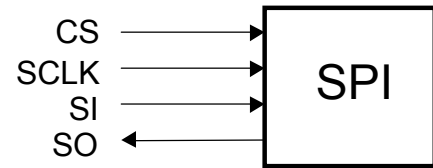
**SI** – Signal Input of the **S**erial **P**eripheral Interface. The pin has an internal pull down structure.

**SCKL** – Clock Input of the **S**erial **P**eripheral Interface. The pin has an internal pull down structure

## SPI

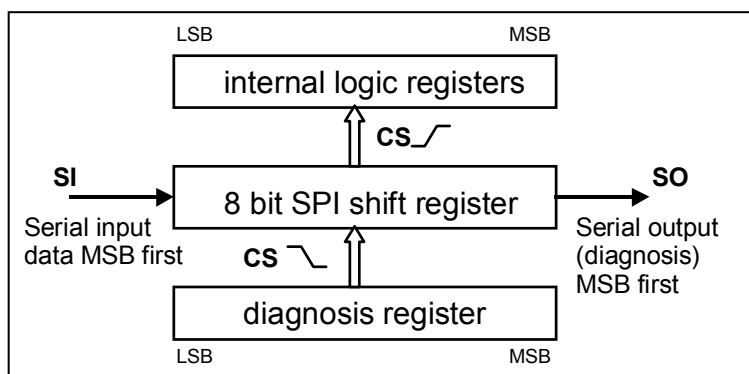
The SPI is a **S**erial **P**eripheral **I**nterface with 4 digital pins and an 8 bit shift register. The SPI is used to configure and program the device, turn on and off channels and to read detailed diagnostic information.

Note: The default setting of the TLE614L is to use the the SO/ST2 pin as status output pin for channel 2. To activate the SO function of the SPI the command "I/O Configure" (see. SPI commands: No.3) has to be used to reconfigure the IC. (e.g. 0111 xxxx)



### SPI Signal Description:

**CS** - Chip Select. The system microcontroller selects the TLE 6214 L by means of the CS pin. Whenever the pin is in a logic low state, data can be transferred from the  $\mu$ C and vice versa.



**CS = H** : Any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

**CS = H  $\rightarrow$  L** :

- diagnostic information is transferred from the diagnosis register into the SPI shift register. (in sleep mode no transfer of diagnostic information)
- serial input data can be clocked into the SPI shift register from then on
- SO changes from high impedance state

to logic high or low state corresponding to the SO bits

**CS = L** : SPI is working like a shift register. With each clock signal at the SCLK pin the state of the SI is read into the SPI shift-register (falling clock edge) and one diagnosis bit is written out of SO (rising edge).

**CS = L  $\rightarrow$  H**:

- transfer of SI bits from SPI shift register into the internal logic registers
- reset of diagnosis register if command was valid

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of CS.

**SCLK** - Serial Clock. The serial clock pin clocks the internal SPI shift register of the TLE 6214 L. The serial input (SI) accepts data into the input SPI shift register on the falling edge if while the serial output (SO) shifts diagnostic information out of the SPI shift register on the rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select CS makes any transition.

**SI** - Serial Input. Serial data bits are shifted in at this pin, the most significant bit (MSB) first. SI information is read in on the falling edge. Input data is latched in the SPI shift register and then transferred to the internal registers of the logic.

The input data consist of 8 bit, made up of x control bits and y data bits. The control word is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see SPI Commands).

**SO** - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit (MSB) first. SO is in a high impedance state until the CS pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge.

**SPI Commands:**

| No | Command                   | MSB          | 6 | 5 | 4                    | 3                       | 2              | 1             | LSB          |
|----|---------------------------|--------------|---|---|----------------------|-------------------------|----------------|---------------|--------------|
|    |                           | Command Bits |   |   | Data Bits            |                         |                |               |              |
| 1  | Diagnosis only            | 0            | 0 | 1 | X                    | X                       | X              | X             | X            |
| 2  | Output Configure          | 0            | 1 | 0 | I <sub>lim</sub> Ch2 | I <sub>lim</sub> Ch1    | Restart /Latch | Slewrate Ch2  | Slewrate Ch1 |
| 3  | I/O Configure             | 0            | 1 | 1 | Status / SPI         | Parallel / Serial Input |                | Fault / Sense |              |
| 4  | Reset Registers           | 1            | 0 | 0 | X                    | X                       | X              | X             | X            |
| 5  | Sleep Mode                | 1            | 0 | 1 | X                    | X                       | X              | X             | X            |
| 6  | Wake Up                   | 1            | 1 | 0 | X                    | X                       | X              | X             | X            |
| 7  | Channels on (1) / off (0) | 1            | 1 | 1 | Ch2                  | Ch1                     | X              | X             | X            |
| 8  | No command                | 0            | 0 | 0 | X                    | X                       | X              | X             | X            |

**Command description:** (default values are bold print)

**1. Diagnosis Only :** Reads out the diagnosis register. This command has no other influence on the device.

**2. Output Configure :** Configures the behaviour of the Power Outputs.

**I<sub>lim</sub> Ch1:** overload behaviour of channel 1

**0: Current limit 2 is activated** (default)

1: Current limit 1 is activated

**I<sub>lim</sub> Ch2:** overload behaviour of channel 2

**0: Current limit 2 is activated**(default)

1: Current limit 1 is activated

**Restart / Latch:** overtemperature behaviour of the IC

**0: Automatic autorestart of a channel after cooling down**(default)

1: Latching "off" of a channel at overtemperature

**Slew rate:** Switching slew rate of channel 1 and 2

**0: fast switching (slew rate 1)** (default)

1: slow switching (slew rate 2)

**3. I/O Configure :** Configures the behaviour of the I/O Ports.

**Status / SPI :** Output of diagnostic information of the IC

**0: Diagnosis output serial with one status output per channel (ST1, ST2)**

1: Diagnosis output with SPI (SO) and Fault Pin / Sense Pin

**Parallel / Serial Input :** Control of the output channels

bit3 bit2

**0 0 : Control of channel 1 and 2 with parallel input (IN1, IN2)** (default)

0 1 : Control of channel 1 and 2 with combination (OR) of serial and parallel input signal

1 0 : Control of channel 1 and 2 with combination (AND) of serial and parallel input signal

1 1 : Control of channel 1 and 2 only with SPI

**Sense / Fault :** Function of the Sense / Fault / ST1 output

bit1 bit0

**0 0 : Pin function is "general Fault pin"**(default)

0 1 : Pin function is current sense output channel 1 (I<sub>IS1</sub>)

1 0 : Pin function is current sense output channel 2 (I<sub>IS2</sub>)

1 1 : Pin function is current sense output channel 1 + 2 (I<sub>IS1</sub> + I<sub>IS2</sub>)

**4. Reset Registers** : Sets back all internal registers. Logic registers to default and Fault registers to no error.

Default settings after Reset:

- Parallel Input control
- Autorestart
- Status Outputs ST1 and ST2 active
- Current Limit 2
- Channel ON/OFF register "OFF"
- Slew rate fast

**5. Sleep mode** : Activates the low quiescent mode. In sleep mode only the command "wake up" is valid. Other commands will not lead to any reactions. Wake up is done by the Wake Up command or by undervoltage reset.

**6. Wake Up** : Deactivates the low quiescent mode. A specified time ( $t_{wake}$ ) after this command the IC is fully functional.

**7. Channels on / off** : Turns on / off the power outputs (if configured for serial control)

**Ch1** : Serial control bit of channel 1

**0: Output off**(default)

1: Output on

**Ch2** : Serial control bit of channel 2

**0: Output off**(default)

1: Output on

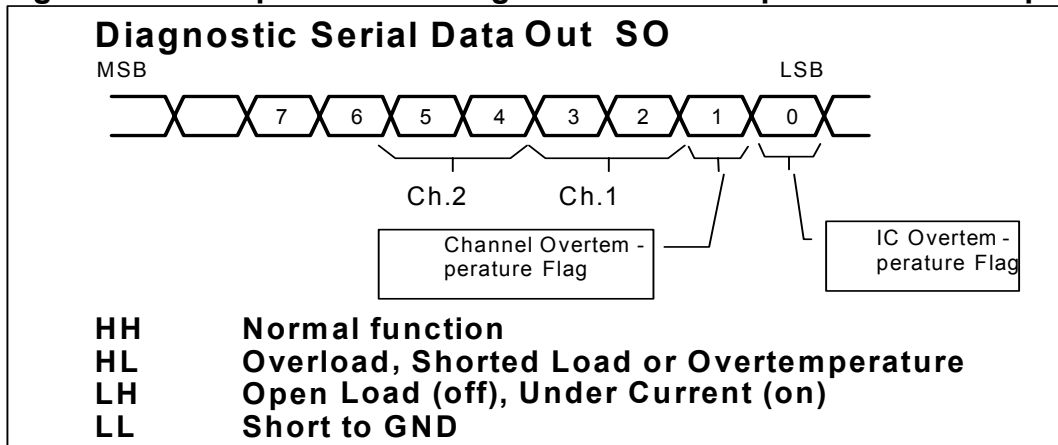
After activation of the low quiescent mode by the "sleep" command, the outputs are turned off and the serial control register is set to default values.

**8. No Command** : No valid command and will not lead to an reaction (register value change, switching channels, ...) of the IC. After Chip Select going L→H the diagnosis register will not be reset.

## SPI Diagnostics:

As soon as a fault occurs for longer than the fault filtering time (except Overtemperature; no filtering time), the fault information is latched into the diagnosis register (and the Fault pin will change from high to low state). A new error on the same channel will over-write the old error report. Serial data out pin (SO) is in a high impedance state when CS is high. If CS receives a LOW signal, all diagnosis bits can be shifted out serially. If the sent command was valid the rising edge of CS will reset all diagnosis registers and restart the fault filtering time. In case of an invalid command the device will ignore the data bits and the diagnosis register will not be reset at the rising CS edge.

**Fig. 1 : Two bits per channel diagnostic feedback plus two overtemperature flags**



For Full Diagnosis there are two diagnostic bits per channel configured as shown in Figure 1. Bit 6 and bit 7 of the diagnostic register are not used and always H.

**Normal function:** The bit combination **HH** indicates that there is no fault condition, i.e. normal function.

**Overload, Shorted Load or Overtemperature:** **HL** is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition. The second reason for this bit combination is overtemperature of the corresponding channel.

**Open load/ Under current:** **LH** is set when open load (in off state of the channel) or under current (in on state of the channel) is detected

**Short to GND :** **LL** is set when this condition is detected (in off state)

**Channel Overtemperature Flag:** In case of overtemperature in any output channel in on state the overtemperature Flag in the SPI diagnosis register is set. This Bit can be used to distinguish between Overload and Overtemperature (both HL combination).

**IC Overtemperature Warning Flag:** When the IC logic temperature exceeds typ.170° the IC Overtemperature Warning Flag will be set in the SPI diagnosis register.

## Parallel Status Output Diagnostics :

Parallel diagnostic outputs (open drain) change state according to the input signal of the corresponding channel. As soon as an error occurs at the corresponding channel ( Overload, Overtemperature and Under current is detected in on state and Open load, short to GND also in off state) the Status output shows the inverted input signal. A fault is detected only if it lasts for longer than the fault filtering time. This fault information is not latched.

If a CS Low to High transition is received the fault filtering time for parallel status output diagnostic is restarted (If a valid command was in the SPI register).

## Diagnostic Table

In general the status follows the input signal in normal operating conditions.  
If any error is detected the status is inverted.

| Operating Condition                                                         | Control Input | Power Output      | Filter time            | Status Output | FAULT Output | SPI diagnostic feedback |        |                         |
|-----------------------------------------------------------------------------|---------------|-------------------|------------------------|---------------|--------------|-------------------------|--------|-------------------------|
|                                                                             |               |                   |                        |               |              | Channel Diagnostic bits |        | Channel overtemp . flag |
|                                                                             |               |                   |                        |               |              | MSB                     | LSB    |                         |
| Sleep Mode                                                                  | X             | off               |                        | L             | H            | -                       | -      | -                       |
| Normal function                                                             | L<br>H        | off<br>on         |                        | L<br>H        | H<br>H       | H<br>H                  | H<br>H | L<br>L                  |
| Short to ground <sup>1)</sup> "off"                                         | L<br>H        | off<br>on         | td(fault)<br>td(fault) | H<br>L        | L<br>L       | L<br>L                  | L<br>H | L<br>L                  |
| Open load <sup>1)</sup> "off"                                               | L             | off               | td(fault)              | H             | L            | L                       | H      | L                       |
| Under current <sup>1)</sup> "on"                                            | H             | on                | td(fault)              | L             | L            | L                       | H      | L                       |
| Overload or short to supply <sup>1)</sup><br>(Current limit 1 / Limitation) | H             | on                | td(fault)              | L             | L            | H                       | L      | L                       |
| Overload or short to supply <sup>2)</sup><br>(Current limit 2 / Shutoff)    | H             | off               | td(off)                | L             | L            | H                       | L      | L                       |
| Overtemperature<br>(Restart mode)                                           | H             | off <sup>3)</sup> | no                     | L             | L            | H                       | L      | H                       |
| Overtemperature<br>(Latch mode)                                             | H             | off <sup>4)</sup> | no                     | L             | L            | H                       | L      | H                       |

Note 1) Short to ground/open load/ under current /overload/short-to-supply - events shorter than min. time td(fault) will not be latched and not reported at the diagnosis pins.

Note 2) Overload/short-to-supply - events shorter than min. time td(off) will not be latched and not reported at the diagnosis pins.

Note 3) Off as long as overtemperature occurs, restart after cooling down.

Note 4) Shutdown latch reset by falling input edge

## Analog Current Sensing :

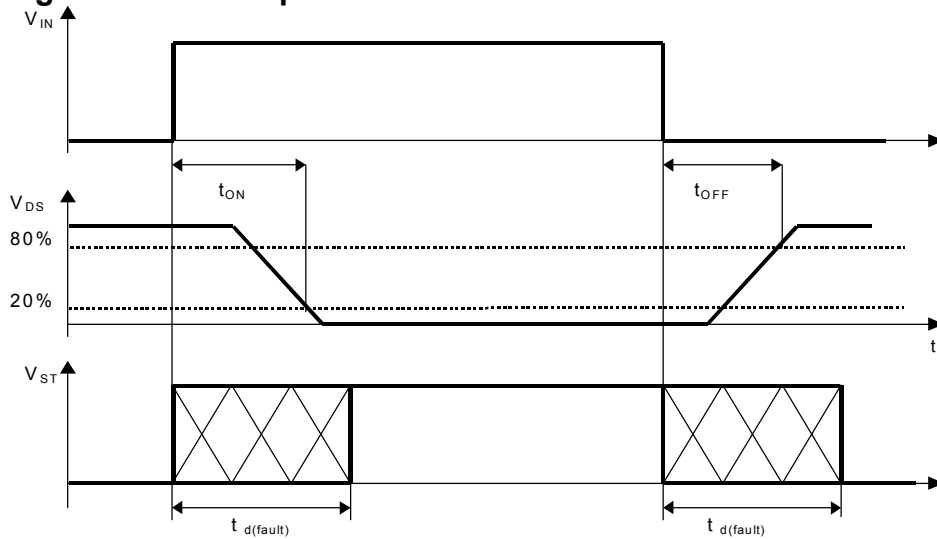
The TLE6214L provides an analog current sensing function for both output channels. By SPI configuration the multifunctional pin CO1 can sink a sense current proportional to the load current of one/ both of the two output channels<sup>1)</sup>. The specified current range and accuracy is described in the electrical characteristics "5.Analog Current Sense Output". To achieve the specified accuracy for current sensing the voltage at the CO1 pin must always be  $U_{CO1} \geq 2V$ .

The specified current sense temperature deviation is related to the typical 25°C

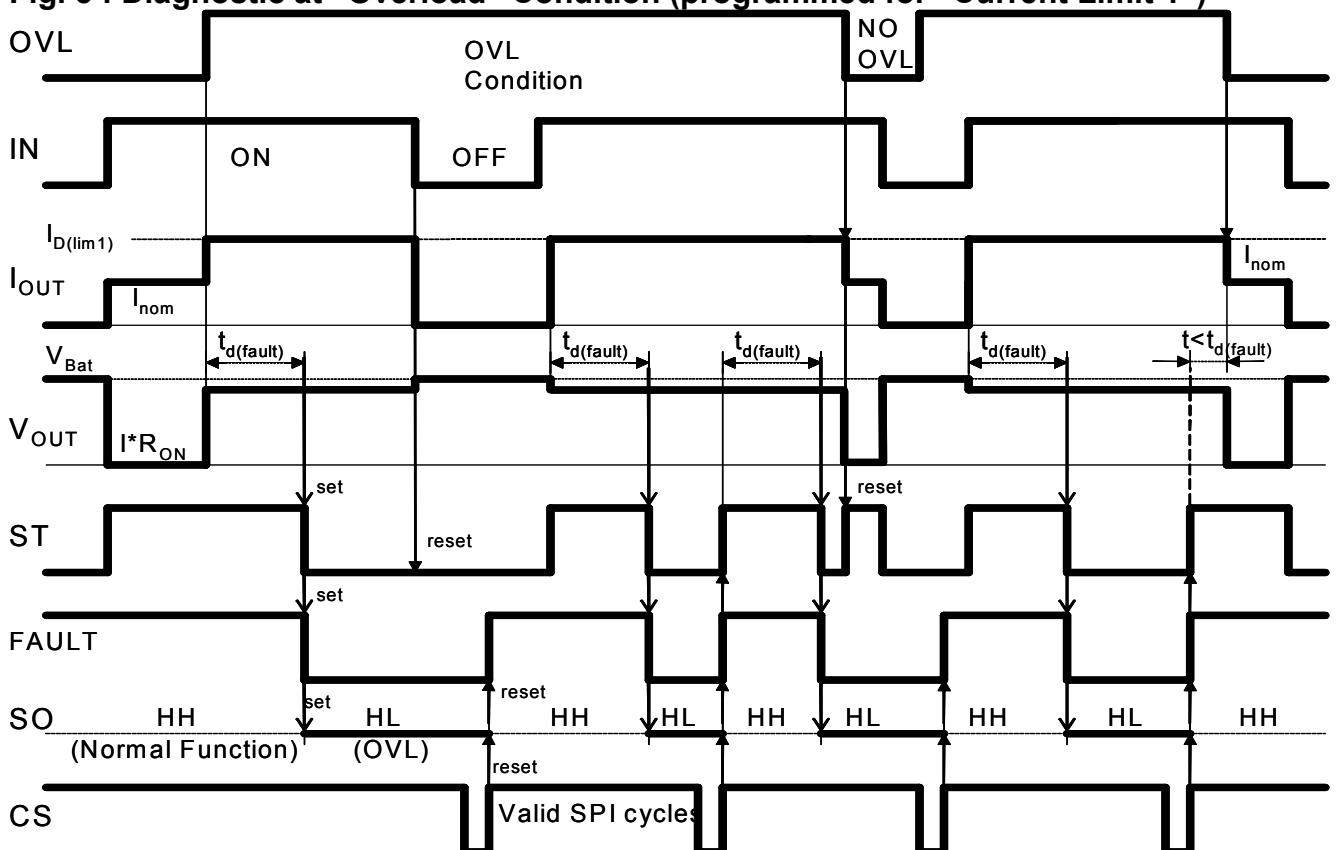
<sup>1)</sup> At a low load current (<<200mA) and IC configured for current sense function an offset current at the CO1 occurs (typ.  $I_S = 40\mu A$  @  $I_D = 0A$ ).

## Timing Figures

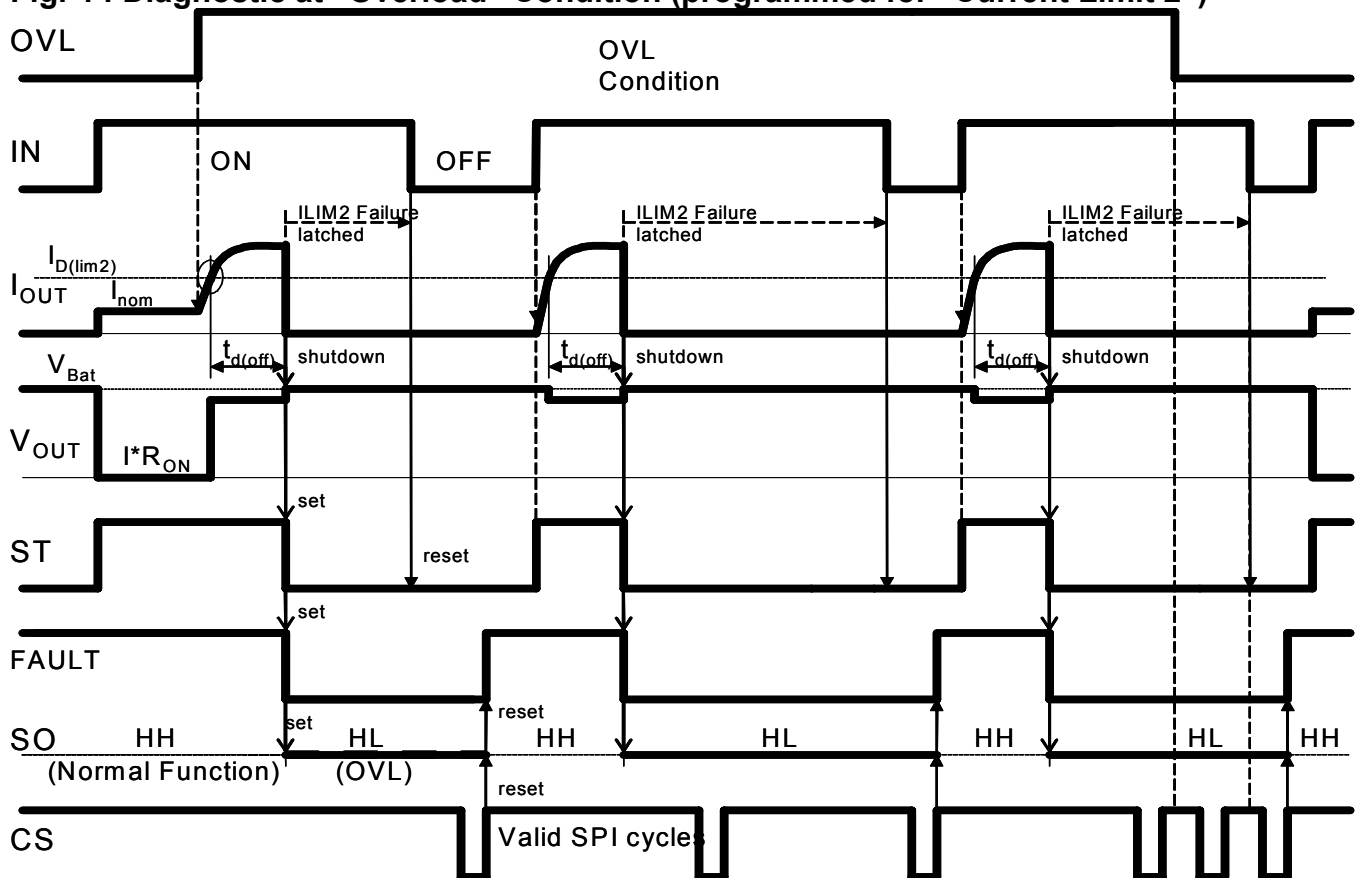
**Fig. 2 : Power Outputs and Status**



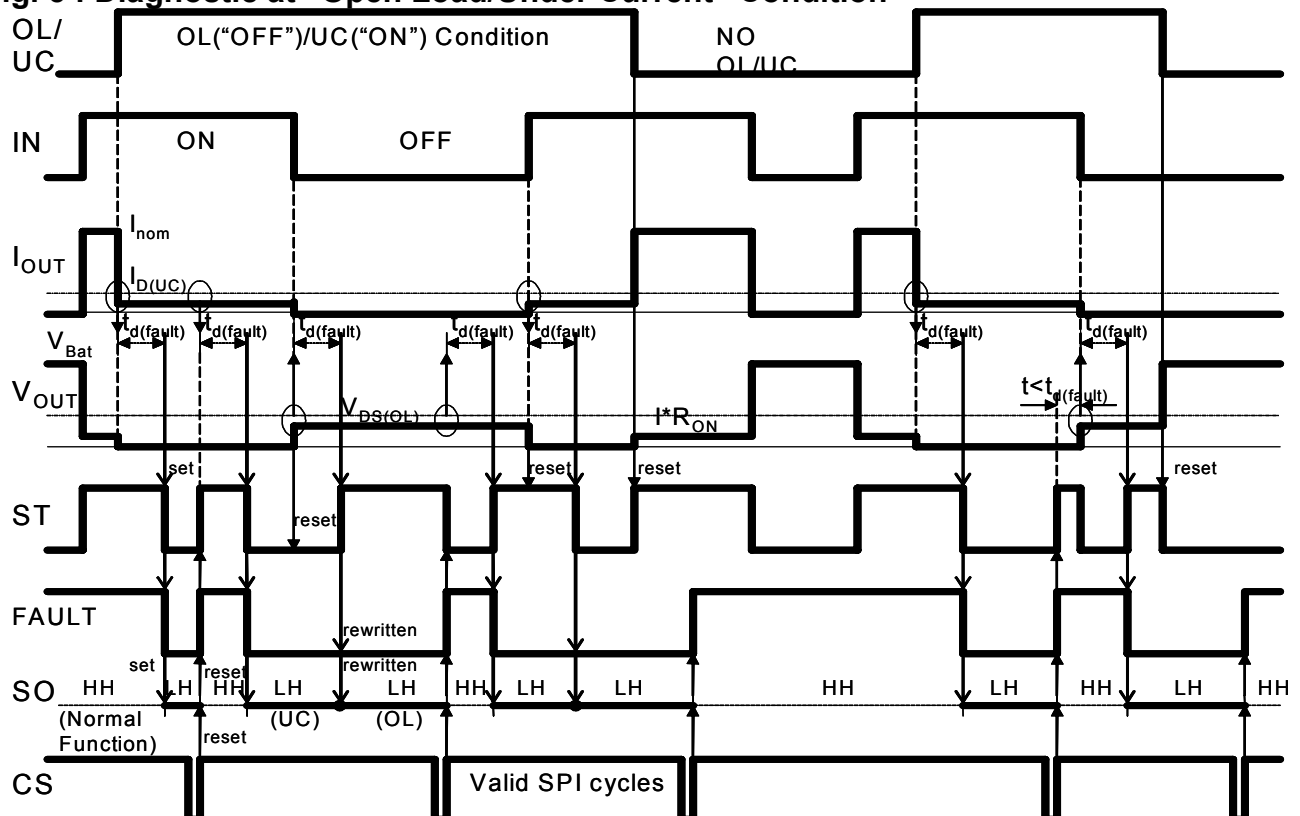
**Fig. 3 : Diagnostic at “Overload” Condition (programmed for “Current Limit 1”)**



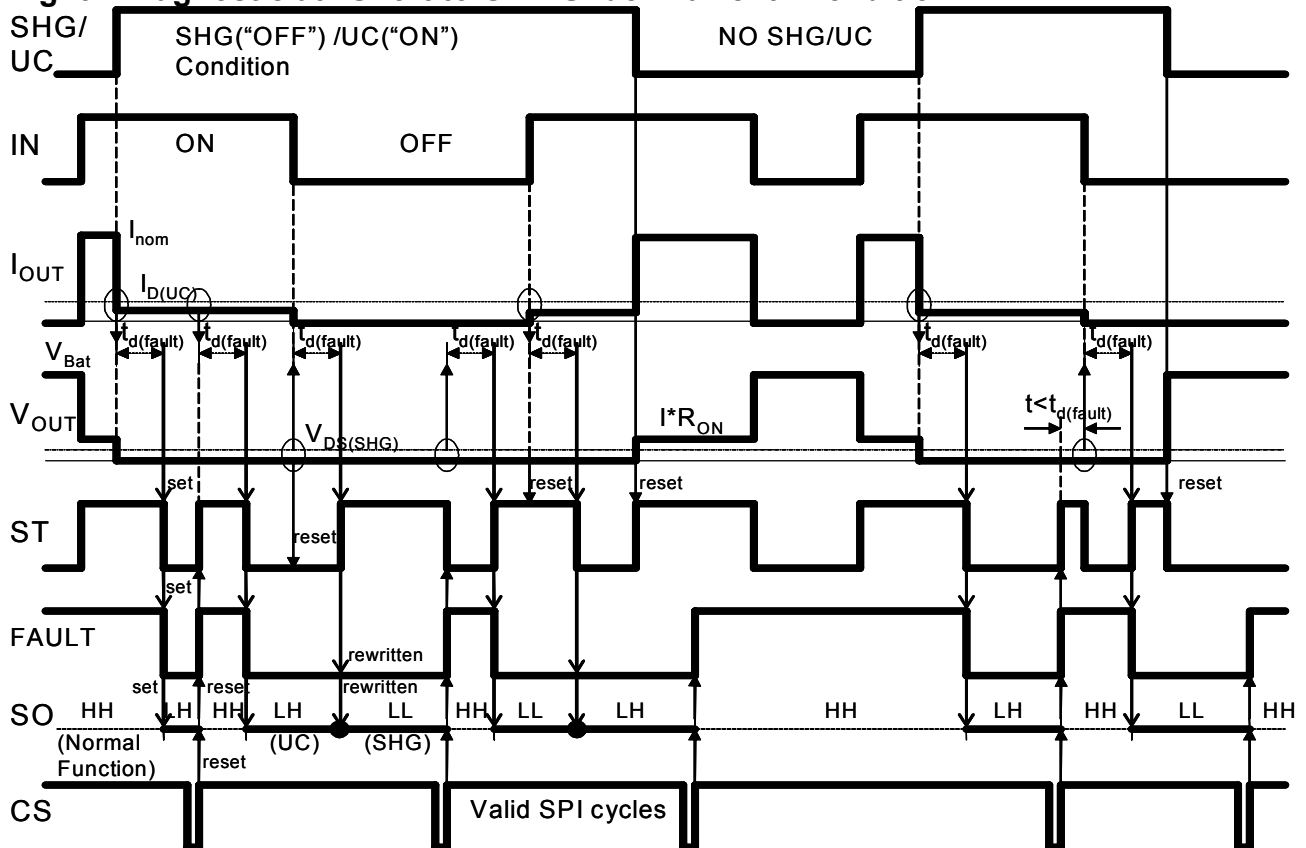
**Fig. 4 : Diagnostic at “Overload” Condition (programmed for “Current Limit 2”)**



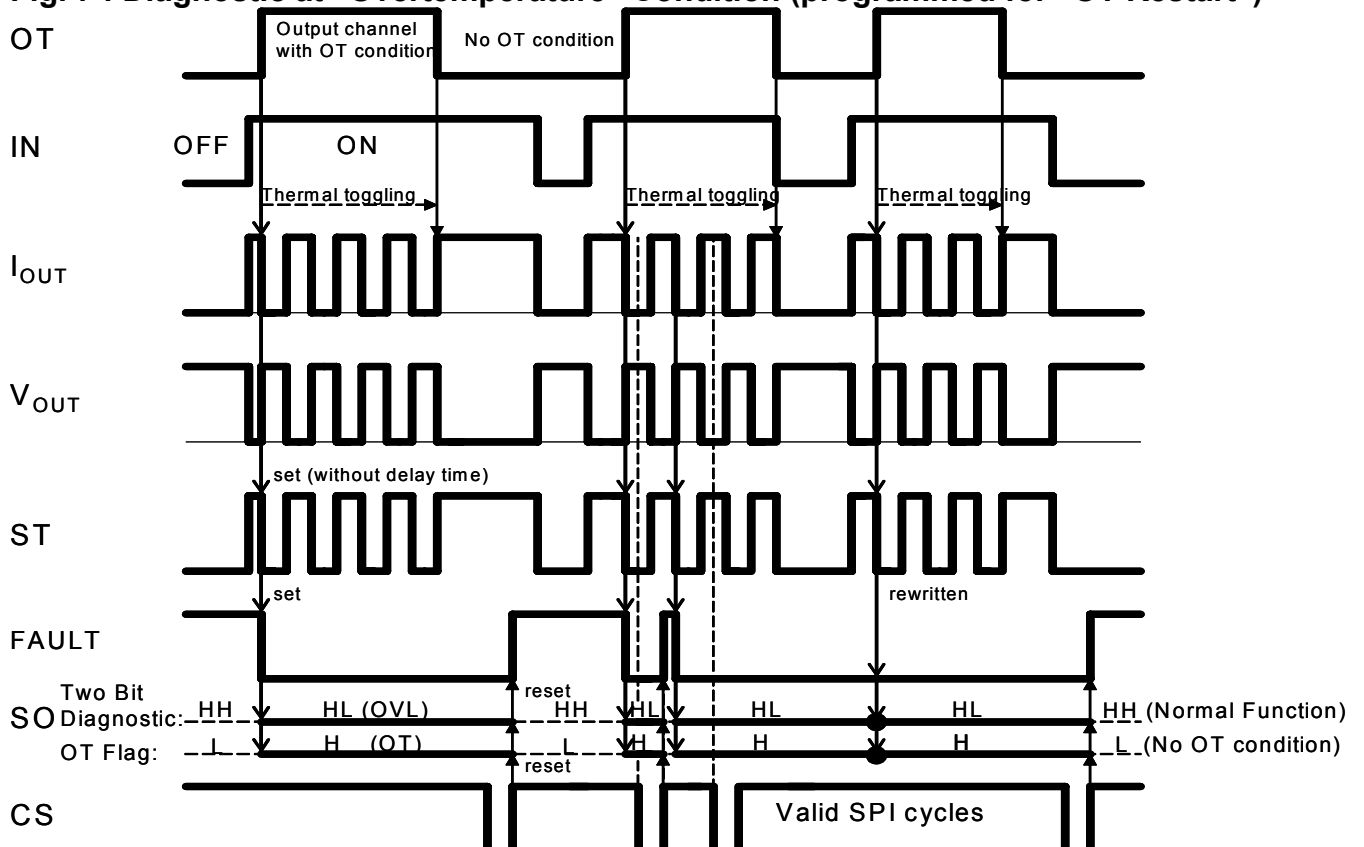
**Fig. 5 : Diagnostic at “Open Load/Under Current” Condition**



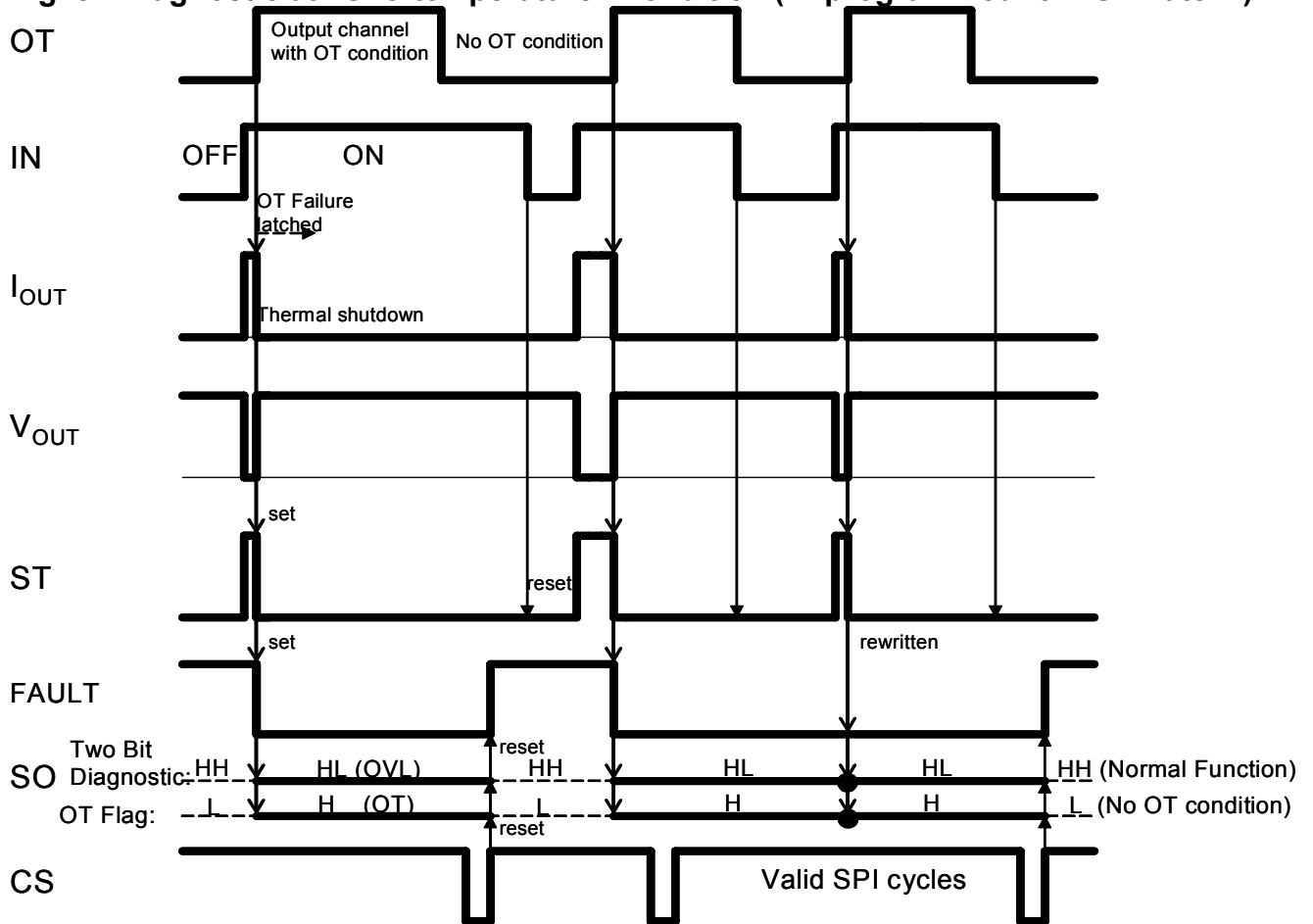
**Fig. 6 : Diagnostic at “Short to GND/Under Current” Condition**



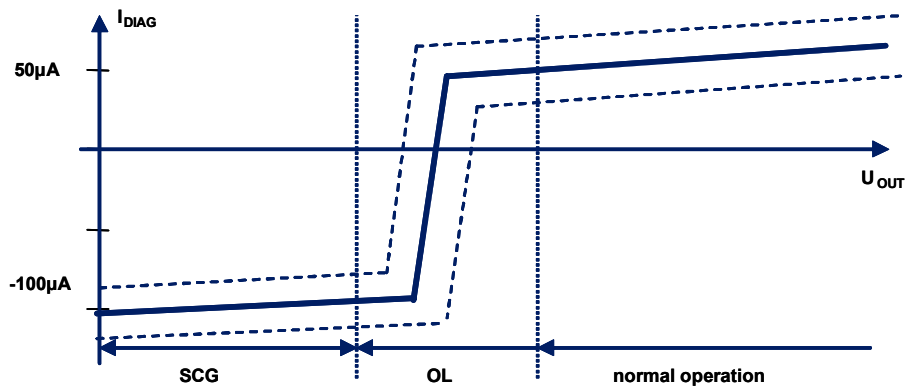
**Fig. 7 : Diagnostic at “Overtemperature” Condition (programmed for “OT Restart”)**



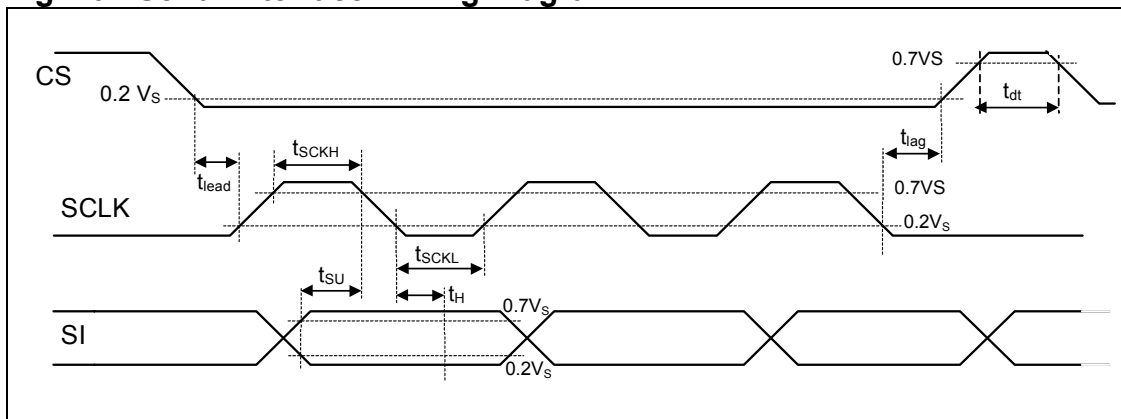
**Fig. 8 : Diagnostic at “Overtemperature” Condition (IC programmed for “OT Latch”)**



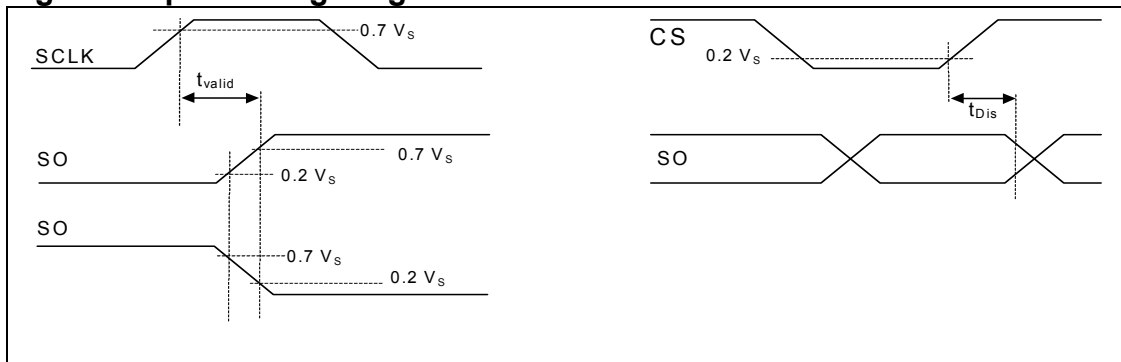
**Fig. 9 : Open load (off) and Short to GND Diagnostics**



**Fig. 10 : Serial Interface Timing Diagram**



**Fig. 11 : Input Timing Diagram**

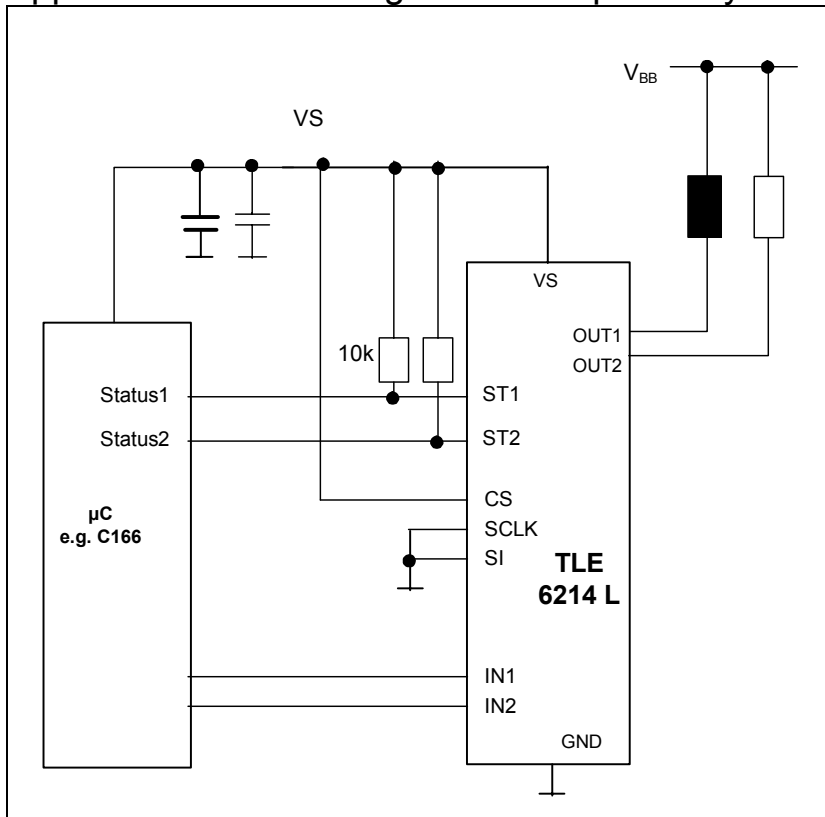


**SO Valid Time Waveforms**

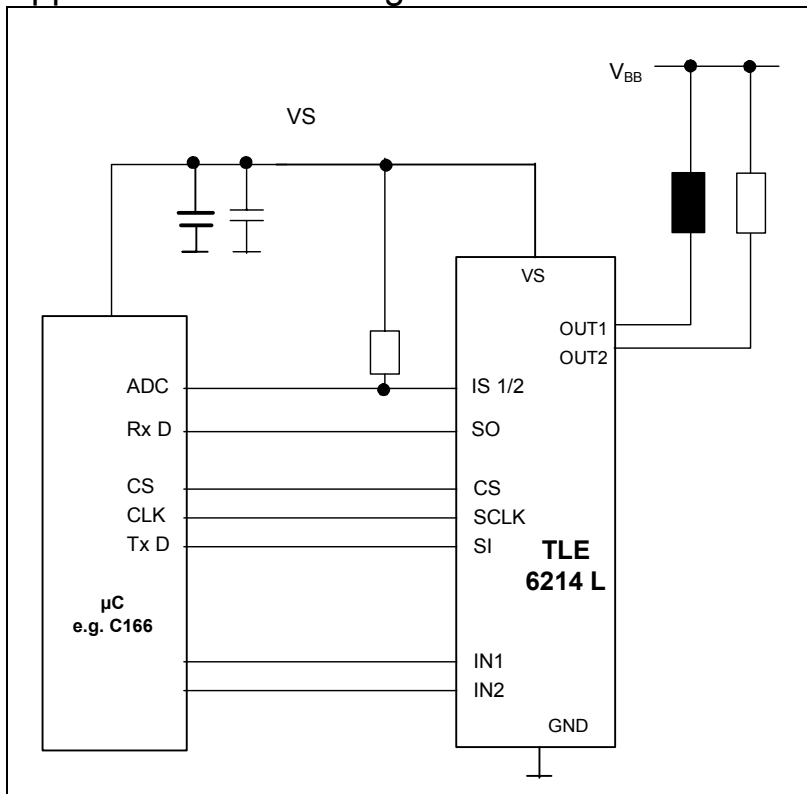
**Enable and Disable Time Waveforms**

## Application Circuits

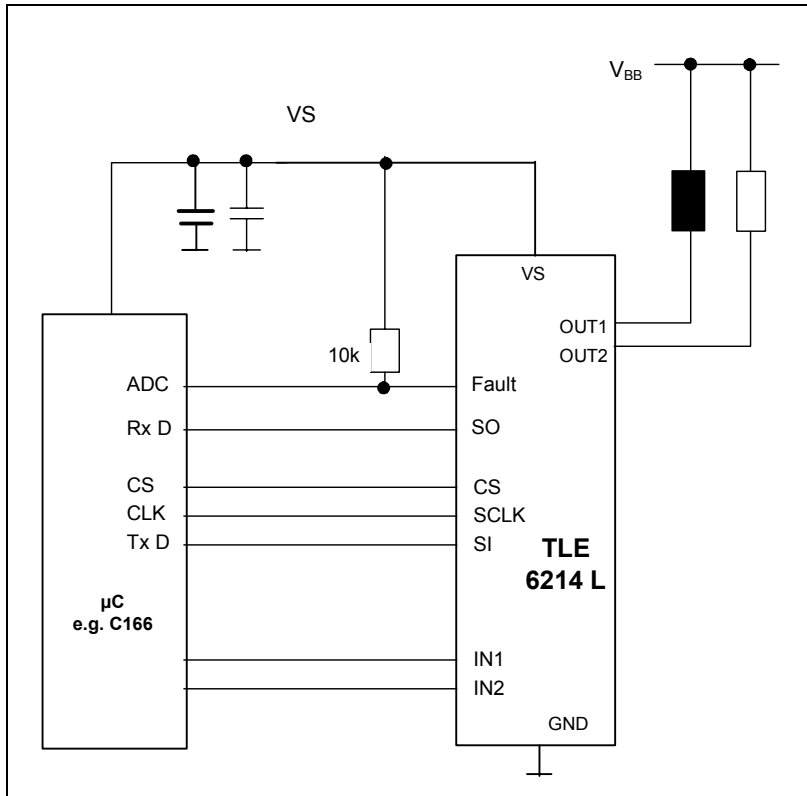
### Application Circuit using Status Outputs only



### Application Circuit using SPI and Current Sense Output

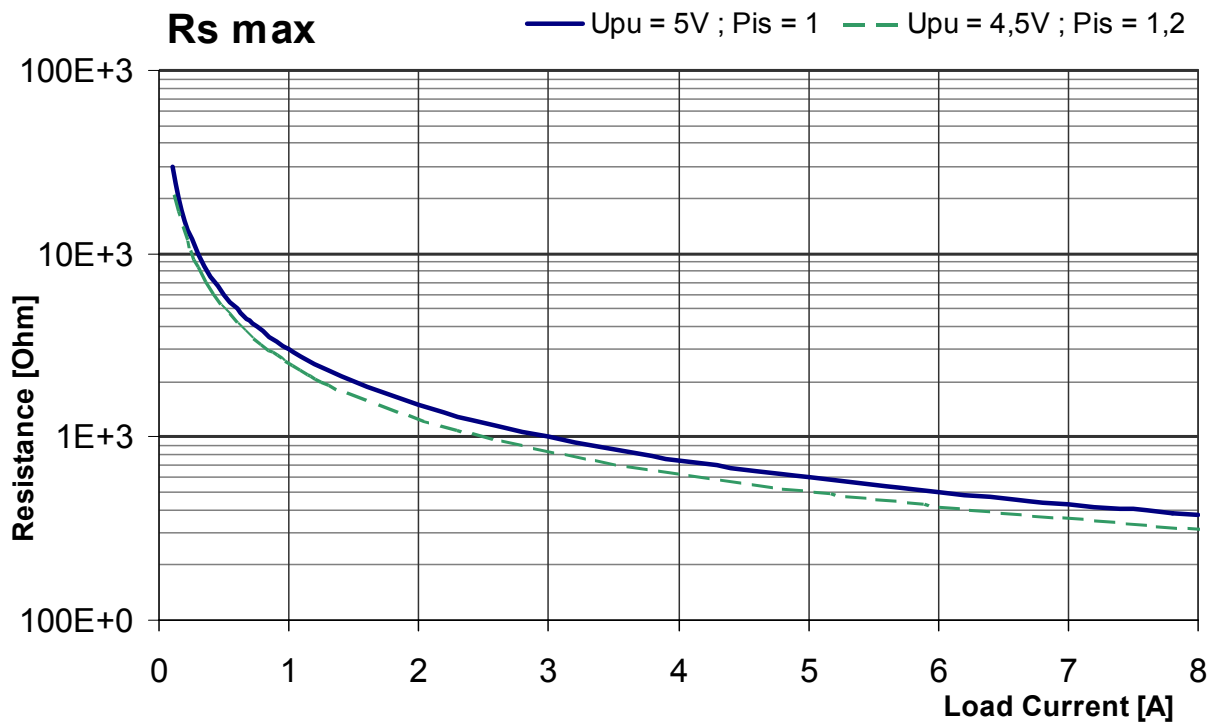


### Application Circuit using SPI and Fault Flag

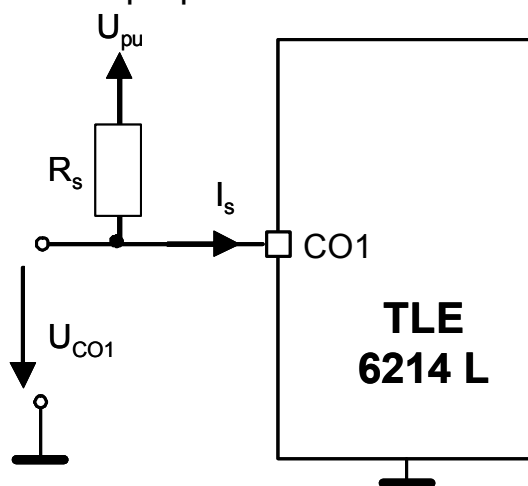


## Typical Characteristics

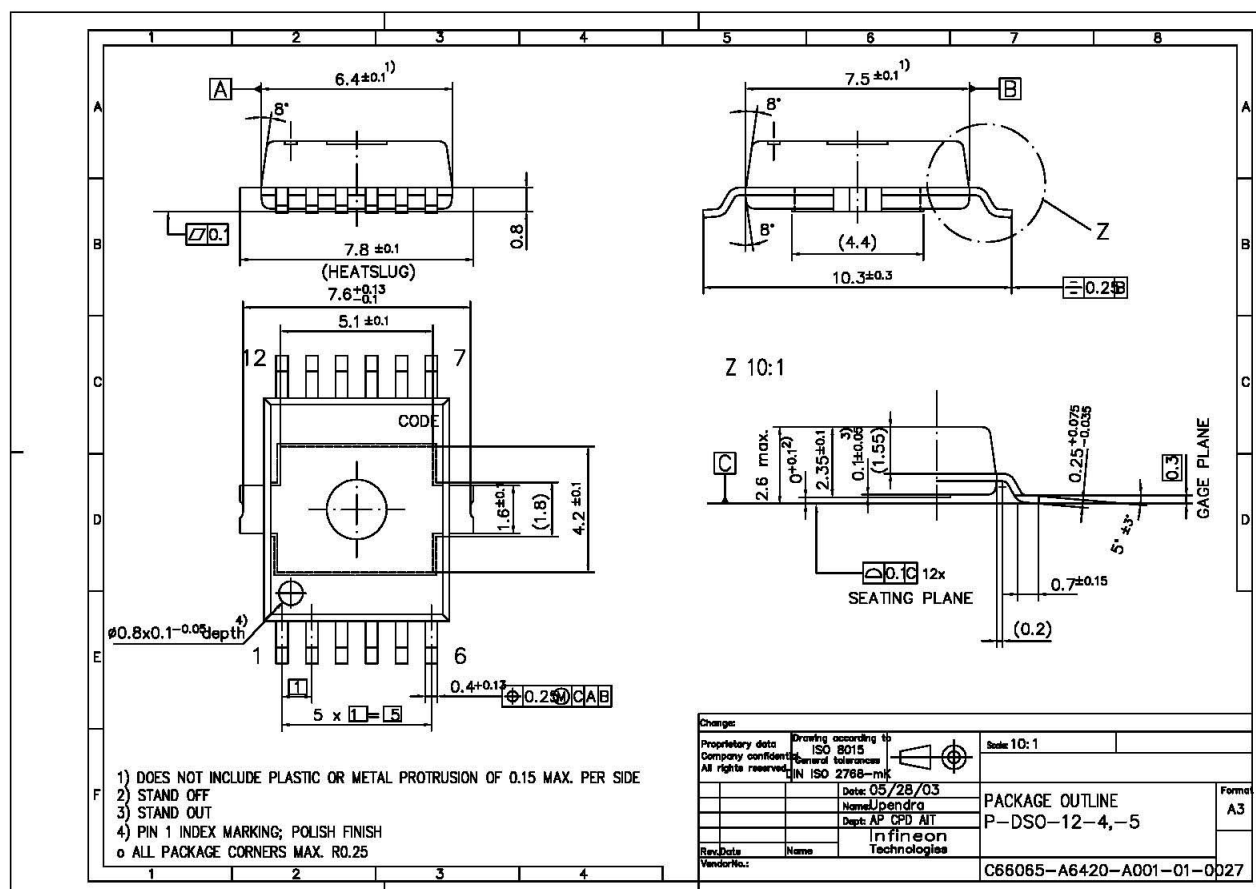
### Maximum Sense Resistor vs. Load Current



### Circuit proposal for current sensing



### Package and Ordering Code



o ~~A~~ CHANGED MARKER WITH REVISION

**(all dimensions in mm)**

**P - DSO - 12 - 4**

Ordering Code

|            |              |
|------------|--------------|
| TLE 6214 L | Q67007-A9698 |
|------------|--------------|

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