Dual Micropower Rail-To-Rail Input CMOS Comparator with Open Drain Output

Check for Samples: LMC6772

FEATURES

(Typical Unless Otherwise Noted)

- **Low Power Consumption (Max): I_S = 10 µA/comp**
- **Wide Range of Supply Voltages: 2.7V to 15V**
- **Rail-to-Rail Input Common Mode Voltage Range**
- **Open Drain Output**
- **Short Circuit Protection: 40 mA**
- **Propagation Delay (@V_S = 5V, 100 mV Overdrive): 5 µs**
- **LMC6772Q is AEC-Q Qualified**
- **LMC6772Q has −40°C to 125°C Temperature Range**

APPLICATIONS

- **Laptop Computers**
- **Mobile Phones**
- **Metering Systems**
- **Hand-Held Electronics**
- **RC Timers**
- **Alarm and Monitoring Circuits**
- **Window Comparators, Multivibrators**

DESCRIPTION

The LMC6772 is an ultra low power dual comparator with a maximum 10 µA/comparator power supply current. It is designed to operate over a wide range of supply voltages, with a minimum supply voltage of 2.7V.

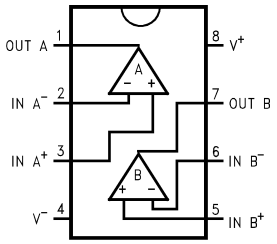
The common mode voltage range of the LMC6772 exceeds both the positive and negative supply rails, a significant advantage in single supply applications. The open drain output of the LMC6772 allows for wired-OR configurations. The open drain output also offers the advantage of allowing the output to be pulled to any voltage rail up to 15V, regardless of the supply voltage of the LMC6772.

The LMC6772 is targeted for systems where low power consumption is the critical parameter. Ensured operation at supply voltages of 2.7V and rail-to-rail performance makes this comparator ideal for battery-powered applications.

Refer to the LMC6762 datasheet for a push-pull output stage version of this device.

Connection Diagram

8-Pin PDIP/SOIC/VSSOP - Top View



See Package Number P0008E/D0008A/DGK0008A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

	Value	Unit
ESD Tolerance(2)	1.5	kV
Differential Input Voltage	(V+)+0.3V to (V−)−0.3	V
Voltage at Input/Output Pin	(V+)+0.3V to (V−)−0.3	V
Supply Voltage (V+–V−)	16	V
Current at Input Pin(3)	±5	mA
Current at Output Pin(4) (5)	±30	mA
Current at Power Supply Pin, LMC6772	40	mA
Lead Temperature (Soldering, 10 seconds)	260	°C
Storage Temperature Range	−65°C to 150	°C
Junction Temperature(6)	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the electrical characteristics.
(2) Human body model, 1.5 kΩ in series with 100 pF. The output pins of the two comparators (pin 1 and pin 7) have an ESD tolerance of 1.5 kV. All other pins have an ESD tolerance of 2 kV.
(3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) Do not short circuit output to V^+, when V+ is > 12V or reliability will be adversely affected.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings(1)

	Value	Unit
Supply Voltage	$2.7 \le V_S \le 15$	V
Junction Temperature Range		
LMC6772AI, LMC6772BI	$-40°C \le T_J \le 85$	°C
LMC6772Q	$-40°C \le T_J \le 125$	°C
Thermal Resistance (θ_{JA})		
8-Pin PDIP	100	°C/W
8-Pin SOIC	172	°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the electrical characteristics.

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2.7V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC6772AI Limit (2)	LMC6772BI Limit (2)	LMC6772Q Limit (2)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	10 **13**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		2.0				µV/°C
	Input Offset Voltage Average Drift	See (3)	3.3				µV/Month
I_B	Input Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio		75				dB
PSRR	Power Supply Rejection Ratio	±1.35V < V_S < ±7.5V	80				dB
A_V	Voltage Gain	(By Design)	100				dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	2.9 **2.7**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	−0.2 **0.2**	V max
V_{OL}	Output Voltage Low	I_{LOAD} = 2.5 mA	0.2	0.3 **0.4**	0.3 **0.4**	0.3 **0.45**	V max
I_S	Supply Current	For Both Comparators (Output Low)	12	20 **25**	20 **25**	20 **25**	µA max
$I_{Leakage}$	Output Leakage Current	V_{IN}(+) = 0.5V, V_{IN}(−) = 0V, V_O = 15V	0.1	500	500	500 **1000**	nA

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Input offset voltage Average Drift is calculated by dividing the accelerated operating life drift average by the equivalent operational time. The input offset voltage average drift represents the input offset voltage change at worst-case input conditions.

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5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5.0V and 15.0V, V^- = 0V, V_{CM} = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC6772AI Limit (2)	LMC6772BI Limit (2)	LMC6772Q Limit (2)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	10 **13**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift	V^+ = 5V	2.0				µV/°C
		V^+ = 15V	4.0				
	Input Offset Voltage Average Drift	V^+ = 5V (3)	3.3				µV/Month
		V^+ = 15V (3)	4.0				
I_B	Input Current	V = 5V	0.04				pA
I_{OS}	Input Offset Current	V^+ = 5V	0.02				pA
CMRR	Common Mode Rejection Ratio	V^+ = 5V	75				dB
		V^+ = 15V	82				
PSRR	Power Supply Rejection Ratio	±2.5V < V_S < ±5V	80				dB
A_V	Voltage Gain	(By Design)	100				dB
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5.0V CMRR > 55 dB	5.3	5.2 **5.0**	5.2 **5.0**	5.2 **5.0**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	−0.2 **0.0**	Vmax
		V^+ = 15.0V CMRR > 55 dB	15.3	15.2 **15.0**	15.2 **15.0**	15.2 **15.0**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OL}	Output Voltage Low	V^+ = 5V I_{LOAD} = 5 mA	0.2	0.4 **0.55**	0.4 **0.55**	0.4 **0.55**	V max
		V^+ = 15V I_{LOAD} = 5 mA	0.2	0.4 **0.55**	0.4 **0.55**	0.4 **0.55**	V max
I_S	Supply Current	For Both Comparators (Output Low)	12	20 **25**	20 **25**	20 **25**	µA max
I_{SC}	Short Circuit Current	V^+ = 15V, Sinking, V_O = 12V (4)	45				mA

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Input offset voltage Average Drift is calculated by dividing the accelerated operating life drift average by the equivalent operational time. The input offset voltage average drift represents the input offset voltage change at worst-case input conditions.
(4) Do not short circuit output to V^+, when V+ is > 12V or reliability will be adversely affected.

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AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ(1)	LMC6772AI Limit(2)	LMC6772BI Limit(2)	Units
t_{RISE}	Rise Time	f = 10 kHz, C_L = 50 pF, Overdrive = 10 mV(3)		0.3			µs
t_{FALL}	Fall Time	f = 10 kHz, C_L = 50 pF, Overdrive = 10 mV(3)		0.3			µs
t_{PHL}	Propagation Delay (High to Low)	f = 10 kHz, C_L = 50 pF(3)	10 mV	10			µs
			100 mV	4			µs
		V^+ = 2.7V, f = 10 kHz, C_L = 50 pF(3)	10 mV	10			µs
			100 mV	4			µs
t_{PLH}	Propagation Delay (Low to High)	f = 10 kHz, C_L = 50 pF(3)	10 mV	10			µs
			100 mV	4			µs
		V^+ = 2.7V, f = 10 kHz, C_L = 50 pF(3)	10 mV	8			µs
			100 mV	4			µs

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) C_L inlcudes the probe and jig capacitance. The rise time, fall time and propagation delays are measured with a 2V input step.

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Typical Performance Characteristics

V^+ = 5V, Single Supply, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage (Output High)

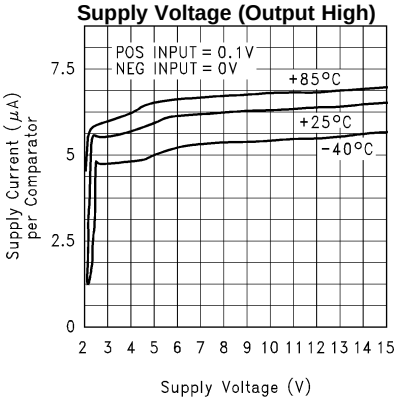

Figure 1.

Supply Current vs. Supply Voltage (Output Low)

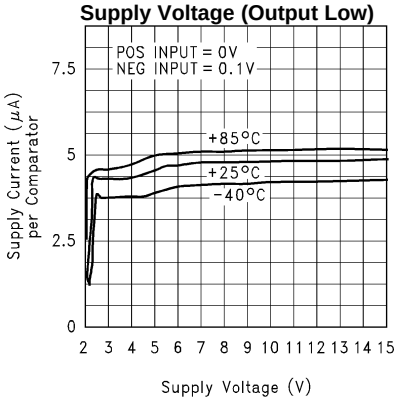

Figure 2.

Input Current vs. Common-Mode Voltage

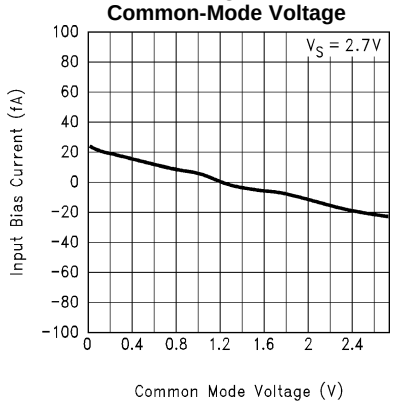

Figure 3.

Input Current vs. Common-Mode Voltage

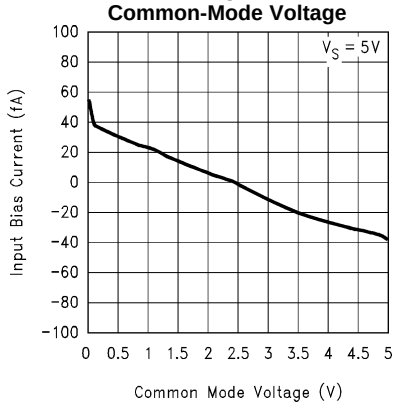

Figure 4.

Input Current vs. Common-Mode Voltage

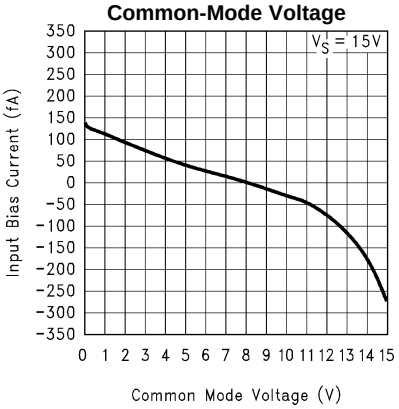

Figure 5.

Input Current vs. Temperature

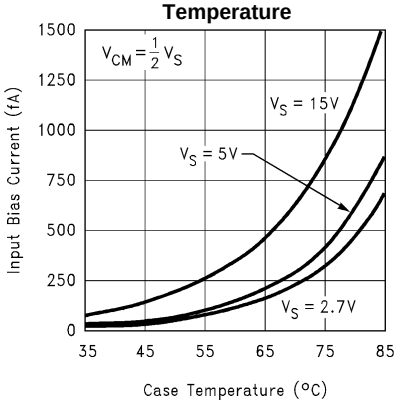

Figure 6.

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Typical Performance Characteristics (continued)

V^+ = 5V, Single Supply, T_A = 25°C unless otherwise specified

ΔV_{OS} vs ΔV_{CM}, V_S = 2.7V

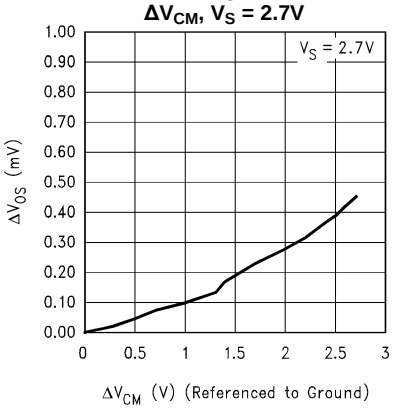

Figure 7.

ΔV_{OS} vs ΔV_{CM}, V_S = 5V

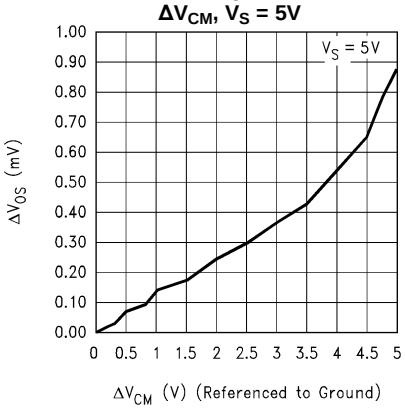

Figure 8.

ΔV_{OS} vs ΔV_{CM}, V_S = 15V

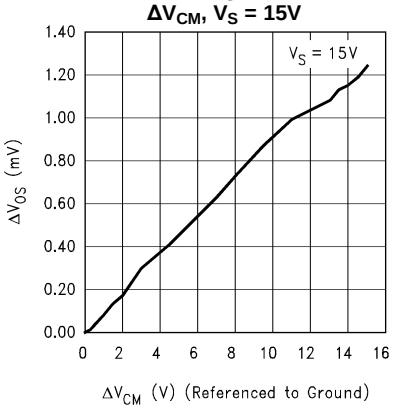

Figure 9.

Output Voltage vs. Output Current (Sinking)

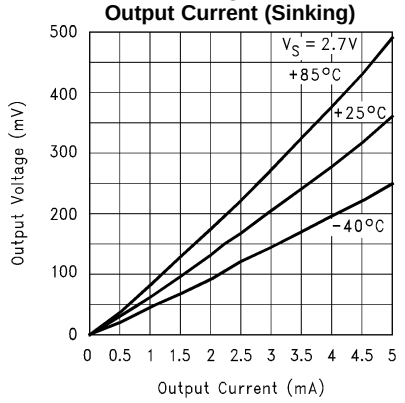

Figure 10.

Output Voltage vs. Output Current (Sinking)

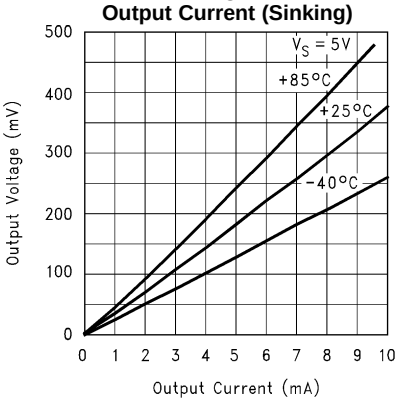

Figure 11.

Output Voltage vs. Output Current (Sinking)

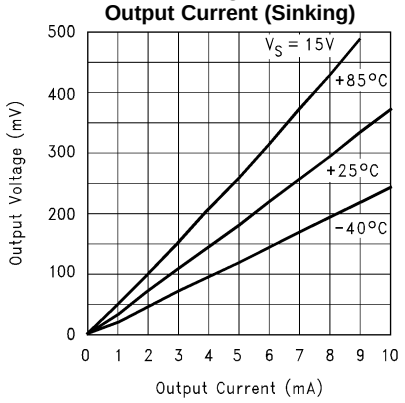

Figure 12.

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Typical Performance Characteristics (continued)

V^+ = 5V, Single Supply, T_A = 25°C unless otherwise specified

Output Short Circuit Current (Sinking) vs. Supply Voltage

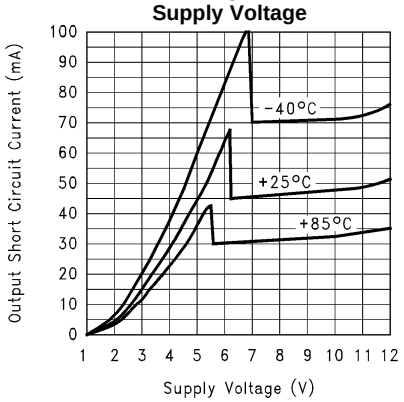

Figure 13.

Leakage Current vs. Output Voltage

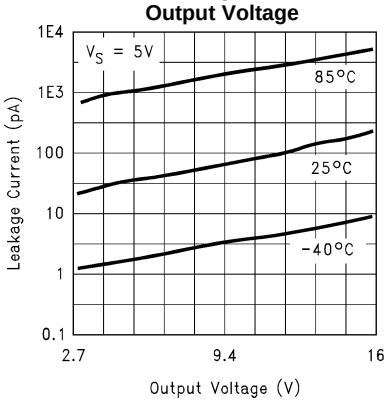

Figure 14.

Response Time for Overdrive (t_{PLH})

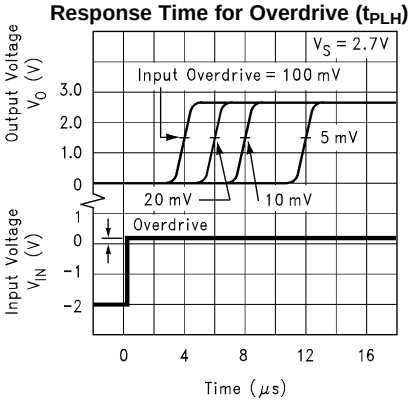

Figure 15.

Response Time for Overdrive (t_{PHL})

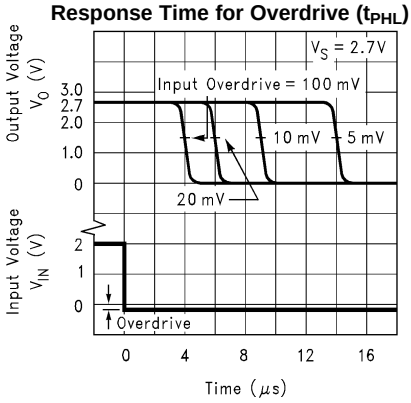

Figure 16.

Response Time for Overdrive (t_{PLH})

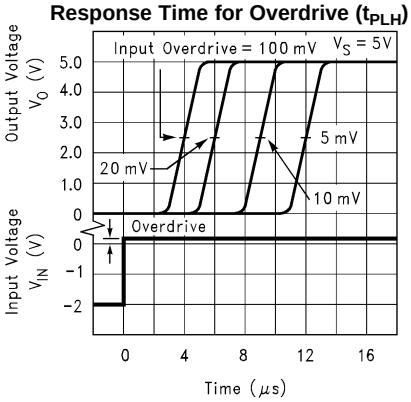

Figure 17.

Response Time for Overdrive (t_{PHL})

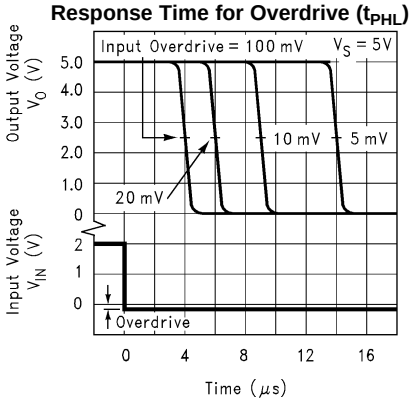

Figure 18.

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Typical Performance Characteristics (continued)

V^+ = 5V, Single Supply, T_A = 25°C unless otherwise specified

Response Time for Overdrive (t_{PLH})

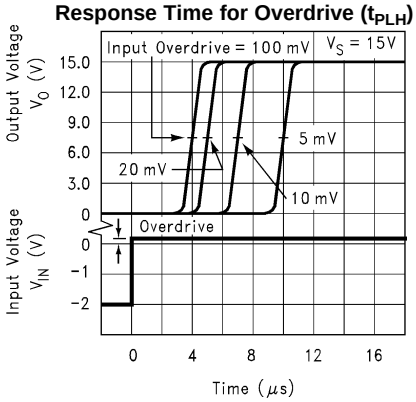

Figure 19.

Response Time for Overdrive (t_{PHL})

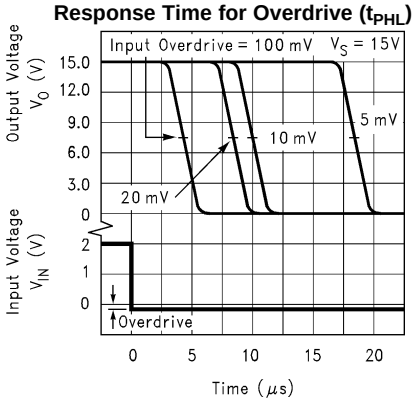

Figure 20.

Response Time vs. Capacitive Load

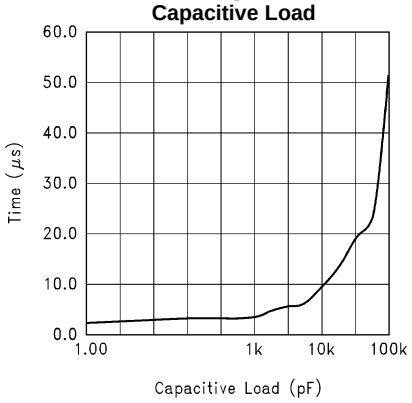

Figure 21.

LMC6772Q

Supply Current vs. Supply Voltage (Output High)

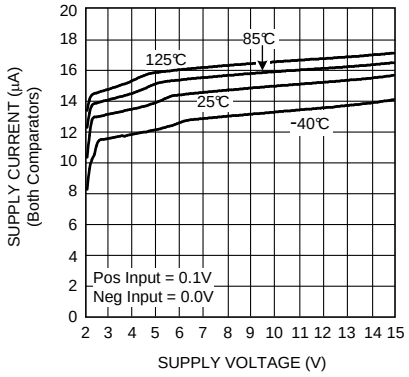

Figure 22.

Supply Current vs. Supply Voltage (Output Low)

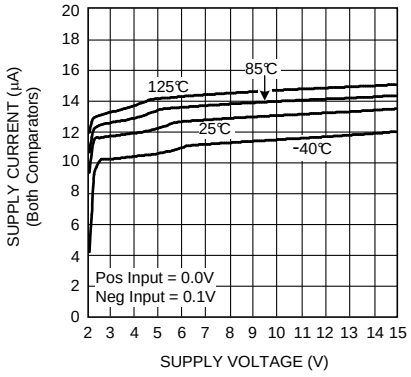

Figure 23.

Output Voltage vs. Output Current (Sinking)

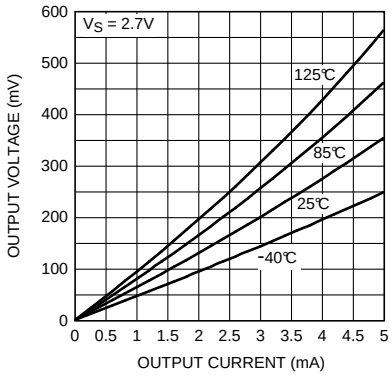

Figure 24.

Output Voltage vs. Output Current (Sinking)

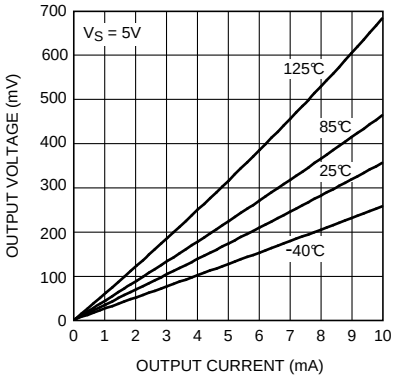

Figure 25.

Output Voltage vs. Output Current (Sinking)

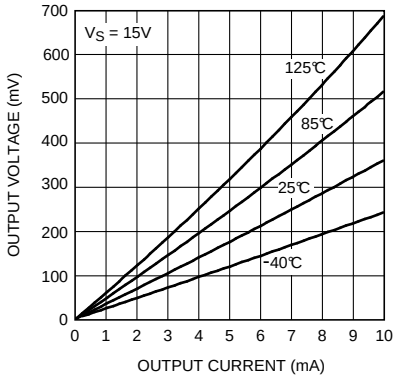

Figure 26.

Output Short Circuit Current vs. Supply

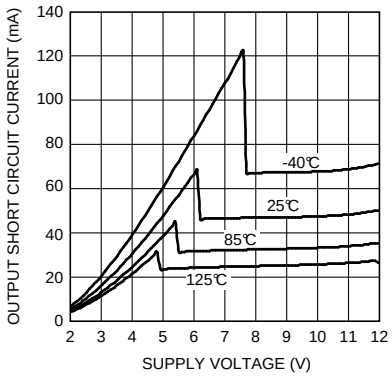

Figure 27.

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LMC6772Q (continued)

Output Leakage vs. Output Voltage

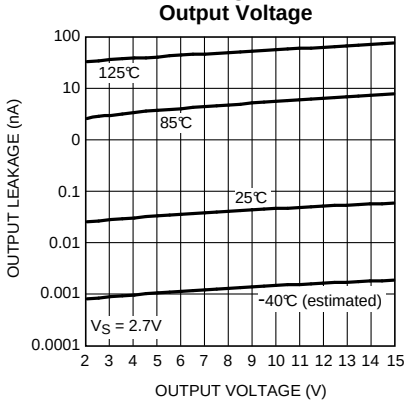

Figure 28.

APPLICATION INFORMATION

INPUT COMMON-MODE VOLTAGE RANGE

At supply voltages of 2.7V, 5V and 15V, the LMC6772 has an input common-mode voltage range which exceeds both supplies. As in the case of operational amplifiers, CMVR is defined by the V_{OS} shift of the comparator over the common-mode range of the device. A CMRR ($\Delta V_{OS}/\Delta V_{CM}$) of 75 dB (typical) implies a shift of < 1 mV over the entire common-mode range of the device. The absolute maximum input voltage at V^+ = 5V is 200 mV beyond either supply rail at room temperature.

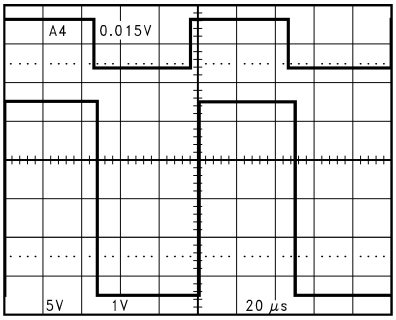

Figure 29. An Input Signal Exceeds the LMC6772 Power Supply Voltages with No Output Phase Inversion

A wide input voltage range means that the comparator can be used to sense signals close to ground and also to the power supplies. This is an extremely useful feature in power supply monitoring circuits.

An input common-mode voltage range that exceeds the supplies, 20 fA input currents (typical), and a high input impedance makes the LMC6772 ideal for sensor applications. The LMC6772 can directly interface to sensors without the use of amplifiers or bias circuits. In circuits with sensors which produce outputs in the tens to hundreds of millivolts, the LMC6772 can compare the sensor signal with an appropriately small reference voltage. This reference voltage can be close to ground or the positive supply rail.

LOW VOLTAGE OPERATION

Comparators are the common devices by which analog signals interface with digital circuits. The LMC6772 has been designed to operate at supply voltages of 2.7V, without sacrificing performance, to meet the demands of 3V digital systems.

At supply voltages of 2.7V, the common-mode voltage range extends 200 mV (ensured) below the negative supply. This feature, in addition to the comparator being able to sense signals near the positive rail, is extremely useful in low voltage applications.

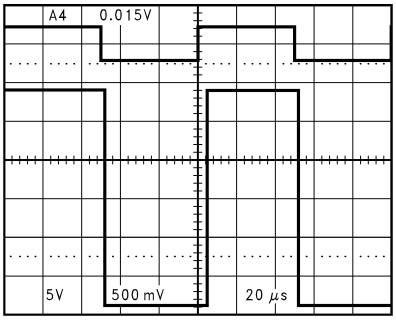

Figure 30. Even at Low-Supply Voltage of 2.7V, an Input Signal which Exceeds the Supply Voltages Produces No Phase Inversion at the Output

At V^+ = 2.7V, propagation delays are t_{PLH} = 4 µs and t_{PHL} = 4 µs with overdrives of 100 mV. Please refer to the performance curves for more extensive characterization.

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OUTPUT SHORT CIRCUIT CURRENT

The LMC6772 has short circuit protection of 40 mA. However, it is not designed to withstand continuous short circuits, transient voltage or current spikes, or shorts to any voltage beyond the supplies. A resistor is series with the output should reduce the effect of shorts. For outputs which send signals off PC boards additional protection devices, such as diodes to the supply rails, and varistors may be used.

HYSTERESIS

If the input signal is very noisy, the comparator output might trip several times as the input signal repeatedly passes through the threshold. This problem can be addressed by making use of hysteresis as shown below.

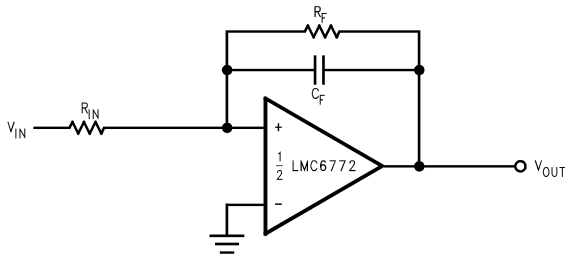

Figure 31. Canceling the Effect of Input Capacitance

The capacitor added across the feedback resistor increases the switching speed and provides more short term hysteresis. This can result in greater noise immunity for the circuit.

SPICE MACROMODEL

A Spice Macromodel is available for the LMC6772. The model includes a simulation of:

- Input common-mode voltage range
- Quiescent and dynamic supply current
- Input overdrive characteristics

and many more characteristics as listed on the macromodel disk.

A SPICE macromodel of this and many other op amps is available at no charge from the WEBENCH Design Center Team at www.ti.com

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TYPICAL APPLICATIONS

UNIVERSAL LOGIC LEVEL SHIFTER

The output of the LMC6772 is the uncommitted drain of the output NMOS transistor. Many drains can be tied together to provide an output OR'ing function. An output pullup resistor can be connected to any available power supply voltage within the permitted power supply range.

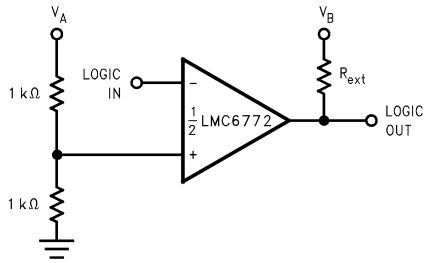

Figure 32. Universal Logic Level Shifter

The two 1 kΩ resistors bias the input to half of the power supply voltage. The pull-up resistor should go to the output logic supply. Due to its wide operating range, the LMC6772 is ideal for the logic level shifting applications.

ONE-SHOT MULTIVIBRATOR

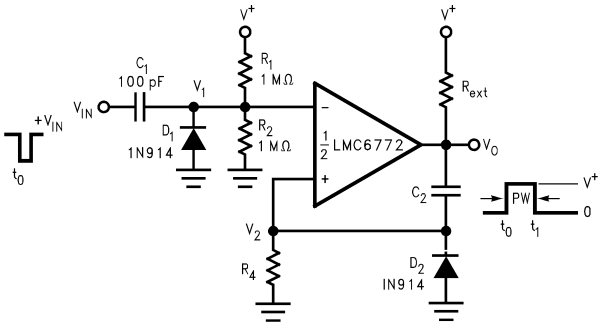

Figure 33. One-Shot Multivibrator

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The LMC6772 will change state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

BI-STABLE MULTIVIBRATOR

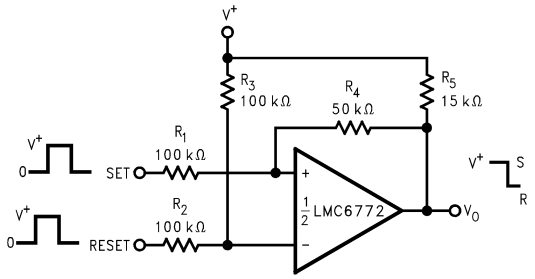

Figure 34. Bi-Stable Multivibrator

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A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

ZERO CROSSING DETECTOR

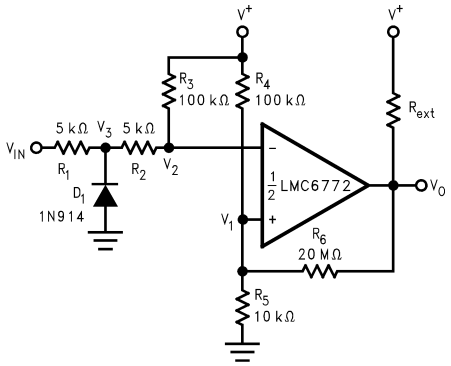

Figure 35. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator will switch when V_{IN} = 0. Diode D_1 insures that V_3 never drops below −0.7V. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

OSCILLATOR

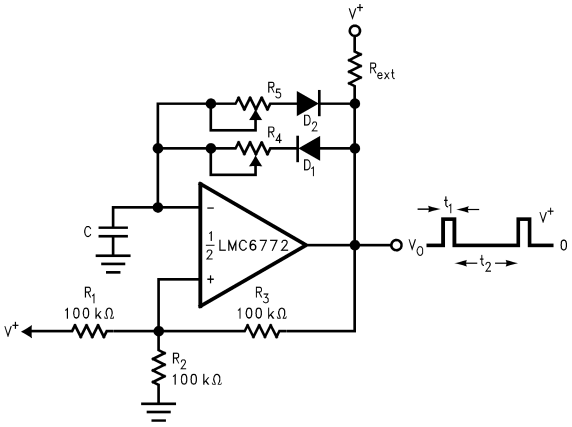

Figure 36. Square Wave Generator

Figure 36 shows the application of the LMC6772 in a square wave generator circuit. The total hysteresis of the loop is set by R_1, R_2 and R_3. R_4 and R_5 provide separate charge and discharge paths for the capacitor C. The charge path is set through R_4 and D_1. So, the pulse width t_1 is determined by the RC time constant of R_4 and C. Similarly, the discharge path for the capacitor is set by R_5 and D_2. Thus, the time t_2 between the pulses can be changed by varying R_5, and the pulse width can be altered by R_4. The frequency of the output can be changed by varying both R_4 and R_5.

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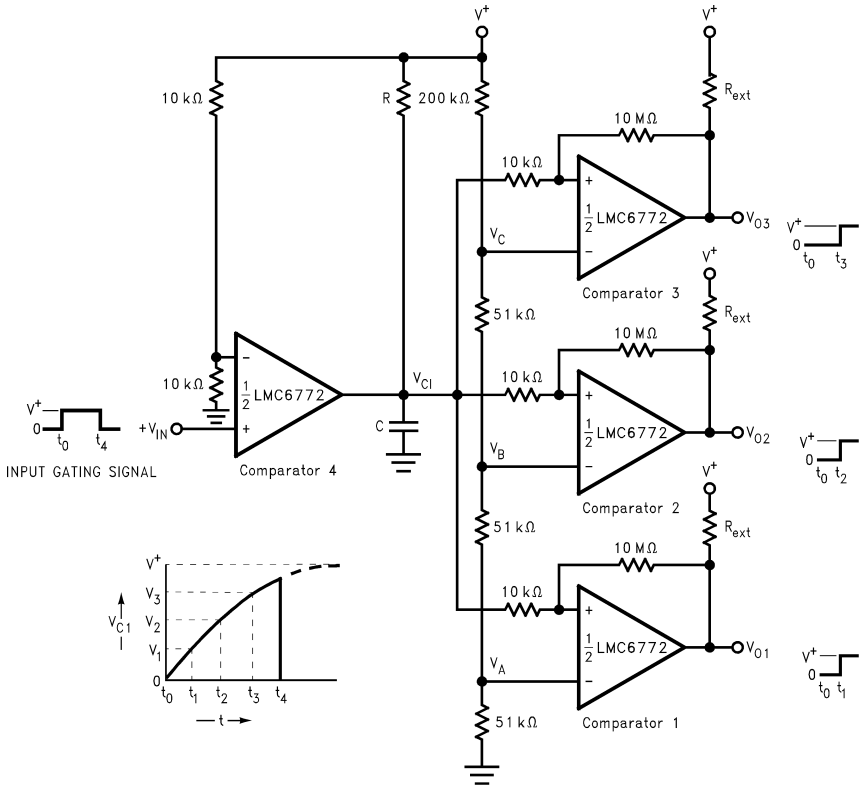

Figure 37. Time Delay Generator

The circuit shown above provides output signals at a prescribed time interval from a time reference and automatically resets the output when the input returns to ground. Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground. This implies that the outputs of comparators 1, 2, and 3 are also at ground. When an input signal is applied, the output of comparator 4 swings high and C charges exponentially through R. This is indicated above. The output voltages of comparators 1, 2, and 3 swtich to the high state when V_{C1} rises above the reference voltages V_A, V_B and V_C. A small amount of hysteresis has been provided to insure fast switching when the RC time constant is chosen to give long delay times.

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REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	16

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6772AIM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC67 72AIM	Samples
LMC6772AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC67 72AIM	Samples
LMC6772AIMM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	C21	Samples
LMC6772AIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C21	Samples
LMC6772AIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C21	Samples
LMC6772AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC67 72AIM	Samples
LMC6772BIM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC67 72BIM	Samples
LMC6772BIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC67 72BIM	Samples
LMC6772BIMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC67 72BIM	Samples
LMC6772BIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC67 72BIM	Samples
LMC6772QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AX5A	Samples
LMC6772QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AX5A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMC6772, LMC6772-Q1 :

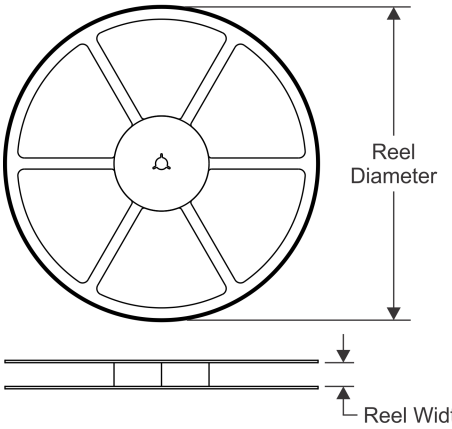
- Catalog: LMC6772
- Automotive: LMC6772-Q1

NOTE: Qualified Version Definitions:

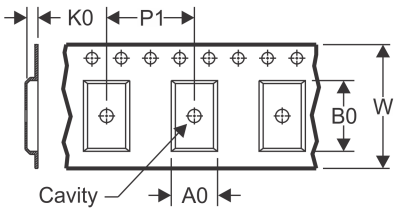
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

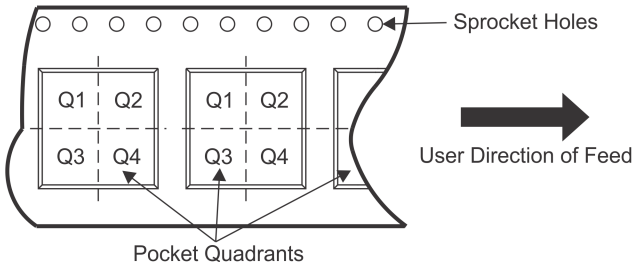


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

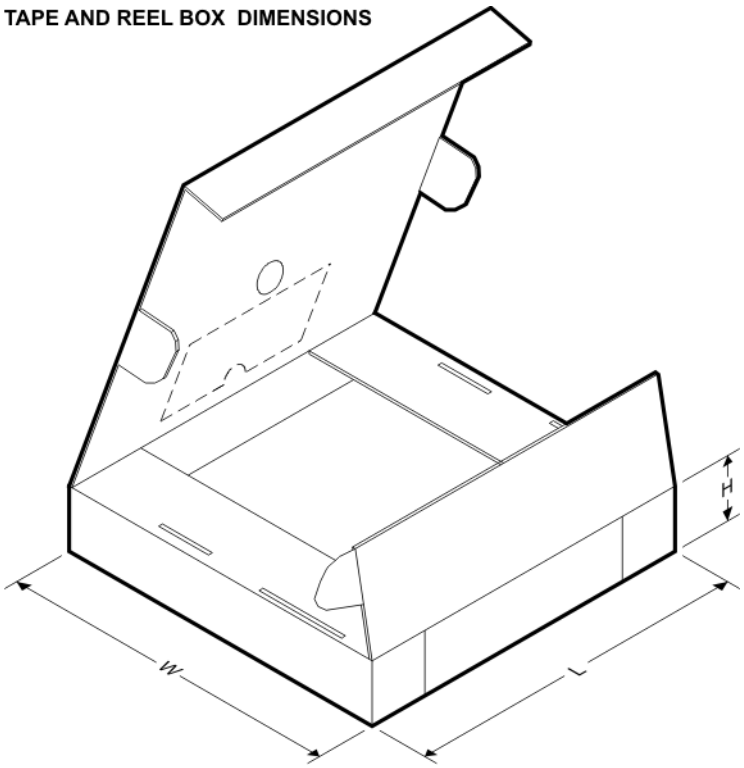
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

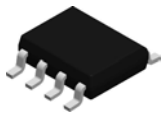
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6772AIMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6772AIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6772AIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6772AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6772BIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6772BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6772QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6772QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6772AIMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6772AIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6772AIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6772AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6772BIMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6772BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6772QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6772QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

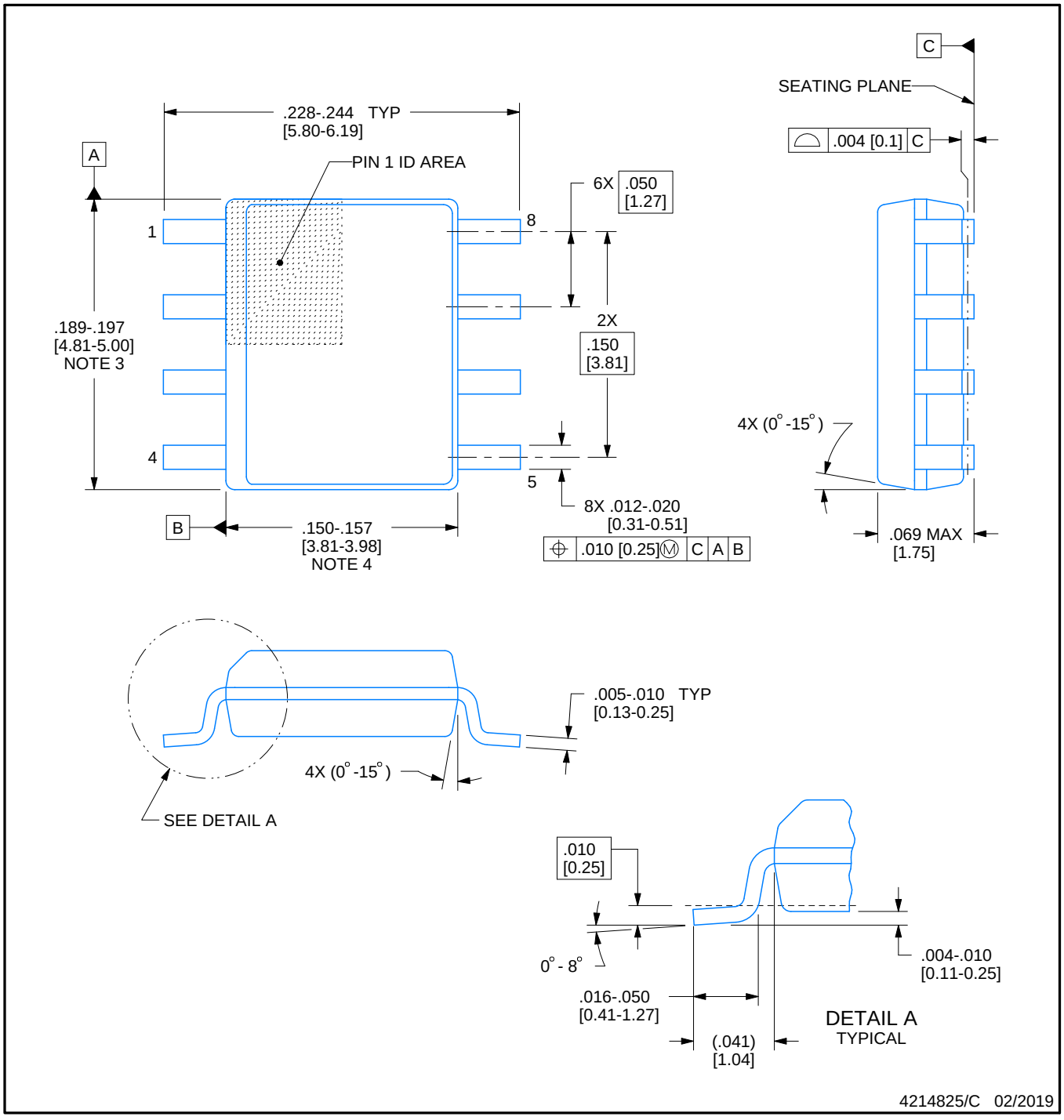


PACKAGE OUTLINE

D0008A

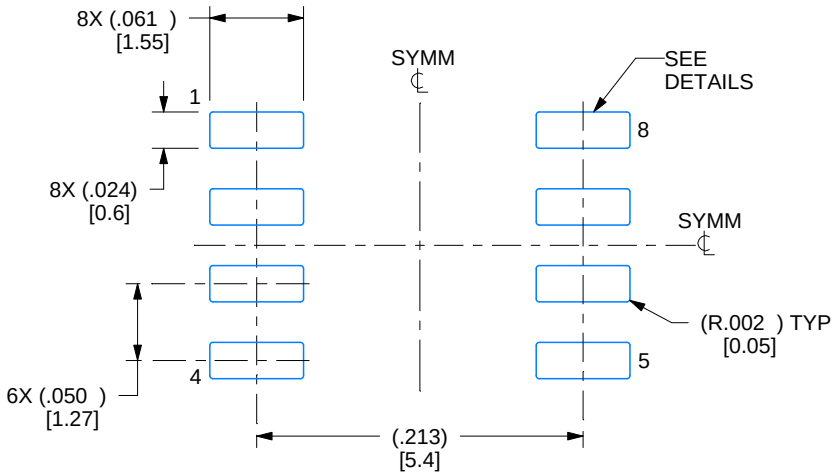
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

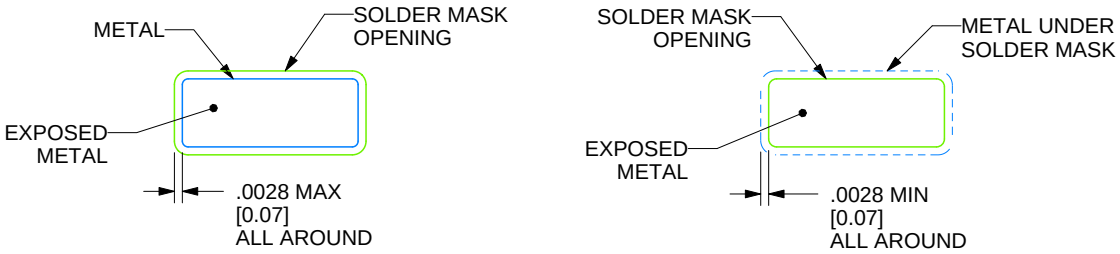


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

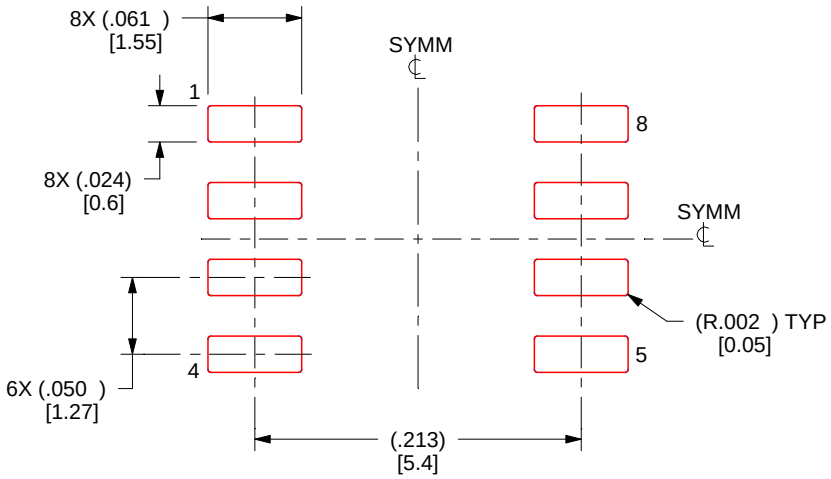
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



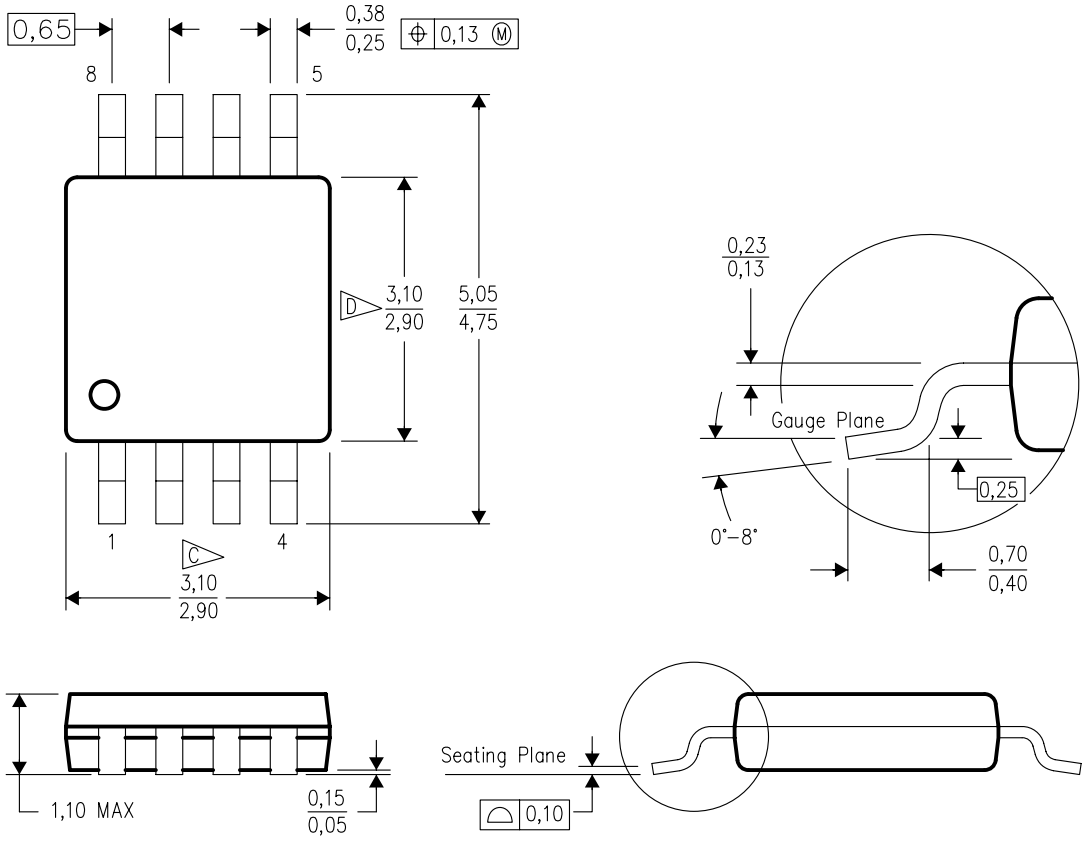
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

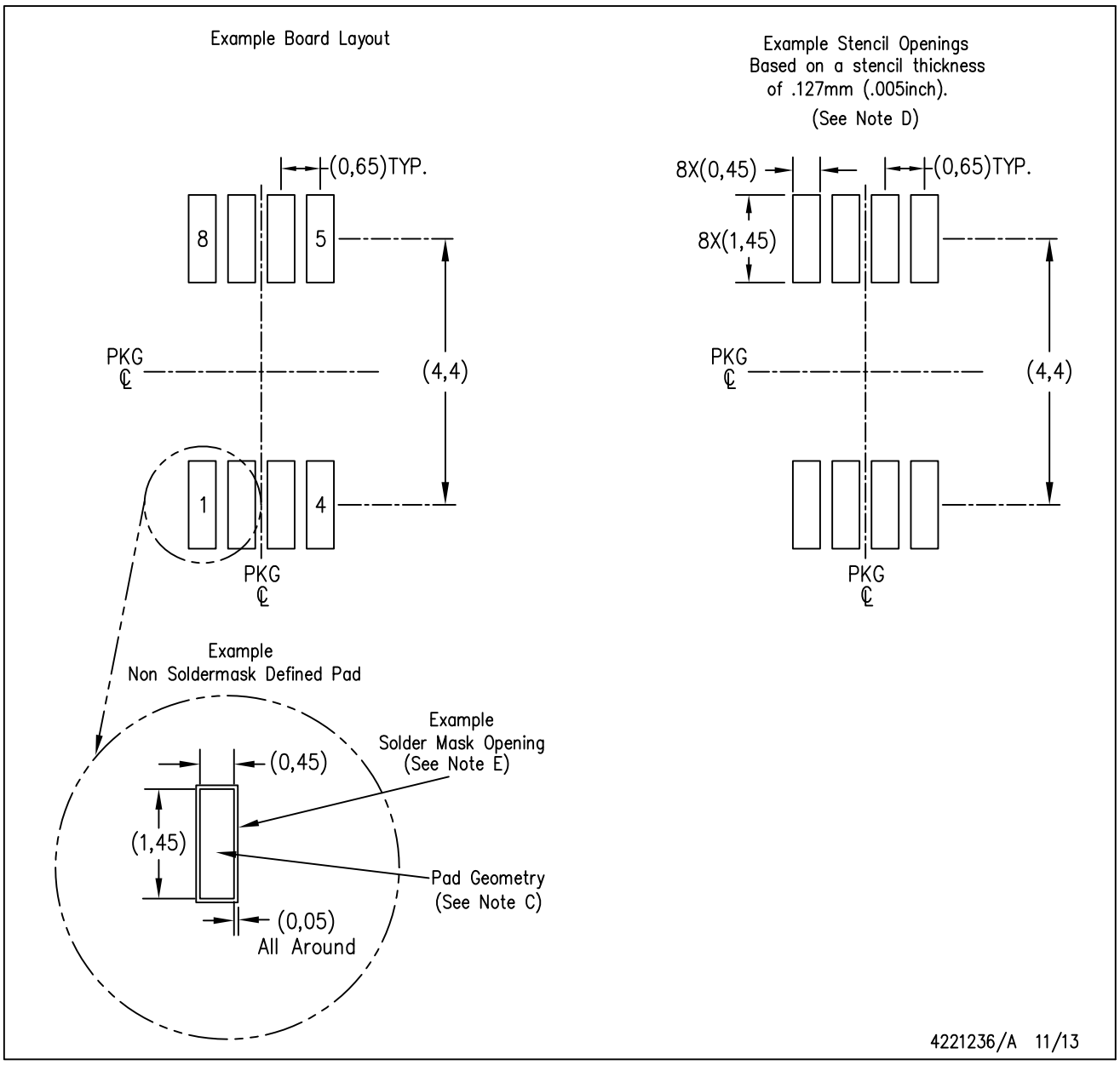
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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