

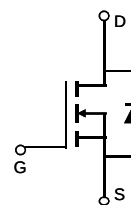
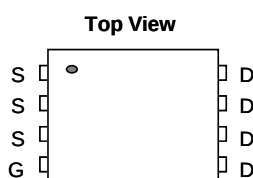
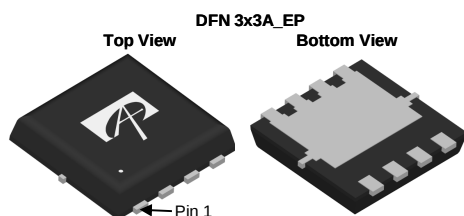
General Description

The AON7458 is fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability this device can be adopted quickly into new and existing offline power supply designs. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

Product Summary

V_{DS}	300V@150°C
I_D (at $V_{GS}=10V$)	5A
$R_{DS(on)}$ (at $V_{GS}=10V$)	< 0.56Ω

100% UIS Tested!
 100% R_g Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current ^B	I_D	5	A
		3.2	
Pulsed Drain Current ^C	I_{DM}	16	
Continuous Drain Current	I_{DSM}	1.5	A
		1.2	
Avalanche Current ^C	I_{AR}	2.1	A
Repetitive avalanche energy ^C	E_{AR}	66	mJ
Single pulsed avalanche energy ^G	E_{AS}	132	mJ
Peak diode recovery dv/dt	dv/dt	5	V/ns
Power Dissipation ^B	P_D	33	W
		13	W
Power Dissipation ^A	P_{DSM}	3.1	W
		2	W
Junction and Storage Temperature Range	T_J, T_{STG}	-50 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient ^{A D}		60	75	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.1	3.7	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	250			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		300		
BV _{DSS} /ΔT _J	Zero Gate Voltage Drain Current	I _D =250μA, V _{GS} =0V		0.25		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =250V, V _{GS} =0V			1	μA
		V _{DS} =200V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3.1	3.7	4.3	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =1.5A		0.46	0.56	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =1.5A		5		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				5	A
I _{SM}	Maximum Body-Diode Pulsed Current				16	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	240	306	370	pF
C _{oss}	Output Capacitance		34	51	68	pF
C _{rss}	Reverse Transfer Capacitance			3.2		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.7	3.4	5.1	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =200V, I _D =1.5A	4.8	6.0	7.2	nC
Q _{gs}	Gate Source Charge			2.0		nC
Q _{gd}	Gate Drain Charge			1.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =125V, I _D =1.5A, R _G =25Ω		14		ns
t _r	Turn-On Rise Time			12		ns
t _{D(off)}	Turn-Off DelayTime			23		ns
t _f	Turn-Off Fall Time			12		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =1.5A, dI/dt=100A/μs, V _{DS} =100V	52	77	102	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =1.5A, dI/dt=100A/μs, V _{DS} =100V	0.2	0.29	0.40	μC

A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power Dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation PD is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

H. L=60mH, I_{AS}=2.1A, V_{DD}=150V, R_G=10Ω, Starting T_J=25° C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

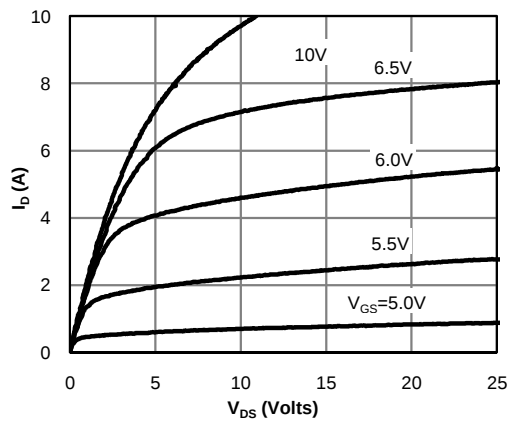


Fig 1: On-Region Characteristics

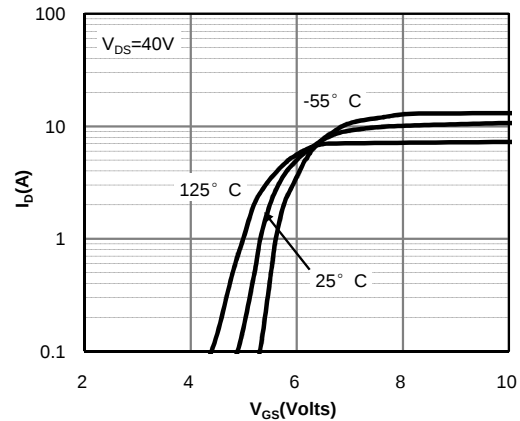


Figure 2: Transfer Characteristics

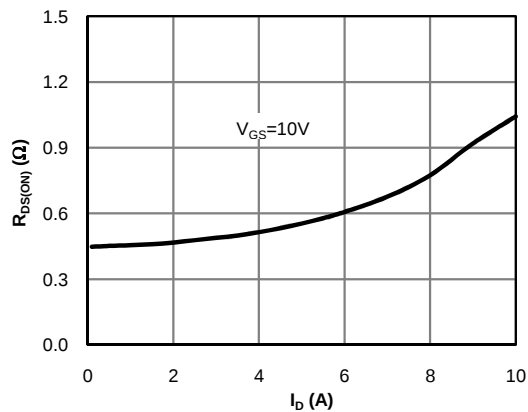


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

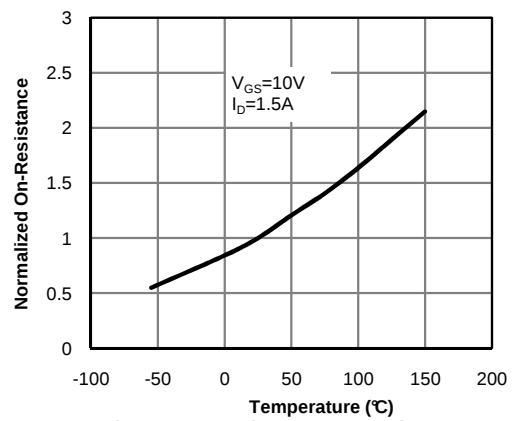


Figure 4: On-Resistance vs. Junction Temperature

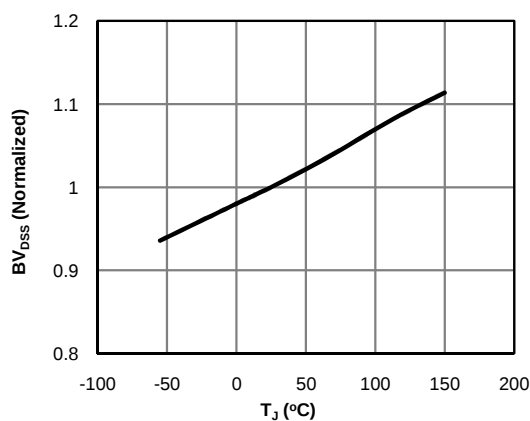


Figure 5: Break Down vs. Junction Temperature

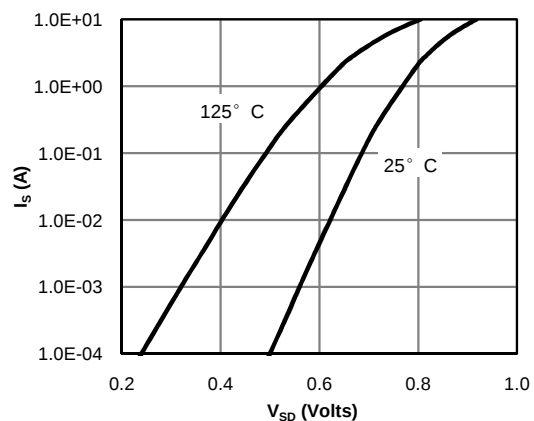


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

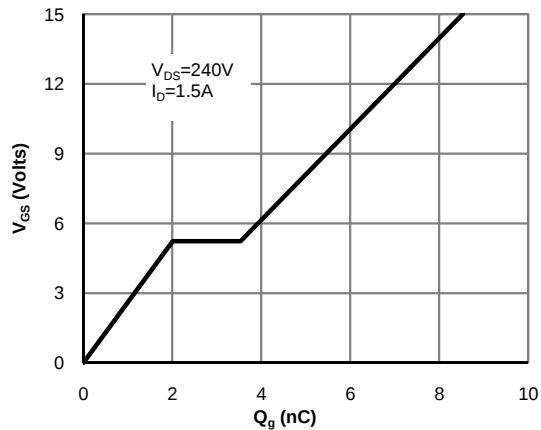


Figure 7: Gate-Charge Characteristics

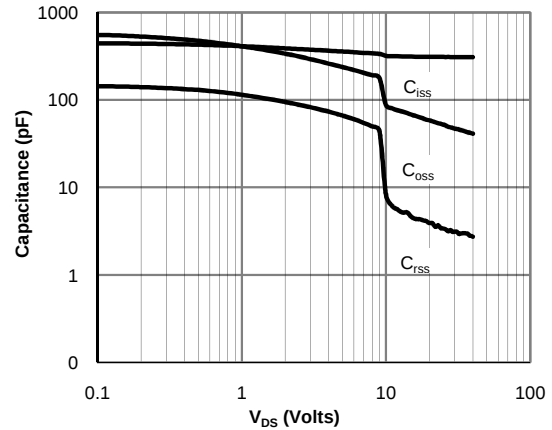


Figure 8: Capacitance Characteristics

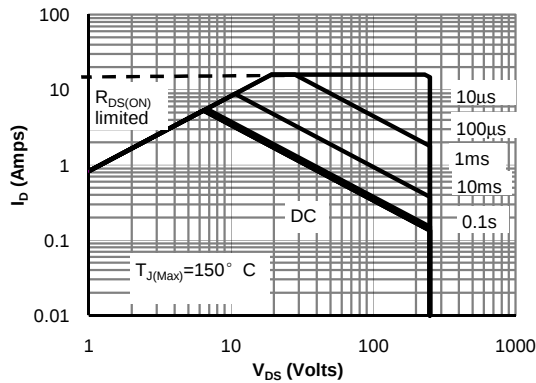


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

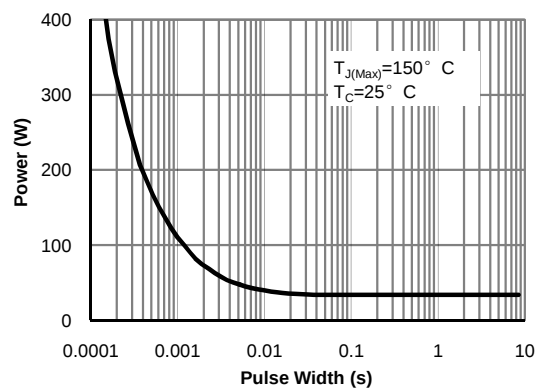


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

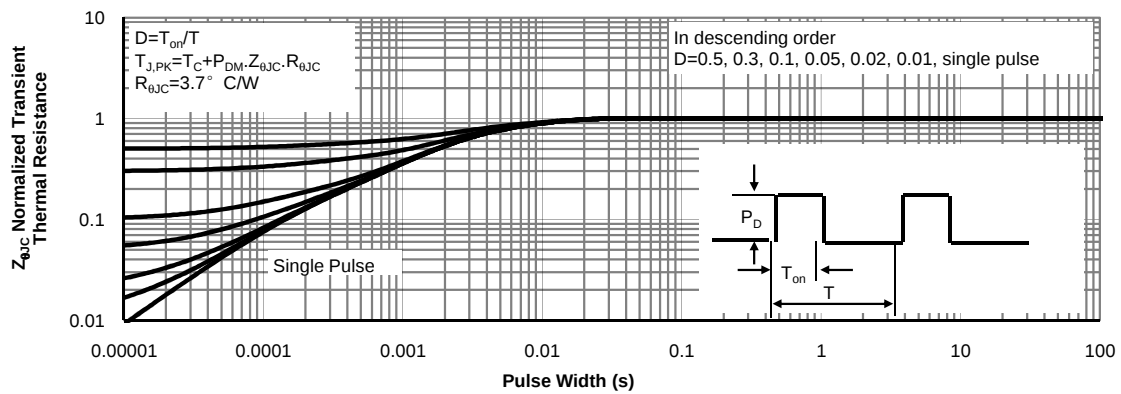


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

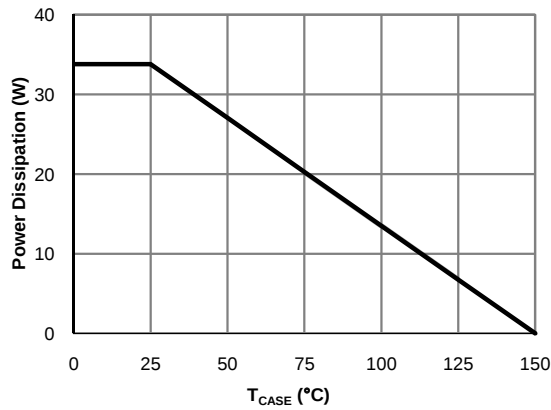


Figure 12: Power De-rating (Note B)

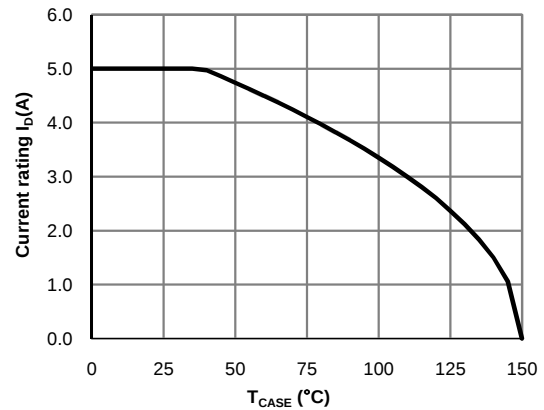


Figure 13: Current De-rating (Note B)

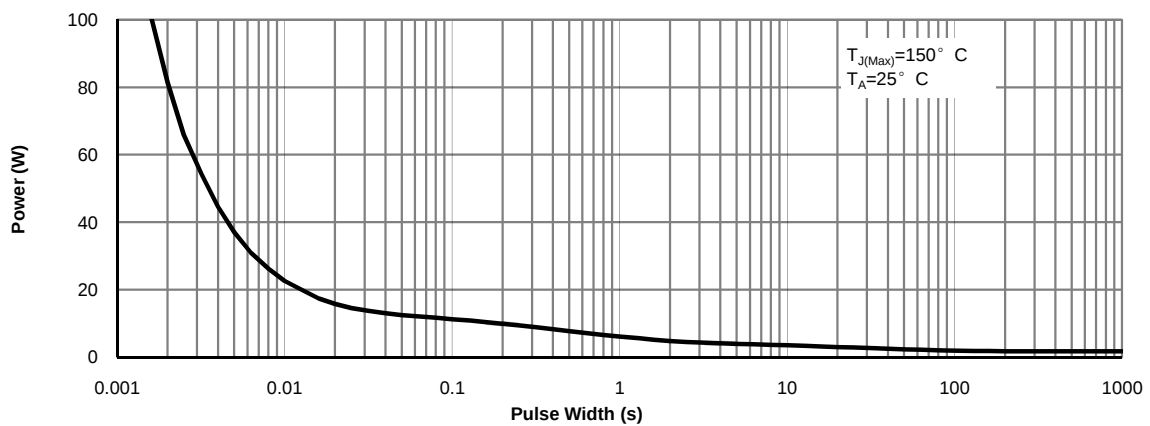


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

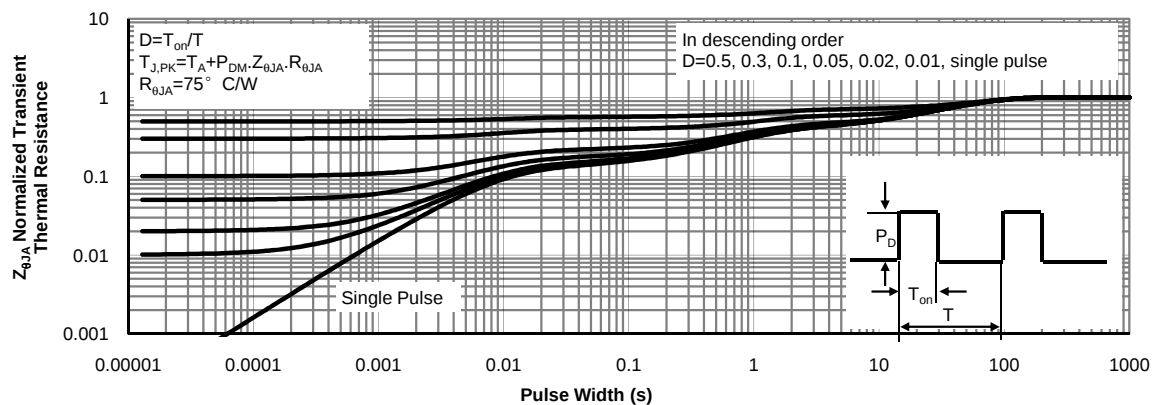
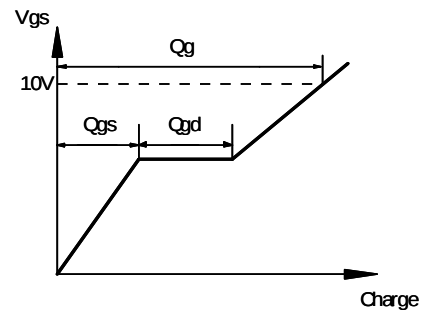
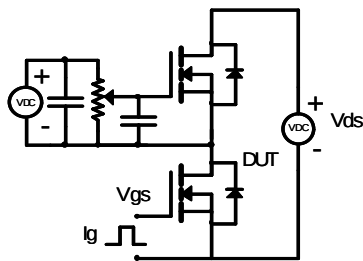
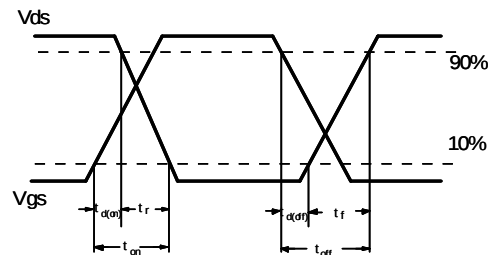
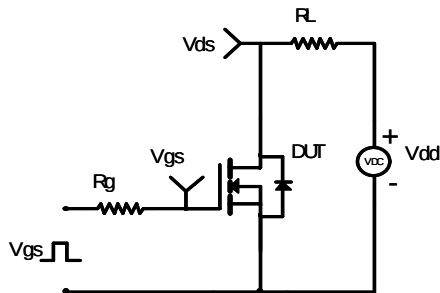


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

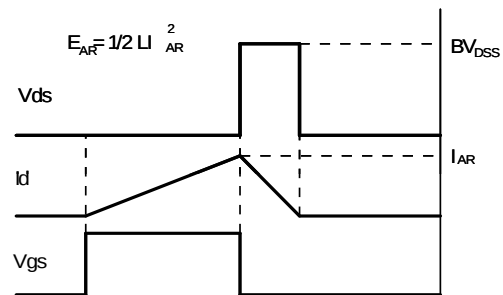
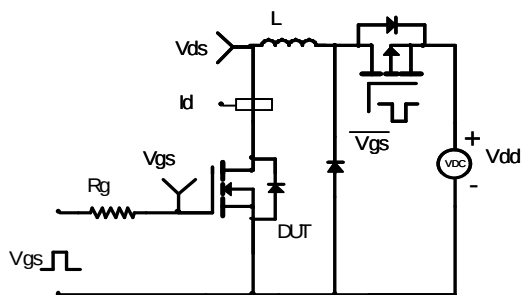
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

