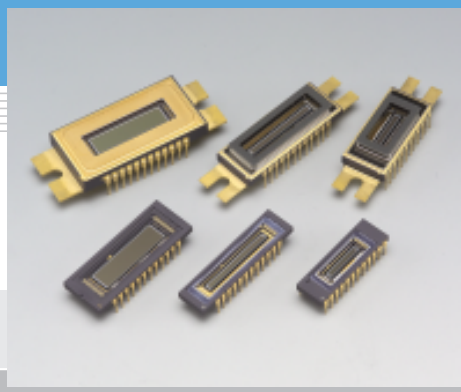


CCD area image sensor

S9970/S9971 series

Low dark signal · low readout noise/front-illuminated FFT-CCD



S9970/S9971 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. S9970/S9971 series offer lower dark current and lower readout noise than S7010/S7011 series that have been marketed. By using the binning operation, S9970/S9971 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S9970/S9971 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S9970/S9971 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.

S9970/S9971 series have an effective pixel size of $24 \times 24 \mu\text{m}$ and are available in image areas ranging from $12.288 \text{ (H)} \times 1.44 \text{ (V)} \text{ mm}^2$ (512×60 pixels) up to a large image area of $24.576 \text{ (H)} \times 6.048 \text{ (V)} \text{ mm}^2$ (1024×252 pixels). S9970/S9971 series are pin compatible with S7010/S7011 series. (Operating conditions are a little bit changed from S7010/S7011 series.)

Features

- Low dark signal: $10 \text{ e}^-/\text{pixel/s}$ Typ. (0°C , MPP mode)
- Low readout noise: $4 \text{ e}^-_{\text{rms}}$ Typ.
- $512 \text{ (H)} \times 60 \text{ (V)}$ to $1024 \text{ (H)} \times 252 \text{ (V)}$ pixel format
- Pixel size: $24 \times 24 \mu\text{m}$
- Line/pixel binning
- 100 % fill factor
- Wide dynamic range
- MPP operation

Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Suitable multichannel Detector head
S9970-0906	Non-cooled	532×64	512×60	12.288×1.440	C7020
S9970-1006		1044×64	1024×60	24.576×1.440	
S9970-1007		1044×128	1024×124	24.576×2.976	
S9970-1008		1044×256	1024×252	24.576×6.048	
S9971-0906	One-stage TE-cooled	532×64	512×60	12.288×1.440	C7021
S9971-1006		1044×64	1024×60	24.576×1.440	
S9971-1007		1044×128	1024×124	24.576×2.976	
S9971-1008		1044×256	1024×252	24.576×6.048	C7025

General ratings

Parameter	Specification
Pixel size	$24 \text{ (H)} \times 24 \text{ (V)} \mu\text{m}$
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	24 pin ceramic DIP (refer to dimensional outlines)
Window *1	S9970 series: quartz glass S9971 series: sapphire glass

*1: Temporary window type (ex. S9970-0906N) and UV coat type (ex. S9970-0906UV) are available upon request. (Temporary window is fixed by tape to protect the CCD chip and wire bonding.)

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-15	-	+15	V
IGH voltage	VIG1H, VIG2H	-15	-	+15	V
SG voltage	VSG	-15	-	+15	V
OG voltage	VOG	-15	-	+15	V
RG voltage	VRG	-15	-	+15	V
TG voltage	VTG	-15	-	+15	V
Vertical clock voltage	VP1V, VP2V	-15	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage	VOD	18	20	22	V
Reset drain voltage	VRD	11.5	12	12.5	V
Output gate voltage	VOG	1	3	5	V
Substrate voltage	VSS	-	0	-	V
Test point (vertical input source)	VISV	-	VRD	-	V
Test point (horizontal input source)	VISH	-	VRD	-	V
Test point (vertical input gate)	VIG1V, VIG2V	-8	0	-	V
Test point (horizontal input gate)	VIG1H, VIG2H	-8	0	-	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	0	4	V
	Low	VP1VL, VP2VL	-9	-8	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	0	4	V
	Low	VP1HL, VP2HL	-9	-8	
Summing gate voltage	High	VSGH	0	4	V
	Low	VSGL	-9	-8	
Reset gate voltage	High	VRGH	0	4	V
	Low	VRGL	-9	-8	
Transfer gate voltage	High	VTGH	0	4	V
	Low	VTGL	-9	-8	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	0.1	1	MHz
Vertical shift register capacitance	S9970/S9971-0906	CP1V, CP2V	-	-	750	pF
	S9970/S9971-1006		-	-	1500	
	S9970/S9971-1007		-	-	3000	
	S9970/S9971-1008		-	-	6000	
Horizontal shift register capacitance	S9970/S9971-0906	CP1H, CP2H	-	-	100	pF
	S9970/S9971-1006		-	-	180	
	S9970/S9971-1007		-	-	180	
	S9970/S9971-1008		-	-	180	
Summing gate capacitance	CSG	-	-	7	-	pF
Reset gate capacitance	CRG	-	-	7	-	pF
Transfer gate capacitance	S9970/S9971-0906	CTG	-	-	60	pF
	S9970/S9971-1006		-	-	100	
	S9970/S9971-1007		-	-	100	
	S9970/S9971-1008		-	-	100	
Transfer efficiency	CTE	*2	0.99995	0.99999	-	-
DC output level	Vout	*3	12	15	18	V
Output impedance	Zo	*3	-	3	-	kΩ
Power dissipation	P	*3, *4	-	15	-	mW

*2: Charge transfer efficiency per pixel, measured at half of the full well capacity.

*3: The values depend on the load resistance. (VOD=20 V, Load resistance=22 kΩ)

*4: Power dissipation of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	-	150	300	-	ke ⁻
	Horizontal			300	600	-	
CCD node sensitivity		Sv	*5	-	3.5	-	μV/e ⁻
Dark current (MPP mode)	+25 °C	DS	*6	-	200	3000	e ⁻ /pixel/s
	0 °C			-	10	150	
Readout noise		Nr	*7	-	4	18	e ⁻ rms
Dynamic range	Line binning	-	*8	16666	150000	-	-
	Area scanning			8333	75000	-	
Spectral response range		λ	-	-	400 to 1100	-	nm
Photo response non-uniformity		PRNU	*9	-	-	±10	%
Blemish	Point defects	-	*10	-	-	0	-
	Cluster defects		*11	-	-	0	
	Column defects		*12	-	-	0	

*5: V_{OD}=20 V , Load resistance=22 kΩ

*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

*7: -40 °C, operating frequency is 80 kHz.

*8: DR = Fw / Nr

*9: Measured at half of the full well capacity. PRNU = noise / signal × 100 [%], noise: fixed pattern noise (peak to peak)

*10: White spots > 3 % of full well at 0 °C after Ts=1 s

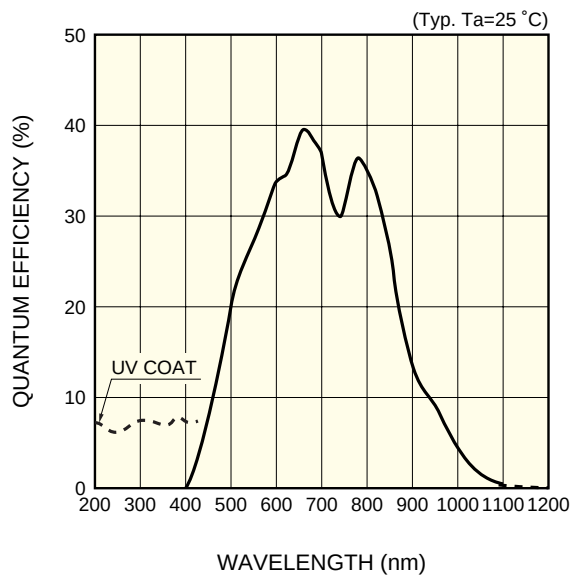
Black spots

Pixels whose sensitivity is lower than one-half of the average pixel output. (Measured with uniform light producing one-half of the saturation charge)

*11: 2 to 9 contiguous defective pixels

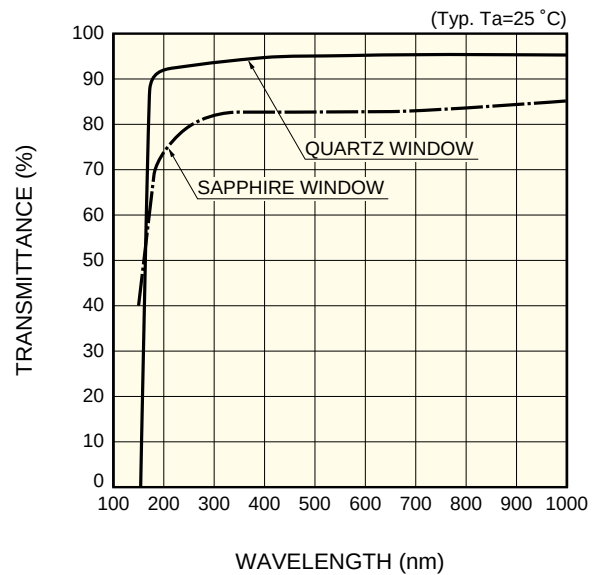
*12: 10 or more contiguous defective pixels

■ Spectral response (without window)



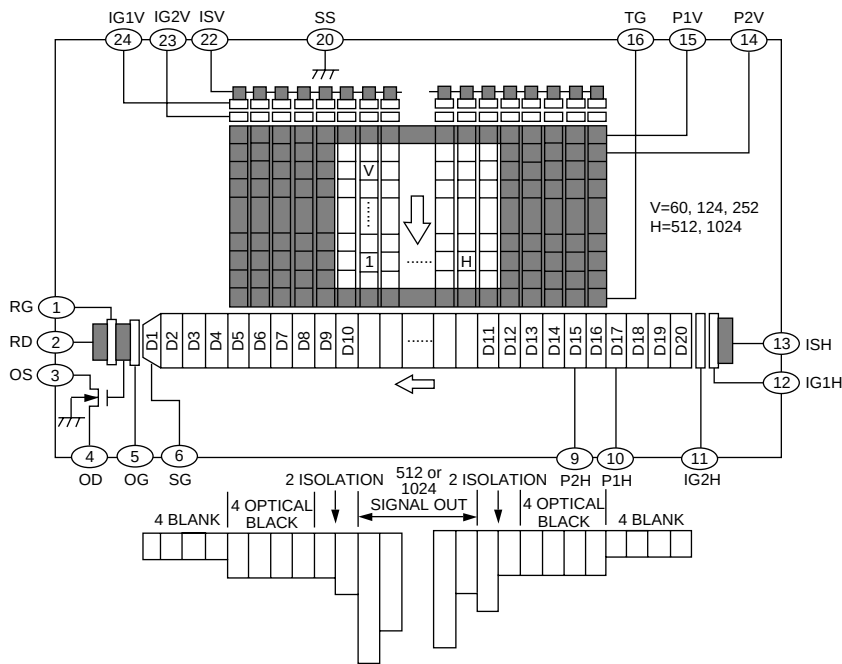
KMPDB0244EB

■ Spectral transmittance characteristics



KMPDB0101EA

■ Device structure, line output format



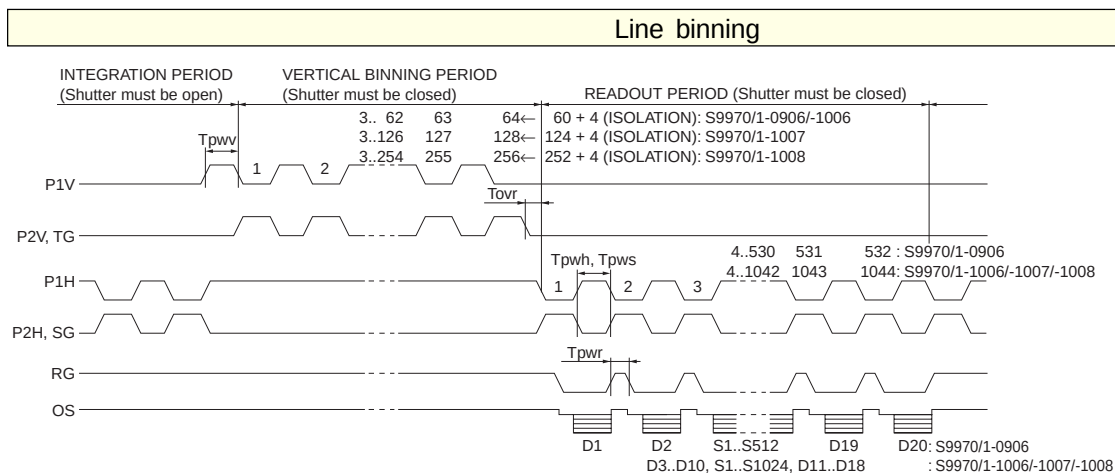
KMPDC0015EE

Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	512 or 1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	60, 124 or 252	2

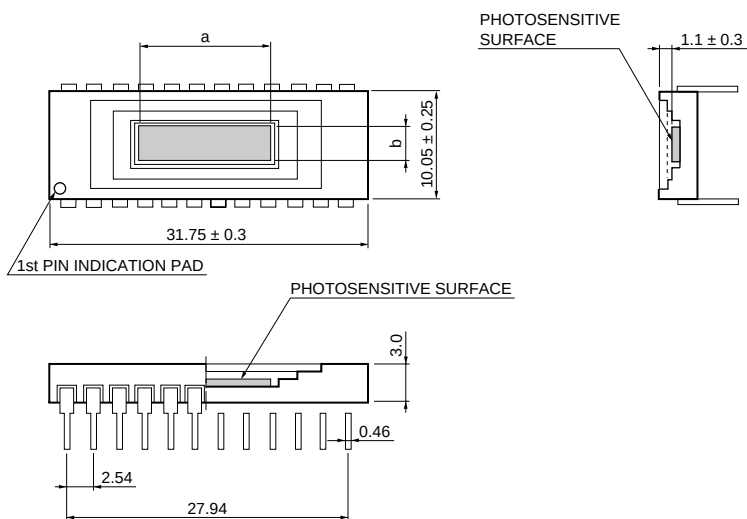
■ Timing chart



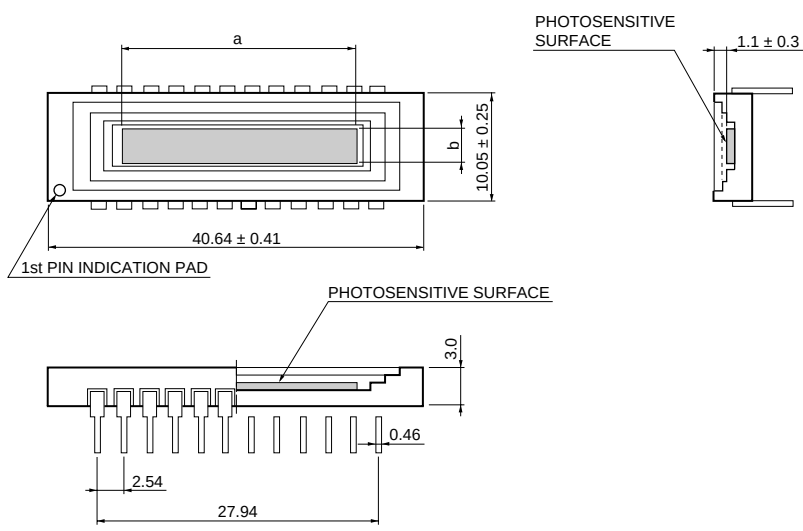
KMPDC0227EA

■ Dimensional outlines (unit: mm)

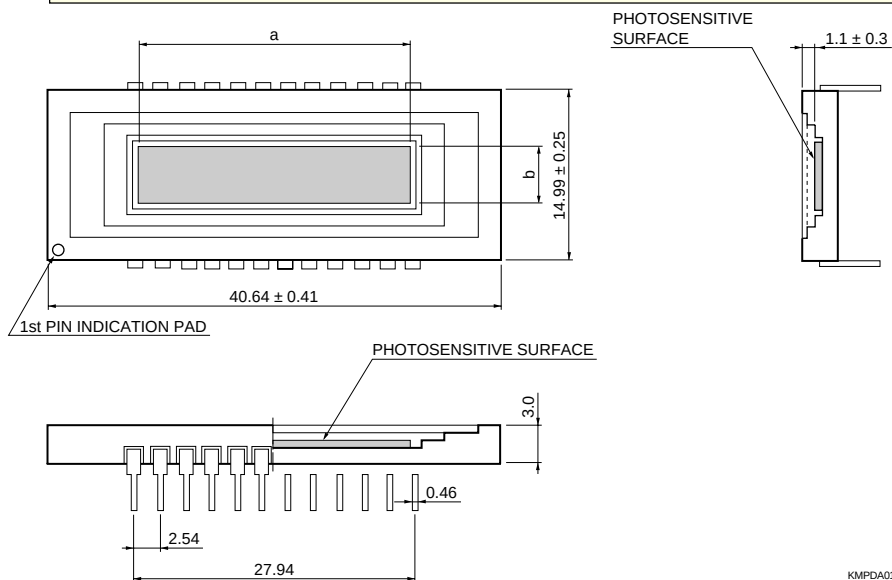
S9970-0906



S9970-1006/-1007

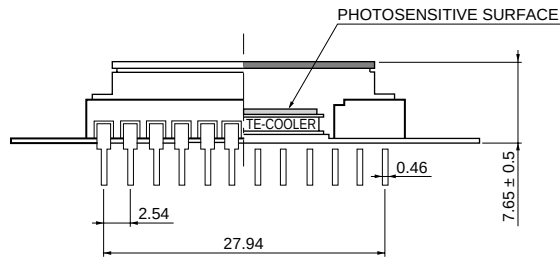
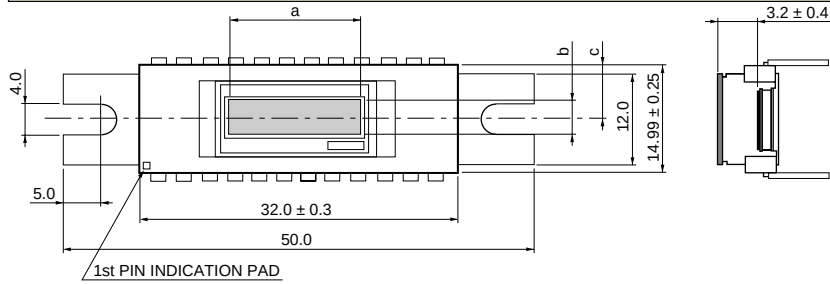


S9970-1008



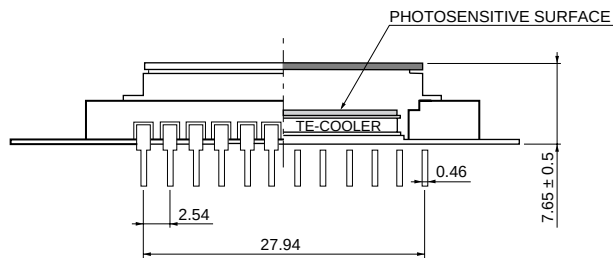
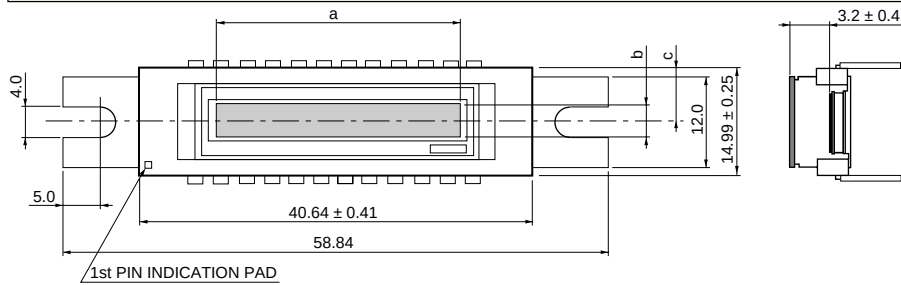
Type No.	Active area	
	a	b
S9970-0906	12.288 (H)	1.440 (V)
S9970-1006	24.576 (H)	1.440 (V)
S9970-1007	24.576 (H)	2.976 (V)
S9970-1008	24.576 (H)	6.048 (V)

S9971-0906



KMPDA0196EA

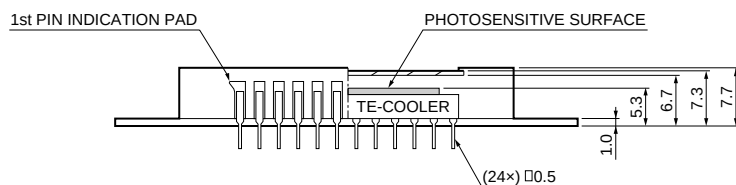
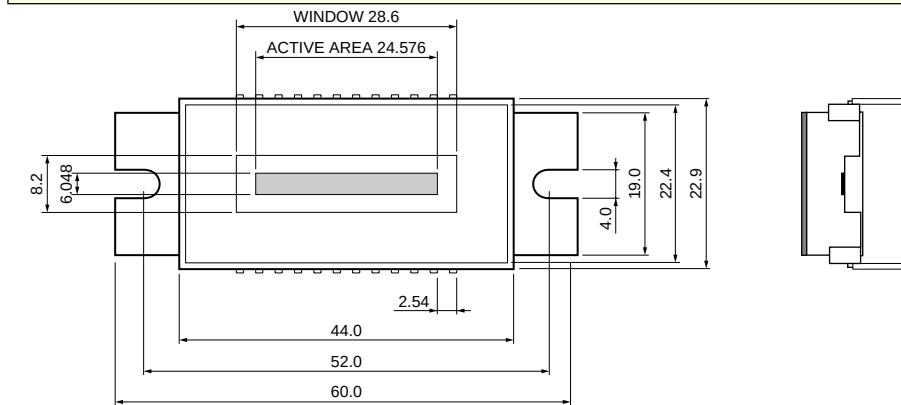
S9971-1006/1007



KMPDA0197EA

Type No.	Active area		
	a	b	c
S9971-0906	12.288 (H)	1.440 (V)	7.5
S9971-1006	24.576 (H)	1.440 (V)	7.5
S9971-1007	24.576 (H)	2.976 (V)	7.1

S9971-1008



KMPDA0198EA

■ Pin connections

Pin No.	S9970 series		S9971 series		Remark
	Symbol	Description	Symbol	Description	
1	RG	Reset gate	RG	Reset gate	
2	RD	Reset drain	RD	Reset drain	
3	OS	Output transistor source	OS	Output transistor source	
4	OD	Output transistor drain	OD	Output transistor drain	
5	OG	Output gate	OG	Output gate	
6	SG	Summing gate	SG	Summing gate	Same timing as P2H
7	NC		Th1	Thermistor	
8	NC		Th2	Thermistor	
9	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	Shorted to GND
12	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	Shorted to GND
13	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Shorted to RD
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	TG *15	Transfer gate	TG *15	Transfer gate	Same timing as P2V
17	NC		NC		
18	NC		P-	TE-cooler-	
19	NC		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	
21	NC		NC		
22	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	Shorted to GND
24	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	Shorted to GND

*15: TG is an isolation gate between vertical register and horizontal register. In standard operation, the same pulse as P2V should be applied to TG.

■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S9971-0906	S9971-1006/-1007	S9971-1008	Unit
Internal resistance	Rint	Ta=25 °C	2.8	6.0	1.2	Ω
Maximum current *16	I _{max}	T _c *17=Th *18=25 °C	1.5	1.5	3.0	A
Maximum voltage	V _{max}	T _c *17=Th *18=25 °C	4.4	8.8	3.6	V
Maximum heat absorption *19	Q _{max}		3.4	6.7	5.1	W
Maximum temperature of hot side	-		70			°C

*16: Maximum current I_{max}:

If the current is greater than I_{max}, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

*17: Temperature of cool side of thermoelectric cooler

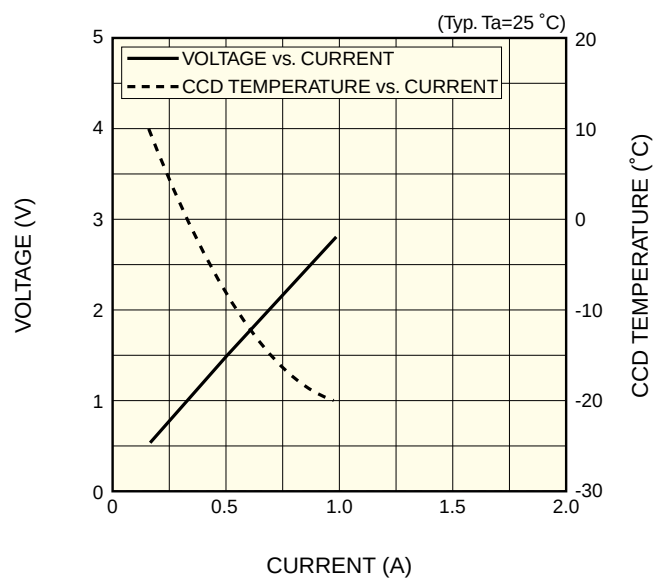
*18: Temperature of hot side of thermoelectric cooler

*19: Maximum heat absorption Q_{max}

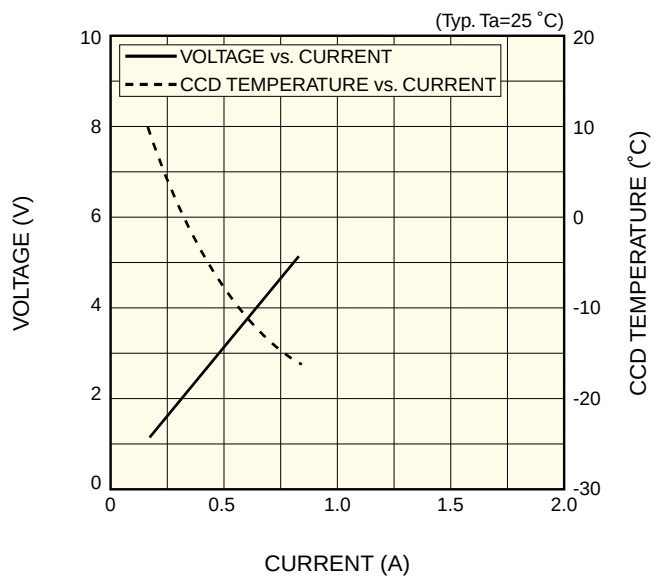
This is a heat absorption when the maximum current is supplied to the TE-cooler.

TE-cooler characteristics

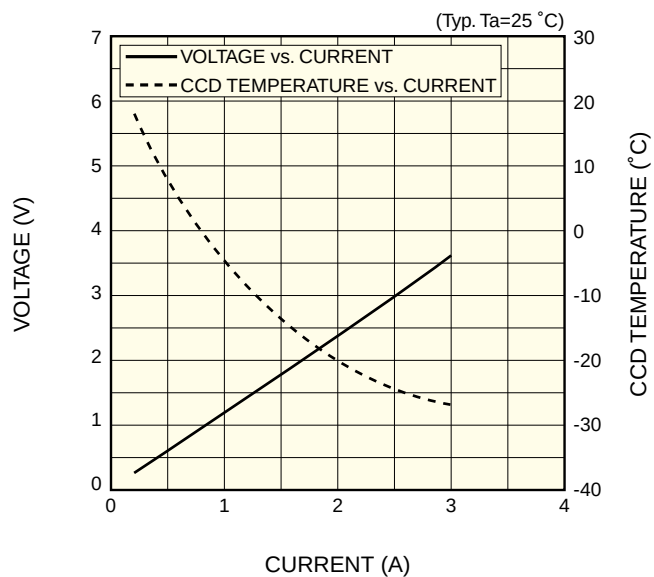
S9971-0906



S9971-1006/-1007



S9971-1008



■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_1 = R_2 \times \exp B (1 / T_1 - 1 / T_2)$$

where R1 is the resistance at absolute temperature T1 (K)

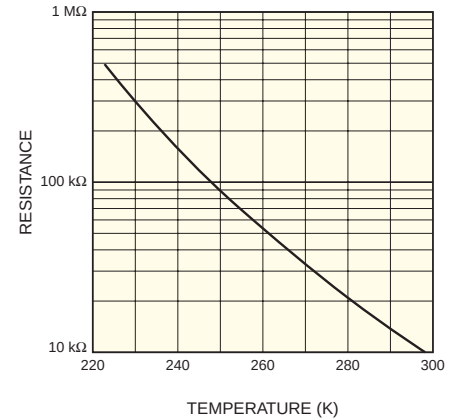
R2 is the resistance at absolute temperature T2 (K)

B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.

$$R (298K) = 10 \text{ k}\Omega$$

$$B (298K / 323K) = 3450 \text{ K}$$



KMPD80111EB

■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist strap, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

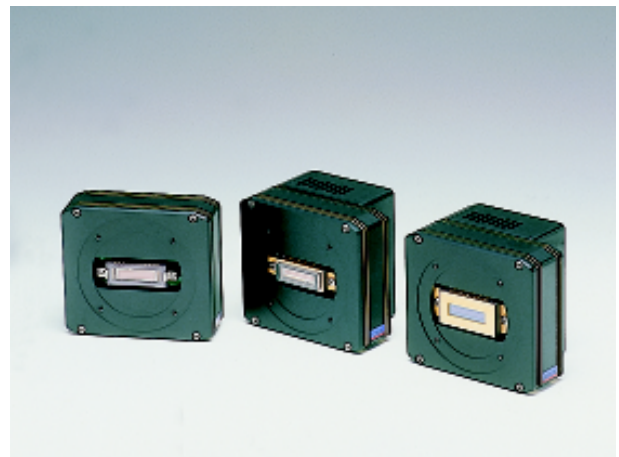
When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

Multichannel detector head (C7020, C7021, C7025)

Features

- C7020: for S9970 series
- C7021: for S9971-0906/-1006/-1007
- C7025: for S9971-1008
- Area scanning or full line-binning operation
- Readout frequency: 250 kHz
- Readout noise: 20 e⁻rms
- ΔT=50 °C (ΔT changes by radiation method.)

Input	Symbol	Value
Supply voltage	VD1	+5 Vdc, 200 mA
	VA1+	+15 Vdc, +100 mA
	VA1-	-15 Vdc, -100 mA
	VA2	+24 Vdc, 30 mA
	VD2	+5 Vdc, 30 mA (C7021, C7025)
	Vp	+5 Vdc, 2.5 A (C7021, C7025)
	VF	+12 Vdc, 100 mA (C7021, C7025)
Master start	φms	HCMOS logic compatible
Master clock	φmc	HCMOS logic compatible, 1 MHz



HAMAMATSU

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184, www.hamamatsu.com

U.S.A.: Hamamatsu Corporation, 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH, Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trappu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741

Information furnished by HAMAMATSU is believed to be reliable. However, no responsibility is assumed for possible inaccuracies or omissions. Specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein. ©2007 Hamamatsu Photonics K.K.