

QUAD, 16-BIT, RAIL-TO-RAIL VOLTAGE OUTPUT, PARALLEL INTERFACE, DIGITAL-TO-ANALOG CONVERTER

FEATURES

- Single Supply: +2.7 V to +5.5 V
- Micropower Operation: 950 μ A @ 5 V
- Rail-To-Rail Voltage Output
- Ultralow Crosstalk: -110 dB
- Settling Time: 10 μ s To $\pm 0.003\%$ FSR
- 16-Bit Monotonic
- Offset Error: ± 0.3 mV
- Gain Error: ± 1 mV
- Total Error: ± 3 mV
- Per-Channel V_{REF+} , V_{REF-} , V_{FB} Pins
- Logic Compatible: +1.8 V to +5.5 V
- Readback Capability
- Double Buffered Inputs
- Simultaneous or Sequential Update
- Schmitt-Triggered Digital Inputs
- Hardware Reset
- 48-Lead TQFP Package

APPLICATIONS

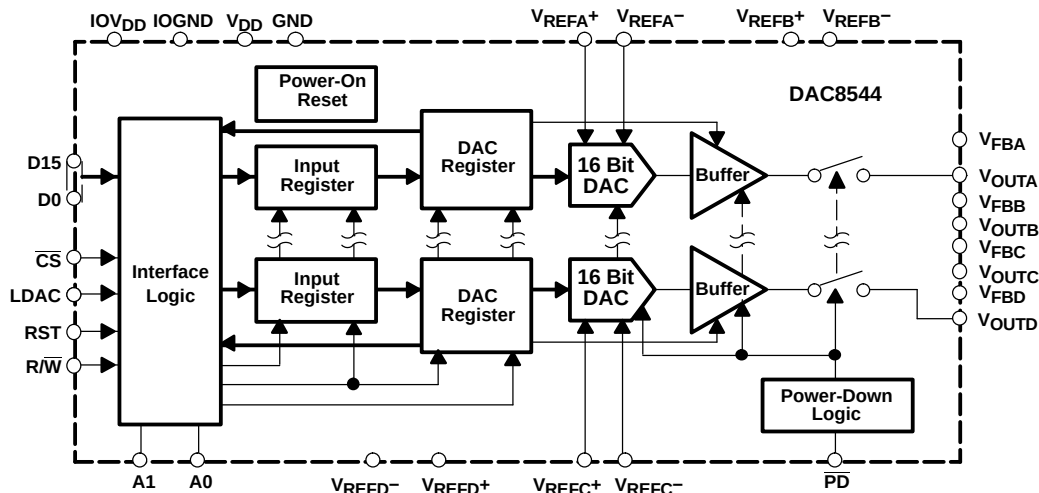
- Process Control
- Data Acquisition Systems
- Closed-Loop Servo Control
- PC Peripherals
- Optical Networking

DESCRIPTION

The DAC8544 is a low-power, quad-channel, 16-bit, voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail voltage swing to be achieved at the output. The DAC8544 is 16-bit monotonic and offers exceptional absolute accuracy with ultralow crosstalk. The DAC8544 uses a 16-bit parallel interface and features additional power-down function pins as well as hardware-enabled, synchronous DAC updating and reset capability.

The DAC8544 requires an external reference voltage to set the output range of the DAC. The device incorporates a power-on-reset circuit that ensures that the DAC outputs power up at zero volt and remains there until a valid write takes place. In addition, the DAC8544 contains a power-down feature, accessed via $\overline{PD}$ pin, that reduces the current consumption of the device to 400 nA at 5 V. The power consumption is typically under 5 mW at $V_{DD} = 5$ V.

The DAC8544 is available in a 48-lead TQFP package with an operating temperature range of -40°C to $+105^{\circ}\text{C}$.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	TA	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC8544	48 - TQFP	PFB	-40°C to 105°C	DAC8544I	DAC8544IPFB	Tray
					DAC8544IPFBR	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

V_{DD} to GND	-0.3 V to 6 V
IOV_{DD} to IOGND	-0.3 V to 6 V
Digital input voltage to IOGND	-0.3 V to $IOV_{DD} + 0.3$ V
V_{OUT} to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating temperature range	-40°C to 105°C
Storage temperature range, Tstg	-65°C to 150°C
Junction temperature, T _J max	+150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{DD} = +2.7$ V to $+5.5$ V; $R_L = 2$ k Ω to GND; $C_L = 200$ pF to GND; all specifications -40°C to +105°C unless otherwise noted

		DAC8544			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE ⁽¹⁾					
Resolution		16			Bits
Relative Accuracy			±0.025	±.098	%FSR
Differential Nonlinearity	16-Bit Monotonic		±0.25	±1	LSB
Zero-Code Offset Error	Measured at code 485, 25°C		0.3	±3	mV
	Measured at code 485, -40°C to 105°C		1.0	±5.0	
Zero-Code Error Drift	All zeroes loaded to DAC register		-20		µV/°C
DC Crosstalk			0.1		LSB
AC Crosstalk	1-kHz sine wave		-110		dB
Gain Error	Measured at code 64714, 25°C		1.0	±3.0	mV
	Measured at code 64714, -40°C to 105°C		2.0	±5.0	
Gain Error Drift			-5		ppm of FSR/°C
Full-Scale Error	Measured at code 64714, 25°C		0.5	±3.0	mV
	Measured at code 64714, -40°C to 105°C		1.0	±5.0	
OUTPUT CHARACTERISTICS ⁽²⁾					
Output Voltage Range		0		V _{REF}	V
Output Voltage Settling Time	R _L = 2 kΩ; C _L <200 pF		8	10	µs
	R _L = 2 kΩ; C _L <500 pF		12		

(1) Linearity calculated using a reduced code range of 485 to 64714. Output unloaded.

(2) Assured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)
 $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications -40°C to $+105^\circ\text{C}$ unless otherwise noted

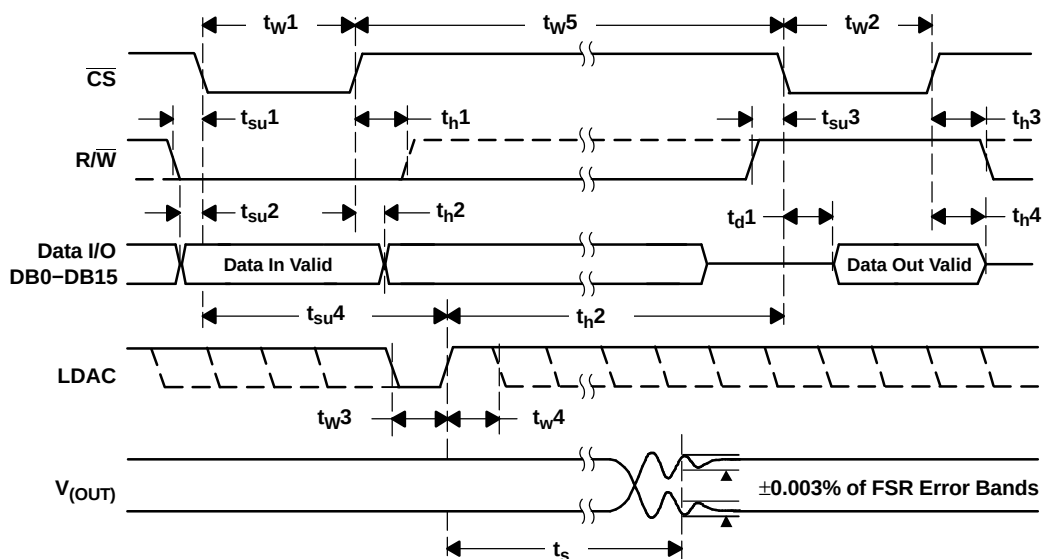
		DAC8544			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	R _L = 2 kΩ; C _L <200 pF		1		V/μs
Capacitive Load Stability	R _L = ∞		470		pF
	R _L = 2 kΩ		1000		pF
Digital-to-Analog Glitch Impulse			20		nV-s
Digital Feedthrough			0.5		nV-s
DC Output Impedance			1		Ω
Short-Circuit Current	V _{DD} = +5 V		50		mA
	V _{DD} = +3 V		20		
Power-Up Time	Coming out of power-down mode, V _{DD} = +5 V		2.5		μs
	Coming out of power-down mode, V _{DD} = +3 V		5		
REFERENCE INPUT					
V _{REF+} Input Range		0		V _{DD}	V
V _{REF-} Input Range		−0.1	0.0	V _{DD} /2	V
Reference Input Impedance			140		kΩ
LOGIC INPUTS					
Input Current				±1	μA
V _{INL} , Input Low Voltage	IOV _{DD} = +1.8 V – +5.5 V		0.3 x IOV _{DD}		V
V _{INH} , Input High Voltage	IOV _{DD} = +1.8 V – +5.5 V	0.7 x IOV _{DD}			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
V _{DD}		2.7		5.5	V
IOV _{DD}		1.8		5.5	V
I _{DD} (Normal Mode)	DAC active and excluding load current				
V _{DD} = +3.6 V to +5.5 V	VI _H = IOV _{DD} and VI _L = IOGND		1.0	1.6	mA
V _{DD} = +2.7 V to +3.6 V	VI _H = IOV _{DD} and VI _L = IOGND		0.96	1.52	
I _{DD} (All Power-Down Modes)					
V _{DD} = +3.6 V to +5.5 V	VI _H = IOV _{DD} and VI _L = IOGND		0.2	1	μA
V _{DD} = +2.7 V to +3.6 V	VI _H = IOV _{DD} and VI _L = IOGND		0.05	1	
POWER EFFICIENCY					
I _{OUT} /I _{DD}	I _{LOAD} = 2 mA, V _{DD} = +5 V		93		%

TIMING CHARACTERISTICS

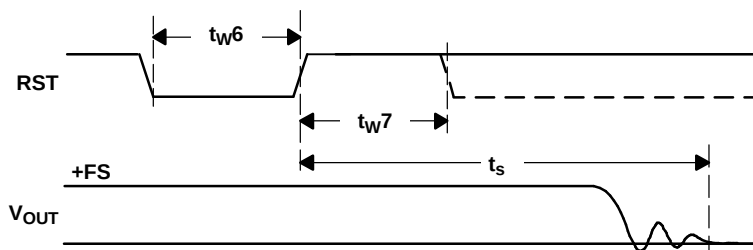
$IOV_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{DD} = 2.7\text{ V to }5.5\text{ V}$; $R_L = 2\text{ k}\Omega\text{ to GND}$; $C_L = 200\text{ pF to GND}$; all specifications $-40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{w1}	Pulse width: $\overline{CS}$ low for valid write	20			ns
t_{su1}	Setup time: $R/\overline{W}$ low before $\overline{CS}$ falling	0			ns
t_{su2}	Setup time: data in valid before $\overline{CS}$ falling	0			ns
t_{h1}	Hold time: $R/\overline{W}$ low after $\overline{CS}$ rising	10			ns
t_{h2}	Hold time: data in valid after $\overline{CS}$ rising	15			ns
t_{w2}	Pulse width: $\overline{CS}$ low for valid read	40			ns
t_{su3}	Setup time: $R/\overline{W}$ high before $\overline{CS}$ falling	30			ns
t_{d1}	Delay time: data out valid after $\overline{CS}$ falling		60	80	ns
t_{h3}	Hold time: $R/\overline{W}$ high after $\overline{CS}$ rising	10			ns
t_{h4}	Hold time: data out valid after $\overline{CS}$ rising	5		20	ns
t_{su4}	Setup time: LDAC rising after $\overline{CS}$ falling	10			ns
t_{d2}	Delay time: $\overline{CS}$ low after LDAC rising	50			ns
t_{w3}	Pulse width: LDAC low	40			ns
t_{w4}	Pulse width: LDAC high	40			ns
t_{w5}	Pulse width: $\overline{CS}$ high	80			ns
t_{w6}	Pulse width: RST low	40			ns
t_{w7}	Pulse width: RST high	40			ns
t_s	$\overline{VOUT}$ Settling time (settling time for a full-scale code change)			10	μs

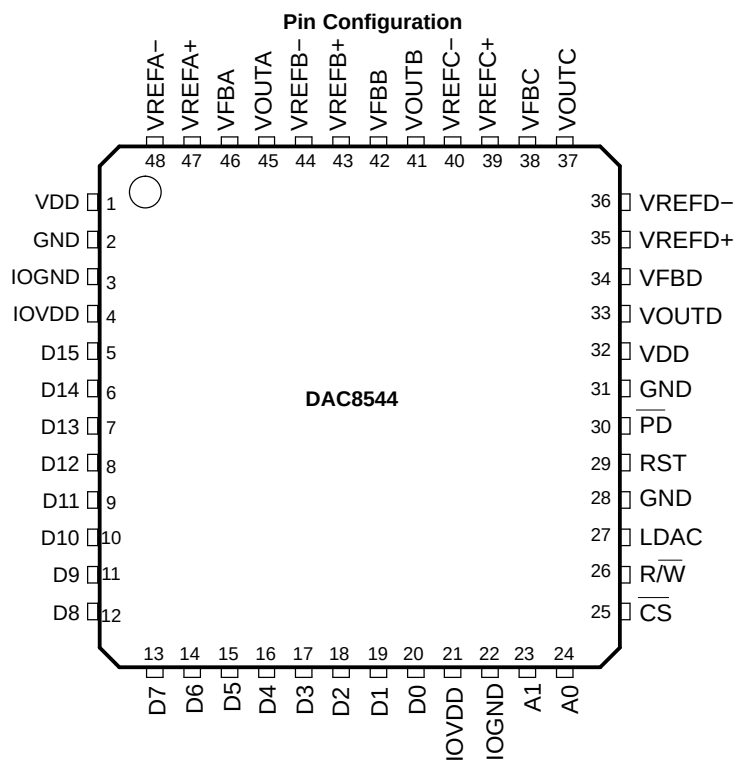
Data Read/Write Timing



Reset Timing



DEVICE INFORMATION



DEVICE INFORMATION (continued)**TERMINAL FUNCTIONS**

DAC8544		
Pin	Mnemonic	Function
1	VDD	Analog supply voltage, +2.7 V to +5.5 V
2	GND	Analog supply ground
3	IOGND	Digital supply ground
4	IOVDD	Digital supply +1.8 V to +5.5 V
5	D15	Digital input, MSB
6	D14	Digital input
7	D13	Digital input
8	D12	Digital input
9	D11	Digital input
10	D10	Digital input
11	D9	Digital input
12	D8	Digital input
13	D7	Digital input
14	D6	Digital input
15	D5	Digital input
16	D4	Digital input
17	D3	Digital input
18	D2	Digital input
19	D1	Digital input
20	D0	Digital input, LSB
21	IOVDD	Digital supply +1.8 V to +5.5 V
22	IOGND	Digital supply ground
23	A1	Address pin for selecting between DAC channels
24	A0	Address pin for selecting between DAC channels
25	$\overline{CS}$	Active-low chip select. Used with $R/\overline{W}$ to write/read data to/from device
26	$R/\overline{W}$	Read/Write select used to write data to input register or read data from DAC register
27	LDAC	Load DACs, rising edge triggered loads all DAC registers
28	GND	Analog ground
29	RST	Asynchronously resets contents of all DAC Registers to zero-scale, but does not affect input register
30	$\overline{PD}$	Active-low power-down pin puts entire device into power-down mode with DAC outputs in 3-state condition
31	GND	Analog supply ground
32	VDD	Analog supply voltage, +2.7 V to +5.5 V
33	VOU_TD	Analog output voltage from DAC-D
34	VFBD	Analog output sense for DAC-D
35	VREFD+	High reference voltage input for DAC-D
36	VREFD–	Low reference voltage input for DAC-D, normally VREFD– = GND
37	VOU_TC	Analog output voltage from DAC-C
38	VFBC	Analog output sense for DAC-C
39	VREFC+	High reference voltage input for DAC-C
40	VREFC–	Low reference voltage input for DAC-C, normally VREFC– = GND
41	VOU_TB	Analog output voltage from DAC-B
42	VFBB	Analog output sense for DAC-B
43	VREFB+	High reference voltage input for DAC-B
44	VREFB–	Low reference voltage input for DAC-B, normally VREFB– = GND
45	VOU_TA	Analog output voltage from DAC-A

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

DAC8544		
Pin	Mnemonic	Function
46	VFBA	Analog output sense for DAC-A
47	VREFA+	High reference voltage input for DAC-A
48	VREFA–	Low reference voltage input for DAC-A, normally VREFA– = GND

TYPICAL CHARACTERISTICS

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

**TOTAL UNADJUSTED ERROR
VS
DIGITAL INPUT CODE**

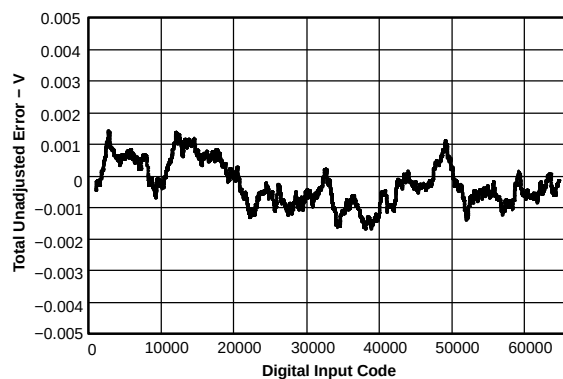


Figure 1.

**ERROR
VS
TEMPERATURE**

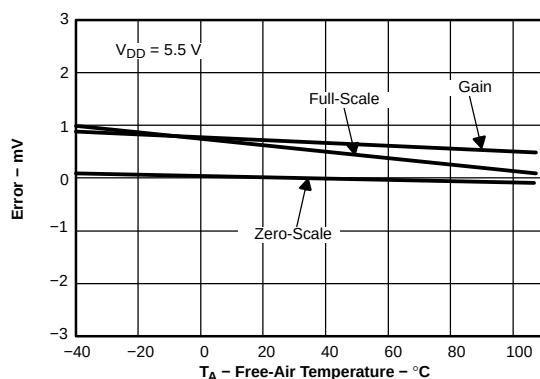


Figure 2.

**ERROR
VS
TEMPERATURE**

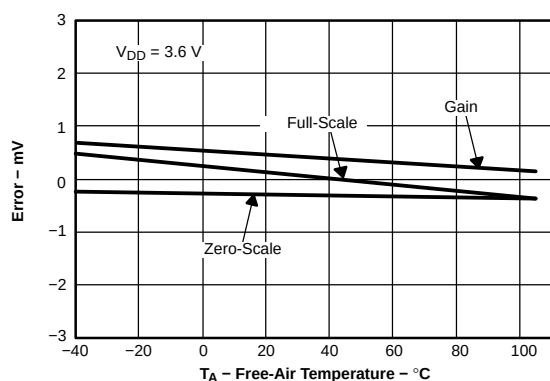


Figure 3.

**OFFSET ERROR DISTRIBUTION
(ACROSS MANY SAMPLES)**

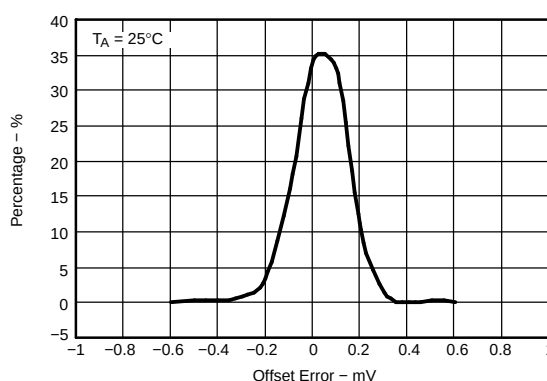


Figure 4.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

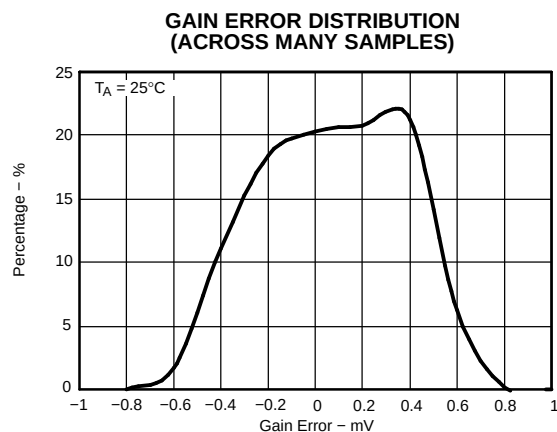


Figure 5.

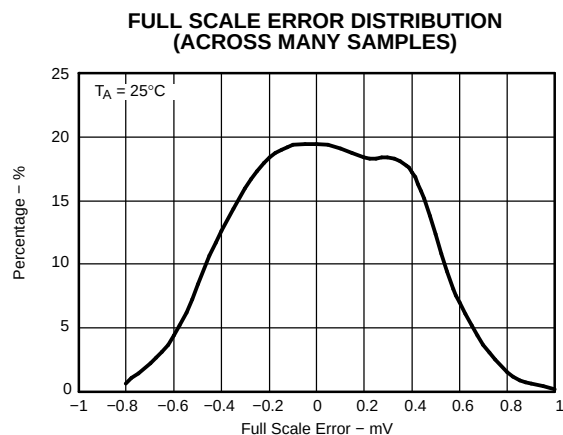


Figure 6.

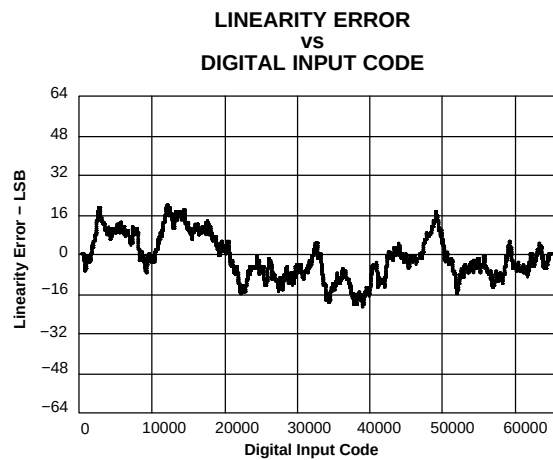


Figure 7.

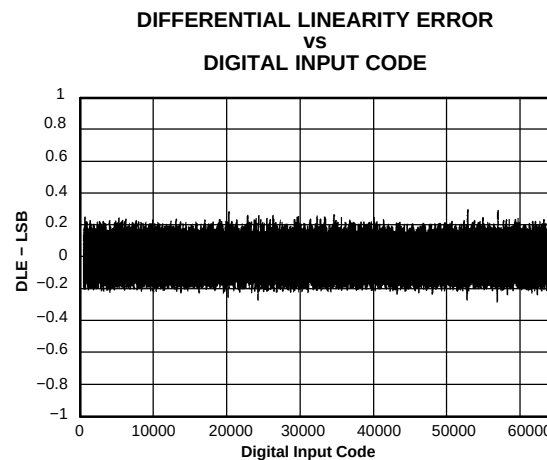


Figure 8.

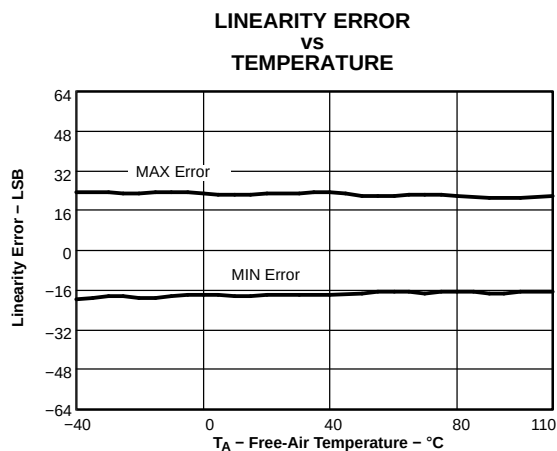


Figure 9.

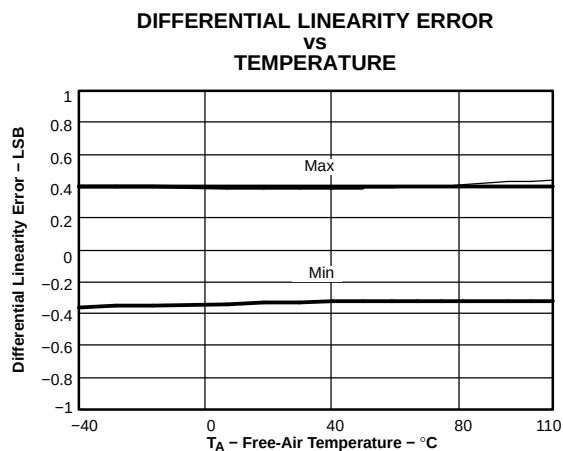


Figure 10.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

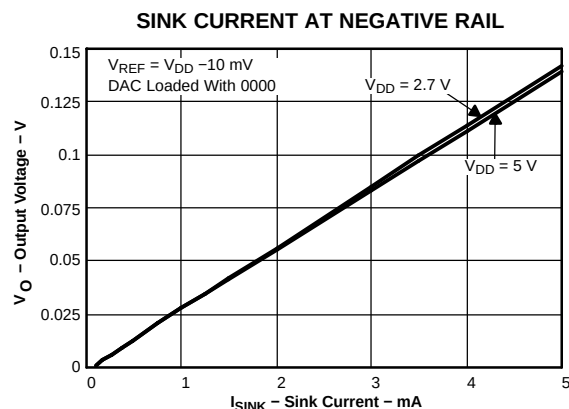


Figure 11.

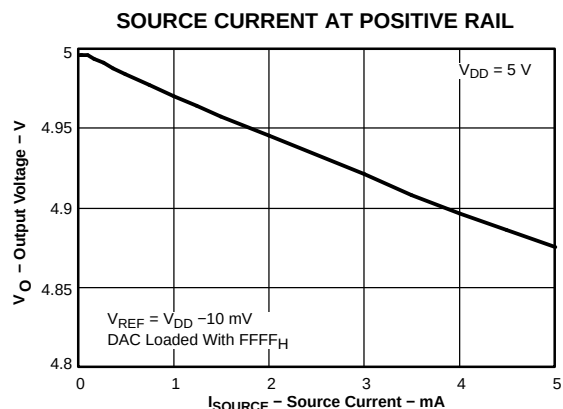


Figure 12.

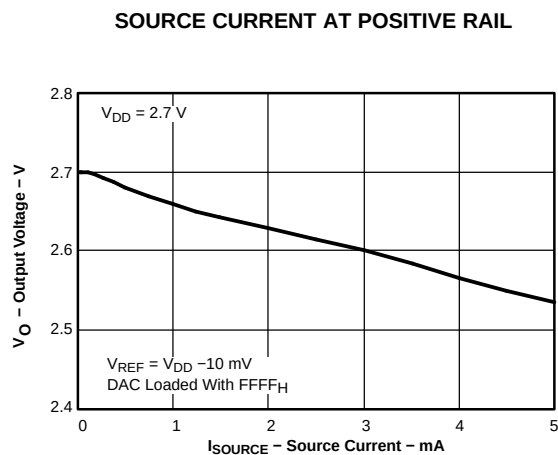


Figure 13.

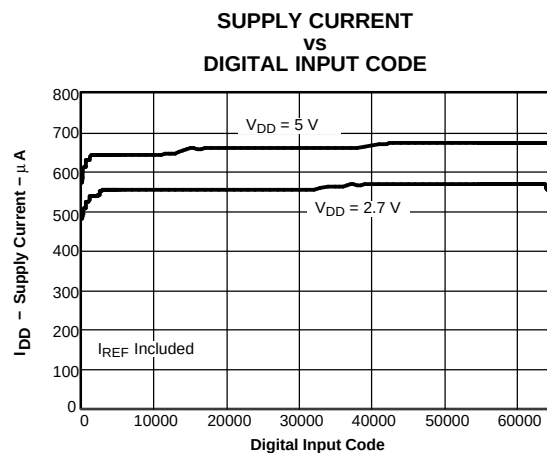


Figure 14.

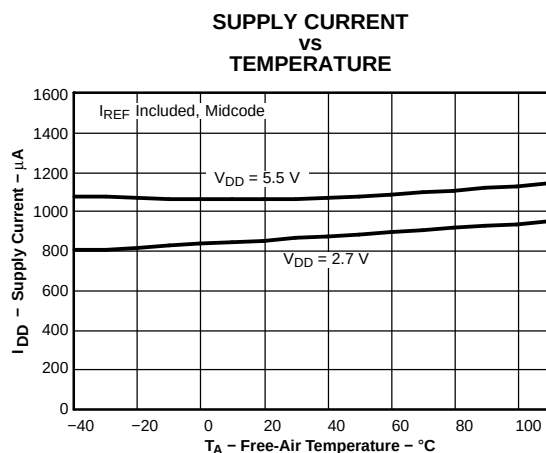


Figure 15.

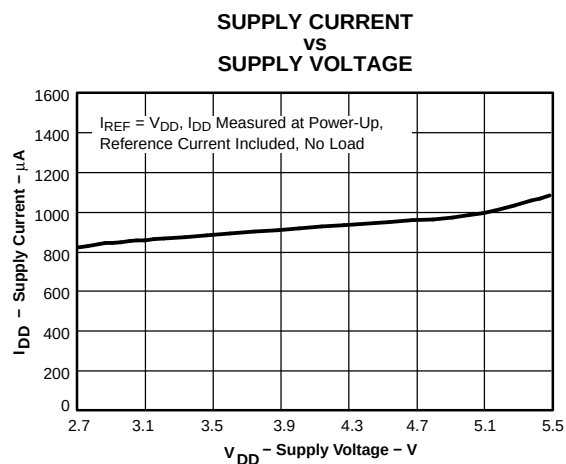


Figure 16.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

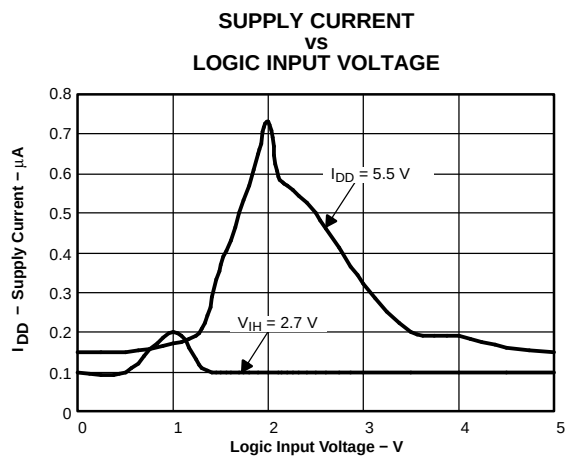


Figure 17.

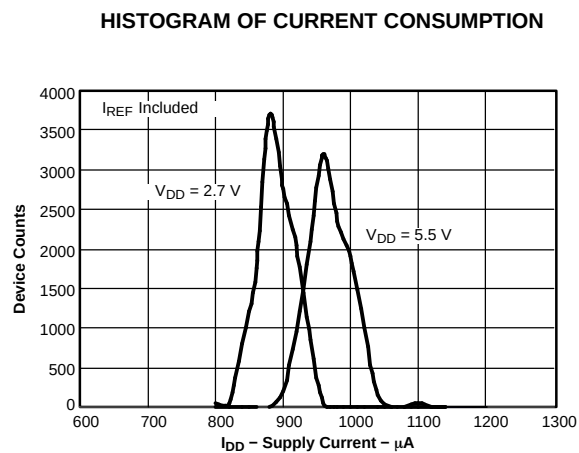


Figure 18.

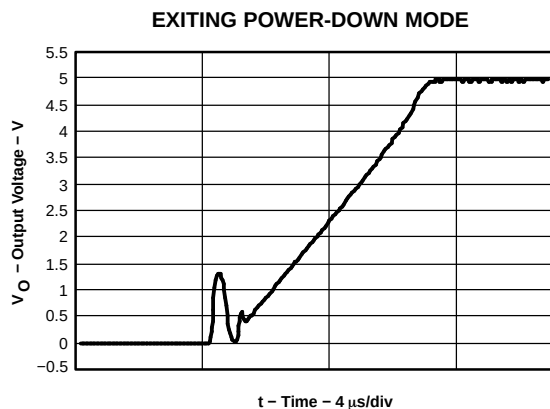


Figure 19.

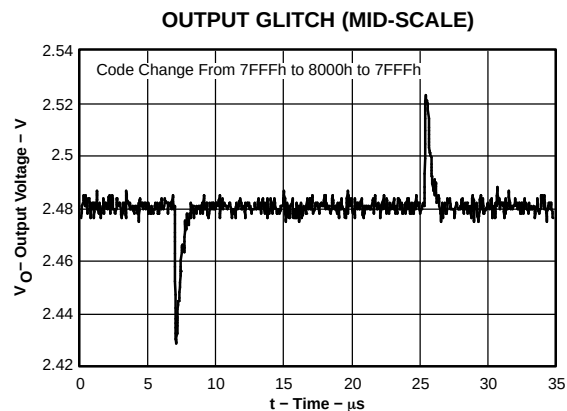


Figure 20.

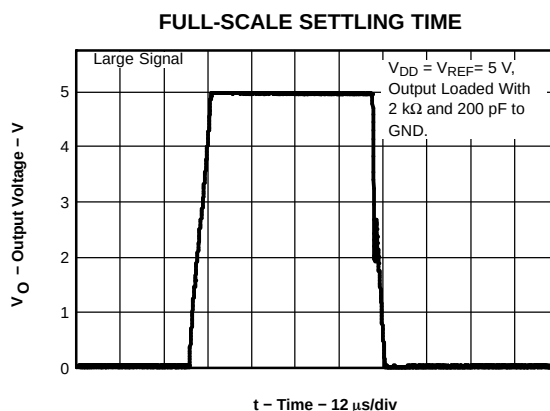


Figure 21.

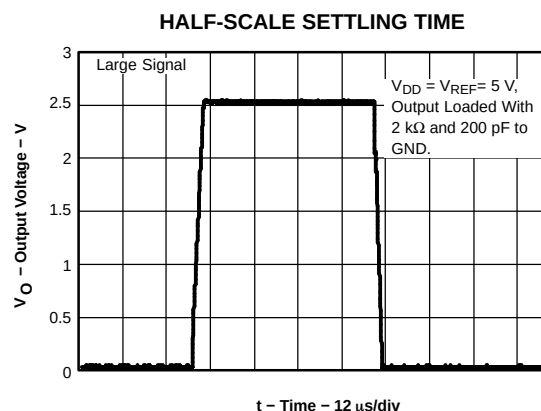


Figure 22.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

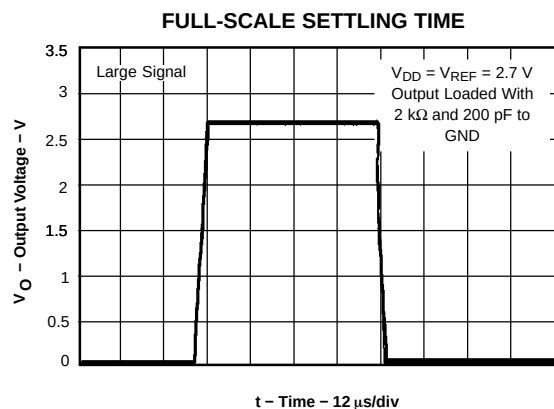


Figure 23.

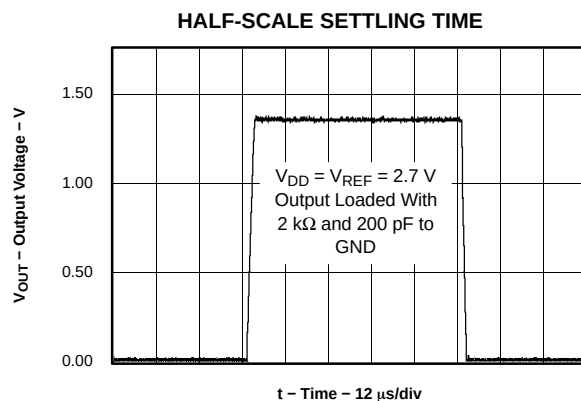


Figure 24.

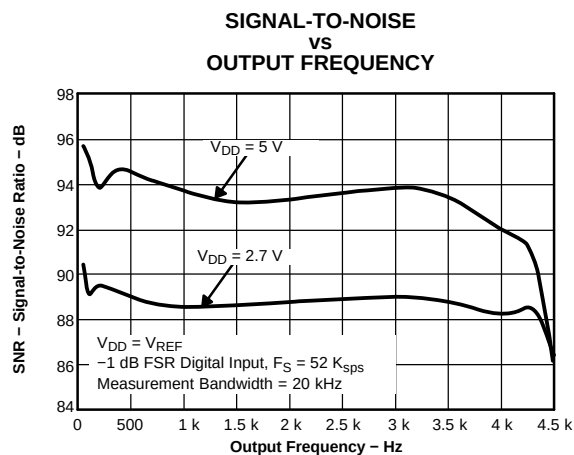


Figure 25.

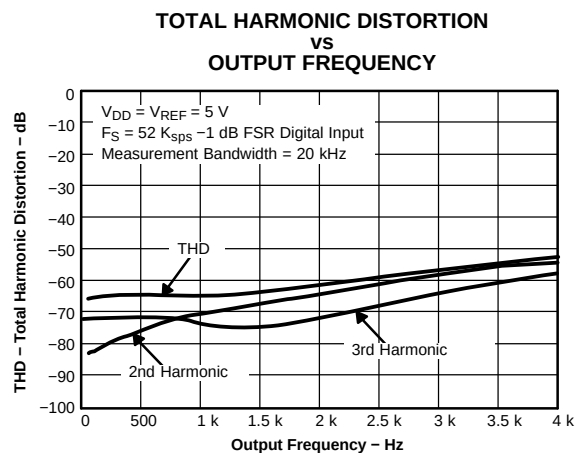


Figure 26.

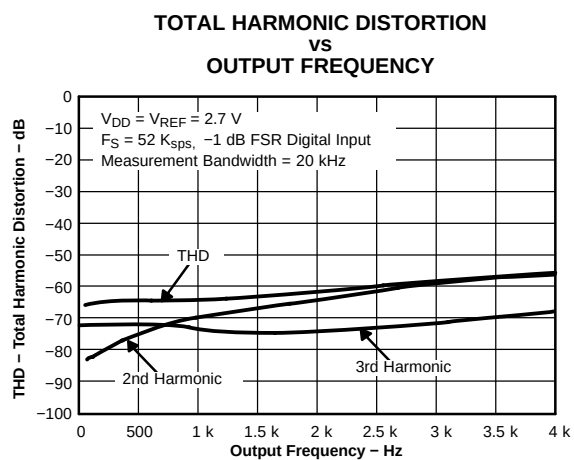


Figure 27.

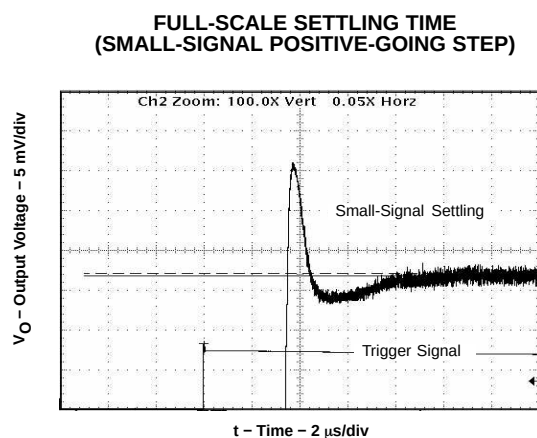


Figure 28.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

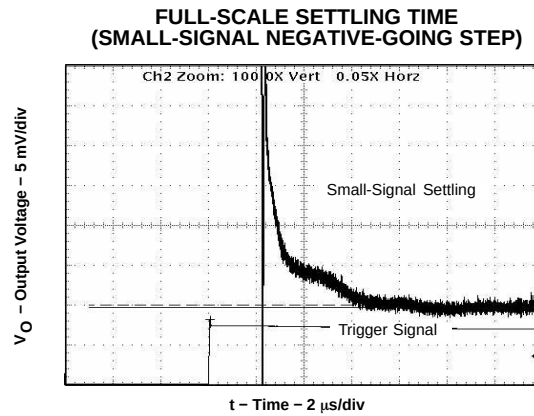


Figure 29.

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC8544 consists of four string DACs followed by an output buffer amplifier. Figure 30 shows a block diagram of the DAC architecture.

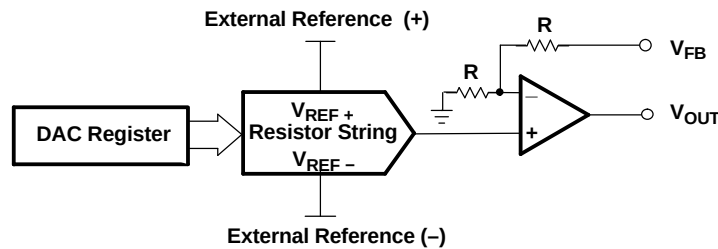


Figure 30. DAC8544 Architecture

The input coding to the DAC8544 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = 2 \times V_{REF-} + (V_{REF+} - V_{REF-}) \times \frac{D}{65536} \quad (1)$$

where

- D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 31. It is simply a divide-by-two resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off, to be fed into the output amplifier, by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is assured monotonic.

THEORY OF OPERATION (continued)

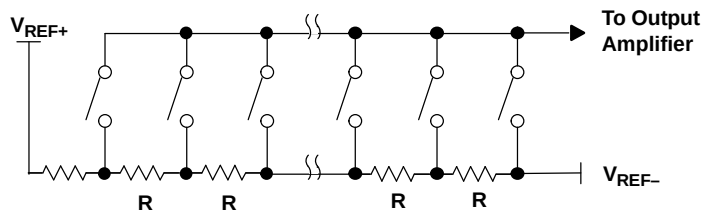


Figure 31. Resistor String

OUTPUT AMPLIFIER

The output buffer is capable of generating rail-to-rail voltages at its output, which gives an output range of 0 V to V_{REF+} . It is capable of driving a load of 2 k Ω in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/ μ s with a full-scale settling time of 10 μ s with the output loaded. The feedback and gain setting resistors of the amplifier are in the order of 50 k Ω . Their absolute value can be off significantly, but they are matched to within 0.1%.

The inverting input of the output amplifier is brought out to the V_{FB} pin, through the feedback resistor. This allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together at the load. Other signal conditioning circuitry may also be connected between these points for specific applications including current sourcing.

PARALLEL INTERFACE

The DAC8544 provides a 16-bit parallel interface and supports both writing to and reading from the DAC input register. (See the timing characteristics section for detailed information for a typical write or read operation.) In addition to the data, $\overline{CS}$, and R/W inputs, the DAC8544's interface also provides power down, LDAC, and reset control. Table 1 to Table 5 show the control signal actions and data format, respectively. These features are discussed in more detail in the remaining sections.

Table 1. DAC8544 CONTROL SIGNAL SUMMARY

$\overline{CS}$	R/W	LDAC	RST	$\overline{PD}$	ACTION
H	X	X	X	X	Device data I/O is disabled on the bus. ⁽¹⁾
↓	L	X	H,L	H	Write initiated, external data is latched when writing to the device.
↓	H	X	H,L	H	Read initiated, data from input register is presented to data bus.
X	X	↑	H,L	H	Data from input register is transferred to DAC register and V_{OUT} is updated.
X	X	X	↑	H	All DAC registers and voltage outputs (V_{OUT}) reset to min-scale. (If DAC is powered down during reset, DAC registers reset and outputs (V_{OUT}) settle to min-scale on power up.)
X	X	X	X	L	Power down device, V_{OUT} impedance equals high impedance

(1) Only disables 16-bit data I/O interface. Other control lines remain active.

LDAC FUNCTION

The DAC8544 is designed using a double-buffered architecture. A write operation (falling edge of $\overline{CS}$ while R/W is low) transfers data from the data input pins into the input register. The data is held in the input register until a rising-edge is detected on the LDAC input. This rising-edge signal transfers the data from the input registers to the DAC registers. On issuance of the rising LDAC edge, the output of the DAC8544 begins settling to the newly written data value presented to the DAC register. Data in the input register is not changed when an LDAC rising edge occurs.

Table 2. LDAC Function Section

A1	A0	CS	R/W	LDAC	ACTION
X	X	X	X	↑	All DAC registers are simultaneously loaded with the contents of their corresponding input registers and all DAC outputs also updated.

UPDATE SEQUENCE

For regular operation, $\overline{R/\overline{W}}$ pin should be kept low while $\overline{CS}$ is kept high. Then, the 16-bit digital data should be applied to the input bus. The channel selection should then be asserted by setting the A0 and A1 pins. Once the data is stable and the channels are selected the falling edge of $\overline{CS}$ enables the device and latches the data to the input register of the selected channel. After the data is latched to the input register, the rising edge of the LDAC signal updates all four channels simultaneously with existing data from their corresponding input register.

Table 3. Update Sequence Section

A1	A0	CS	R/W	LDAC	ACTION
0	0	↓	L	X	Latches external data into the DAC A input register.
0	1	↓	L	X	Latches external data into the DAC B input register.
1	0	↓	L	X	Latches external data into the DAC C input register.
1	1	↓	L	X	Latches external data into the DAC D input register.

READBACK

For read-back operation, the user first releases the 16-bit bus, while $\overline{CS}$ is high. Then, the DAC channel should be selected using the A0 and A1 pins. $\overline{R/\overline{W}}$ pin is then brought high to enable read-back operation. Following the falling edge of $\overline{CS}$, the data from the selected channel (buffer data) is output on the bus.

Table 4. Readback Section

A1	A0	CS	R/W	ACTION
0	0	↓	H	DAC A input register data is presented to the data bus.
0	1	↓	H	DAC B input register data is presented to the data bus.
1	0	↓	H	DAC C input register data is presented to the data bus.
1	1	↓	H	DAC D input register data is presented to the data bus.

RST

The RST input controls the reset of the DAC register and, consequently, the DAC output, but does not change the input register. The reset operation is edge-triggered by a low-to-high transition on the RST pin. Once a rising edge on RST is detected, the DAC output settles to the zero code. Application of a valid reset signal to the DAC does not overwrite existing data in the input register.

POWER-ON RESET

The DAC8544 contains a power-on reset circuit that controls the output voltage after power up. On power up, the DAC register (and DAC output) is set to zero (plus a small offset error produced by the output buffer). It remains at zero until a valid write sequence is made to the DAC, changing the DAC register data. This is useful in applications where it is important to know the state of the output of the DAC after power up. All digital inputs must be logic low until the digital and analog supplies are applied. Logic high voltages, applied to the input pins when power is not applied to IOV_{DD} and V_{DD} , may power the device through the ESD input structures causing undesired operation.

POWER-DOWN MODES

The DAC8544 uses two modes of operation. These modes are programmable via pin $\overline{PD}$.

Table 5 shows how the state of the pin correspond to the mode of operation of the DAC8544.

Table 5. Modes of Operation for the DAC8544

$\overline{PD}$	OPERATING MODE
High	Normal operation
Low	Power down, high impedance

When pin $\overline{\text{PD}}$ is high, the device works normally with its typical power consumption of 950 μA at $V_{\text{DD}} = 5\text{ V}$. However, when $\overline{\text{PD}}$ pin is in low state, the device is in power-down mode, the supply current falls to 200 nA at $V_{\text{DD}} = 5\text{ V}$ (50 nA at $V_{\text{DD}} = 3\text{ V}$), and the output is open circuit (high impedance).

All analog circuitry is shut down when a power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down mode. This allows the DAC output voltage to return to the previous level when power up resumes. The delay time required to exit power-down is typically 2.5 μs for $V_{\text{DD}} = 5\text{ V}$, and 5 μs for $V_{\text{DD}} = 3\text{ V}$. (See the typical characteristics section for additional information.)

VOLTAGE REFERENCE INPUTS

Two voltage inputs provide the reference set points for the DAC architecture. These are $V_{\text{REF}+}$ and $V_{\text{REF}-}$. For typical rail-to-rail operation, $V_{\text{REF}+}$ should be equivalent to V_{DD} and $V_{\text{REF}-}$ tied to GND. The output voltage is given by:

$$V_{\text{OUT}} = 2 \times V_{\text{REF}-} + (V_{\text{REF}+} - V_{\text{REF}-}) \times \frac{D}{65536} \quad (2)$$

The use of the $V_{\text{REF}-}$ input allows minor adjustments to be made to the offset of the DAC output by applying a small voltage to the $V_{\text{REF}-}$ input. A low output impedance source is needed, so that the accuracy of the DAC over its operating range is not affected.

ANALOG AND DIGITAL SUPPLIES

The analog supply (V_{DD}) powers the output buffer and DAC while the digital supply (IOV_{DD}) powers the digital interface. V_{DD} can operate from 2.7 V to 5.5 V while IOV_{DD} can independently function from 1.8 V to 5.5 V. IOV_{DD} determines the interface logic level. See the device specification table for details.

EXTERNAL REFERENCE VOLTAGE

To take advantage of the absolute accuracy of DAC8544, a high-performance reference voltage generator must be used. DAC8544 has a typical absolute accuracy error of 2 millivolts, and a typical voltage drift of 3 ppm/ $^{\circ}\text{C}$. This level of performance requires an accurate external reference voltage generator with good temperature drift characteristics. Accuracy, drift, supply voltage, power consumption, and cost are important factors in choosing a voltage reference. TI's REF02 is recommended. TI's REF3140 and REF3040 are small and low-cost alternatives.

FEEDBACK PINS

For regular operation, the feedback pins (V_{FBA} through V_{FBD}) must be tied to their corresponding output pins (V_{OUTA} through V_{OUTD}) at the load. For higher current applications sensitive to gain error, the feedback pin should be routed to the target node, to sense the node voltage accurately (DAC8544 gain error is typically low, around 1 mV).

HOST PROCESSOR INTERFACING

DAC8544 to MSP430 Microcontroller

Figure 32 shows a typical parallel interface connection between the DAC8544 and a MSP430 microcontroller. The setup for the interface shown uses ports 4 and 5 of the MSP430 to send or receive the 16-bit data while bits 0-7 of port 2 provides the control signals for the DAC. When data is to be transmitted to the DAC8544, the data is made available to the DAC via P4 and P5, and P2.1 is taken low. The MSP430 then toggles P2.0 from high-to-low and back to high, transferring the 16-bit data to the DAC. This data is loaded into the DAC register by applying a rising edge to P2.4. The remaining five I/O signals of P2 shown in the figure control the reset, power-down, and data format functions of the DAC. Depending on the specific requirements of a given application, these pins may be tied to IOGND or IOV_{DD} , enabling the desired mode of operation.

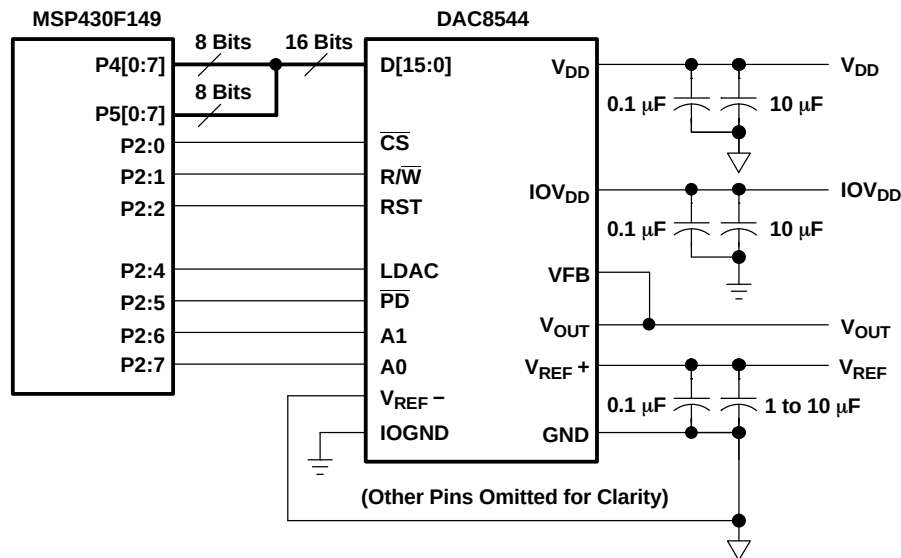


Figure 32. DAC8544 to MSP430 Microcontroller

DAC8544 to TMS320C5402 DSP

Figure 33 shows the connections between the DAC8544 and the TMS320C5402 digital signal processor. Data is provided via the parallel data bus of the DSP while the DAC CS control input is derived from the decoded I/O strobe signal. The IOSTRB in addition to the R/W and XF(I/O) signals control the data transmission to and from the DAC as well as the LDAC control. With additional decoding, multiple DAC8544s can be connected to the same parallel data bus of the DSP.

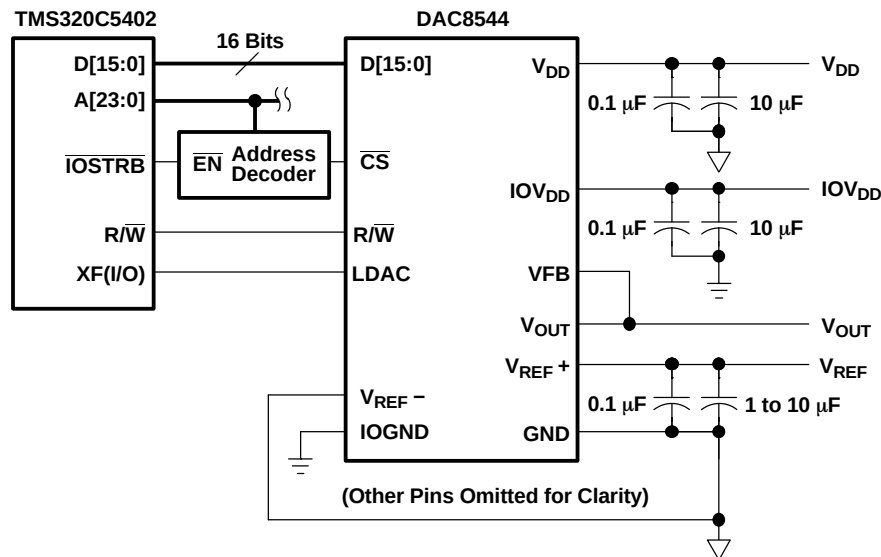


Figure 33. DAC8544 to TMS320 DSP

BIPOLAR OPERATION USING THE DAC8544

The DAC8544 has been designed for single-supply operation but a bipolar output range is also possible using the circuit shown in Figure 34. The circuit allows the DAC8544 to achieve an analog output range of ± 5 V. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

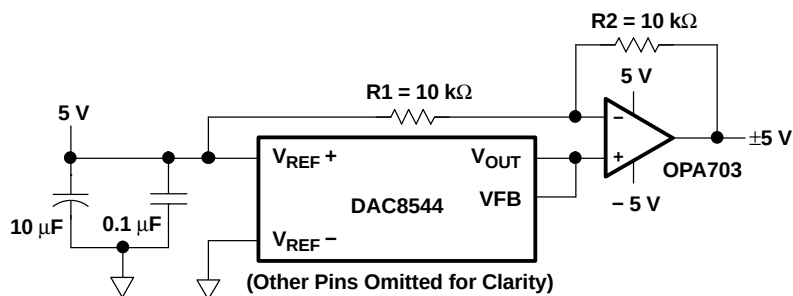


Figure 34. Bipolar Operation With the DAC8544

With $V_{REF+} = 5V$, $R1 = R2 = 10k\Omega$:

$$V_{OUT} = \left(\frac{10 \times D}{65536} \right) - 5V$$

(3)

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The following measures should be taken to assure optimum performance of the DAC8544. The DAC8544 offers dual-supply operation, as it can often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more important it becomes to separate the analog and digital ground and supply planes at the DAC.

Because the DAC8544 has both analog and digital ground pins, return currents can be better controlled and have less effect on the DAC output error. Ideally, GND would be connected directly to an analog ground plane and GND to the digital ground plane. The analog ground plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system. The power applied to V_{DD} and V_{REF+} (this also applies to V_{REF-} if not tied to GND) should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1- μ F to 10- μ F and 0.1- μ F bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100- μ F electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially lowpass-filter the V_{DD} supply, removing the high-frequency noise.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8544IPFB	Active	Production	TQFP (PFB) 48	250 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8544I
DAC8544IPFB.B	Active	Production	TQFP (PFB) 48	250 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8544I
DAC8544IPFBG4	Active	Production	TQFP (PFB) 48	250 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8544I
DAC8544IPFBG4.B	Active	Production	TQFP (PFB) 48	250 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8544I
DAC8544IPFBR	Active	Production	TQFP (PFB) 48	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8544I
DAC8544IPFBR.B	Active	Production	TQFP (PFB) 48	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8544I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

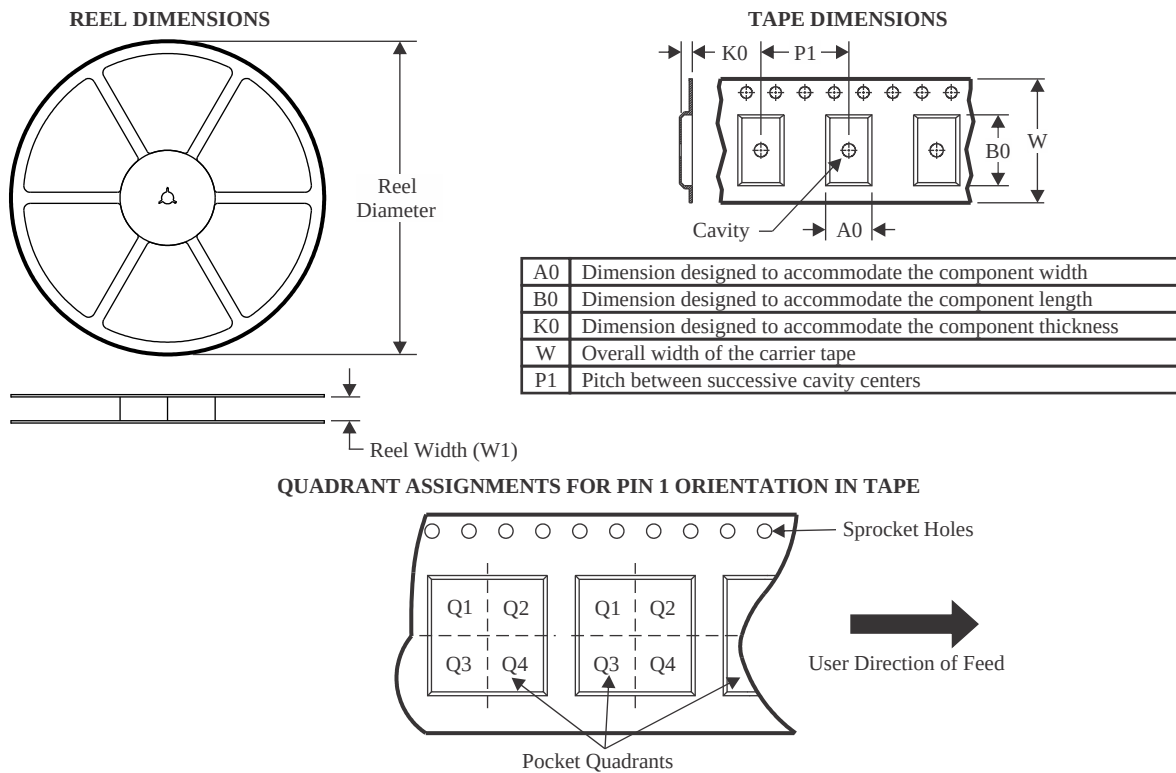
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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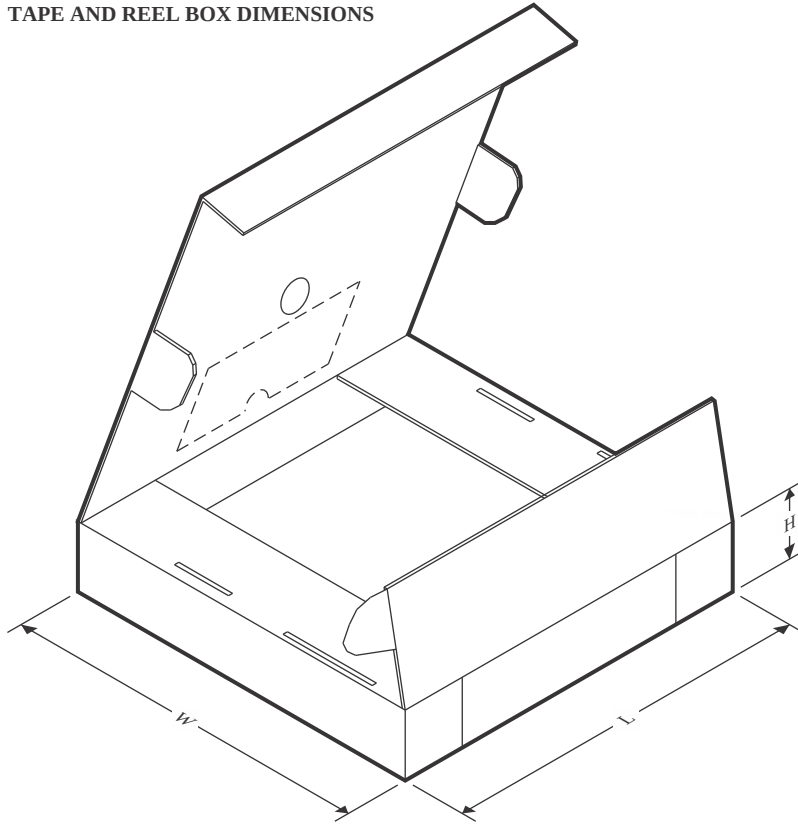
TAPE AND REEL INFORMATION



*All dimensions are nominal

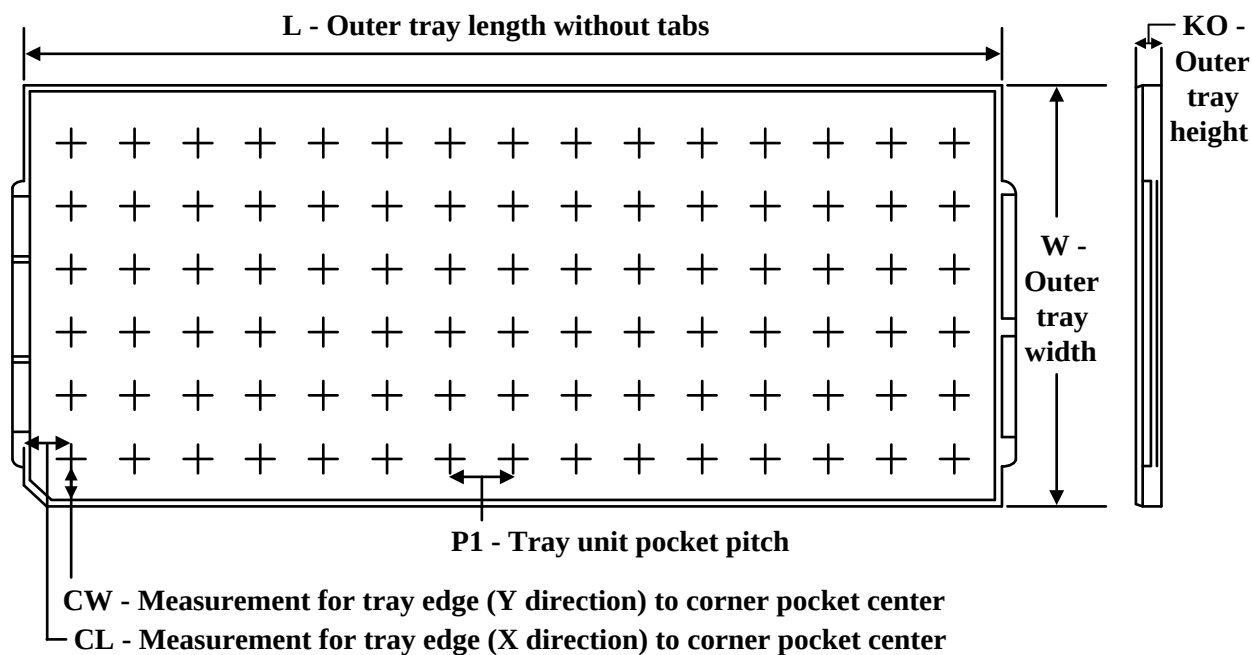
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8544IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8544IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0

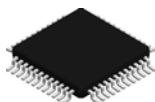
TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
DAC8544IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC8544IPFB.B	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC8544IPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC8544IPFBG4.B	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

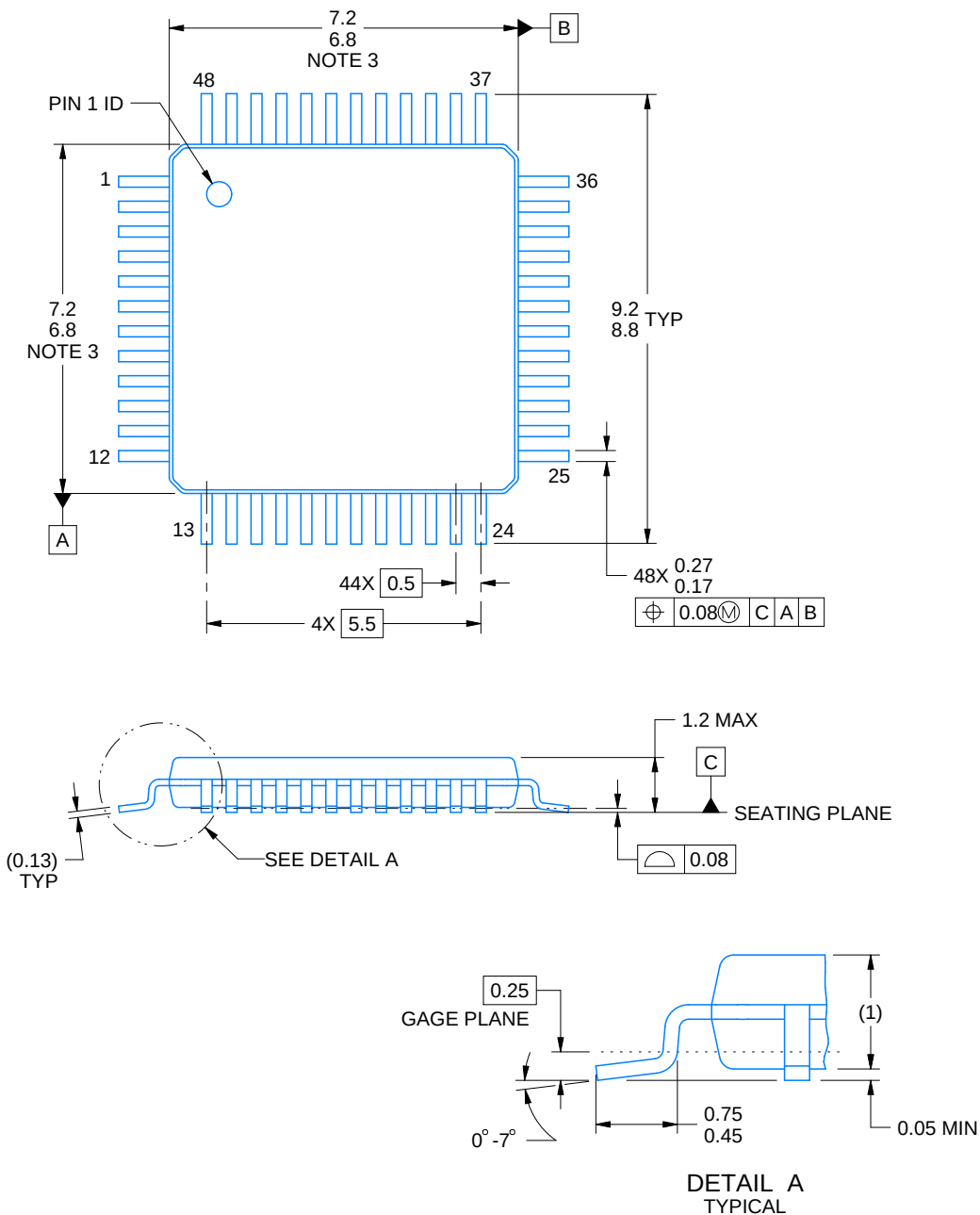
PFB0048A



PACKAGE OUTLINE

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

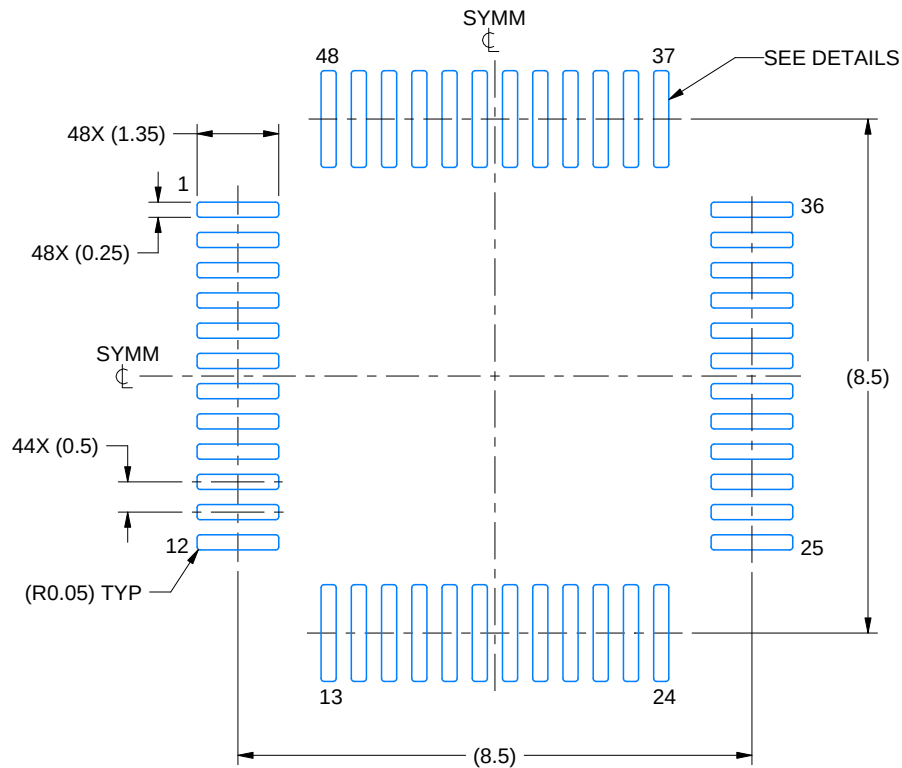


EXAMPLE BOARD LAYOUT

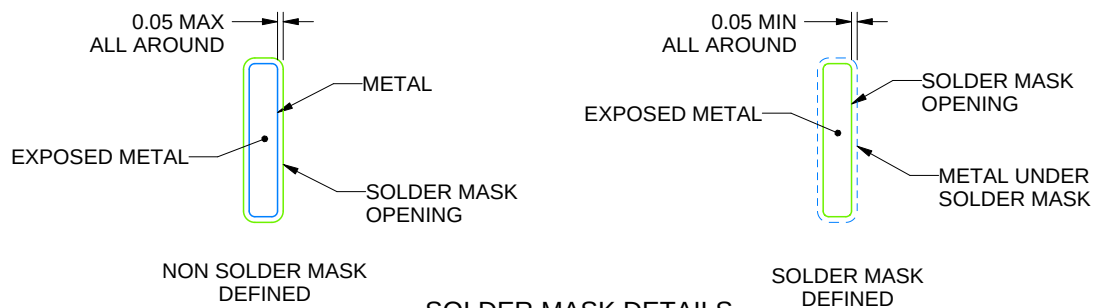
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

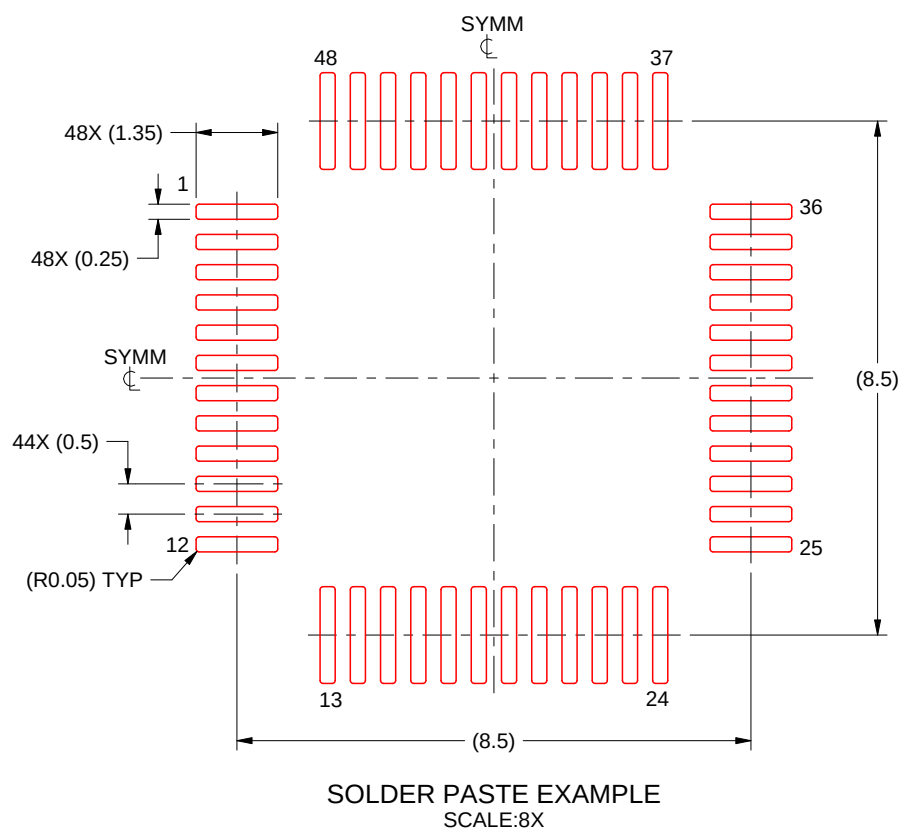
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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