

# MPC8569E-MDS-PB

This document describes the MPC8569E-MDS-PB and its related hardware kit. The MPC8569E-MDS-PB getting started procedure explains and verifies the board's basic operation in a step-by-step format.

Settings for switches, jumpers, LEDs, and push buttons are shown, and there are instructions for connecting peripheral devices.

The MPC8569E-MDS-PB functions with an integrated development environment (IDE), such as Freescale's *CodeWarrior™*, but instructions for working with the IDE are beyond the scope of this document.

## NOTE!

The terms PEX and PCIe are interchangeable. However, as the modules are stamped "PEX", the document uses this term.

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# 1 Revisions Table

Table 1. Revisions Table

| Date         | Rev. | Author         | Tech Editor | Description                                                              |
|--------------|------|----------------|-------------|--------------------------------------------------------------------------|
| 19 Jan 2009  | 1.0  | Vladimir Yukht | Hadas Khen  | HWGS Rev. 1.0                                                            |
| 12 Mar 2009  | 2.0  | Vladimir Yukht | Hadas Khen  | BCSR changes.                                                            |
| 31 Mar 2009  | 2.1  | Vladimir Yukht | Hadas Khen  | RCW changes                                                              |
| 5 May 2009   | 2.2  | Vladimir Yukht | Hadas Khen  | BCSR, terminology, reference document changes, and new photos (Bootwiz). |
| 21 May 2009  | 3.0  | Vladimir Yukht | Hadas Khen  | Revised content                                                          |
| 22 June 2009 | 3.1  | Vladimir Yukht | Hadas Khen  | BCSR changes                                                             |

# 2 Definitions, Acronyms, and Abbreviations

Table 2. Definitions, Acronyms, and Abbreviations

| Usage    | Description                                      |
|----------|--------------------------------------------------|
| ADDR     | Address                                          |
| ADS      | Application Development System                   |
| BCSR     | Board Control and Status Register                |
| BVDD     | Local Bus Volt Direct Current                    |
| CCB      | Platform Clock                                   |
| CKE      | DDR Clock Enable                                 |
| CLKIN    | Clock Input; interchangeable with SYSCLK         |
| CLKOUT   | Clock Output                                     |
| CNTR ISP | Control PLD Integrated SW Programming            |
| COP      | Common On-Chip Processor                         |
| CPU      | Central Processing Unit                          |
| CS       | Component Side                                   |
| DDR      | Double Data Rate                                 |
| DIP      | Dual-in-Line Package (switches)                  |
| DUART    | Dual Universal Asynchronous Receiver/Transmitter |
| e500     | CPU Core Name                                    |
| ECC      | Error Detection and Correction                   |
| EEPROM   | Electrical Erasable Programmable Memory          |

**Table 2. Definitions, Acronyms, and Abbreviations**

| Usage            | Description                                               |
|------------------|-----------------------------------------------------------|
| eLBC             | Enhanced Local Bus Controller                             |
| EN               | Enable                                                    |
| EP               | End Point                                                 |
| ETH              | Ethernet                                                  |
| FCM              | NAND Flash Control Machine                                |
| FSL              | Freescale Semiconductor                                   |
| GETH             | Gigabit Ethernet (also GbE)                               |
| GPCM             | General Purpose Chip-Select Machine                       |
| Host             | MPC8569E                                                  |
| HRESET           | Hard Reset                                                |
| HW               | Hardware                                                  |
| I <sup>2</sup> C | Inter-Integrated Circuit multi-master serial computer bus |
| IDE              | Integrated Development Environment                        |
| IO               | Input/Output                                              |
| IRSENSE          | Service Voltage Drop Testing                              |
| JTAG             | Joint Test Access Group (IEEE® Std. 1149.1™)              |
| LED              | Light-emitting Diode                                      |
| LYNX             | Internal terminology; interchangeable with SerDes         |
| LVDD             | QUICC Engine Block UCC1-UCC4 Voltage                      |
| MCK(E)           | DDR Master Clock                                          |
| MDIC             | DDR Memory Driver Impedance Calibration                   |
| MEMC             | Memory Controller                                         |
| MMC              | Multi Media Card                                          |
| MPI              | Metallized Particle Interconnect Matrix                   |
| NAND             | FLASH Memory                                              |
| NMI              | Non-Maskable Interrupt                                    |
| nMVRST           | Marvell PHY Reset Signal                                  |
| NOR              | Flash Memory                                              |
| PB               | MPC8569E-MDS Processor Board                              |
| PCI              | Peripheral Components Interconnect                        |
| PCIe             | PCI Express = PCIe = PEX                                  |

**Table 2. Definitions, Acronyms, and Abbreviations**

| Usage       | Description                                                                                                                                                       |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PEX         | PCI Express = PEX = PCIe                                                                                                                                          |
| PHY         | Physical Layer                                                                                                                                                    |
| PIB         | Platform I/O Board                                                                                                                                                |
| PLD         | Programmable Logic Device                                                                                                                                         |
| PLL         | Phased Lock Loop                                                                                                                                                  |
| POST FA_AND | Service Failure Analysis                                                                                                                                          |
| PRESET      | Power-on-Reset                                                                                                                                                    |
| PS          | Print Side                                                                                                                                                        |
| PS ISP      | PS Control PLD Integrated SW Programming                                                                                                                          |
| PTP         | Precision Time Protocol                                                                                                                                           |
| QE          | Quick Engine                                                                                                                                                      |
| RC          | Root Complex                                                                                                                                                      |
| RCW         | Reset Configuration Word                                                                                                                                          |
| REG CFG     | Configuration Register                                                                                                                                            |
| RGMII       | Reduced General Media Independent Interface                                                                                                                       |
| RMII        | Reduced Media Independent Interface                                                                                                                               |
| ROM         | Read Only Memory                                                                                                                                                  |
| RTC         | Real Time Clock                                                                                                                                                   |
| SD          | Secure Digital Card                                                                                                                                               |
| SDHC        | Secure Digital High Capacity Card                                                                                                                                 |
| SerDes      | <ul style="list-style-type: none"> <li>• Serializer/Deserializer</li> <li>• High Speed Serial Communication Lines; e.g., PEX (PCIe), SRIO, SGMII, etc.</li> </ul> |
| SGMII       | Serial Gigabit Media Independent Interface                                                                                                                        |
| SHMOO       | Graphical representation of selected test parameters in an electronic circuit.                                                                                    |
| SMII        | Serial Media Independent Interface                                                                                                                                |
| SODIMM      | Mini DIMM Form Factor                                                                                                                                             |
| SRESET      | Soft Reset                                                                                                                                                        |
| SRIO        | Serial RapidIO                                                                                                                                                    |
| SW          | Switch                                                                                                                                                            |
| SYSCLK      | System Clock; interchangeable with CLKIN                                                                                                                          |

**Table 2. Definitions, Acronyms, and Abbreviations**

| Usage    | Description                                 |
|----------|---------------------------------------------|
| TAP      | e.g., USB or ETH TAP                        |
| TDM      | Time Division Multiplexing                  |
| TRIG OUT | Signal Trigger_Out                          |
| UART     | Universal Asynchronous Receiver/Transmitter |
| UCC      | Universal Communication Controller          |
| UEM      | Universal Ethernet Module                   |
| UPC      | Universal Programmable Controller           |
| USB      | Universal Serial Bus                        |
| V        | Volt                                        |
| VDD      | Common Power Supply Terminals               |

### 3 Related Reading

The below noted documents are available in the Freescale website to those with NDA Agreement access; the website is found at <http://www.freescale.com/>.

**Table 3. Related Reading**

| Document                                                              | Description                                                                                                                                                                                |
|-----------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CodeWarrior™ Kit Configuration Guide                                  | <ul style="list-style-type: none"> <li>Complete HW setup explanation.</li> <li>Kit Configuration Guide explains how to set up and use each SW component in the development kit.</li> </ul> |
| MPC8569E PowerQUICC™ III Integrated Processor Hardware Specifications | MPC8569EEC                                                                                                                                                                                 |
| MPC8569E PowerQUICC™ III Integrated Processor Reference Manual        | MPC8569ERM                                                                                                                                                                                 |

## 4 Hardware Kit Content

### NOTE!

The terms PEX and PCIe are interchangeable. However, as the modules are stamped “PEX”, the document uses this term.

| Hardware Kit Contents                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Figure 1. HW Kit Inventory |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|
| <p><b>Processor Board and Modules</b></p> <ol style="list-style-type: none"> <li>1. MPC8569E-MDS-PB (1)</li> <li>2. UEM (2)</li> <li>3. SRIOx1 (2) and plastic screws (2)</li> <li>4. PEXx2 (1) and plastic screw (1)</li> <li>5. SRIO_LOOPBACK CARD (2)</li> <li>6. Bootwiz (1)</li> </ol> <p><b>Cables</b></p> <ol style="list-style-type: none"> <li>7. RS-232 standard serial cable with two 9-pin connectors (2)</li> <li>8. FSL adaptor cable with one 10-pin and two RS-232 connectors (1)</li> <li>9. ETH cables (4) with RJ45 connectors</li> <li>10. ETH loop-back cables (4)</li> </ol> <p><b>Power Supply and USB TAP</b></p> <ol style="list-style-type: none"> <li>11. AC/DC 5V/8A power supply</li> <li>12. CodeWarrior USB TAP</li> </ol> <p><b>Miscellaneous</b></p> <ol style="list-style-type: none"> <li>13. Allen key</li> <li>14. UEM plastic guide pins (6)</li> <li>15. Auxiliary UTAP to CNTR-ISP connector (1)</li> </ol> <p><b>Printed Matter (not shown in Figure 1)</b></p> <ul style="list-style-type: none"> <li>• MPC8569E-MDS-PB HW Getting Started</li> <li>• Freescale Warranty Card: 920-75133</li> <li>• Safety Notice: 926-75254</li> <li>• Contact Information Sheet: 920-90570-00</li> </ul> |                            |

## 5 MPC8569E-MDS-PB Schematic CS and PS Views

Figure 2. MPC8569E-MDS-PB Component Side (CS) View

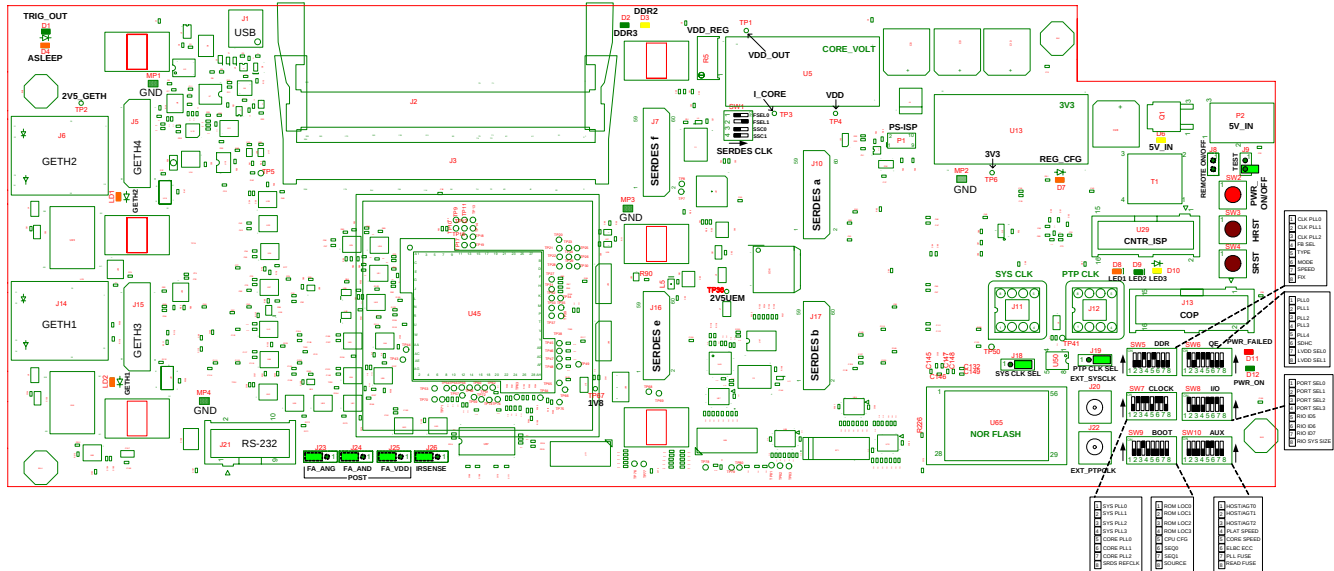
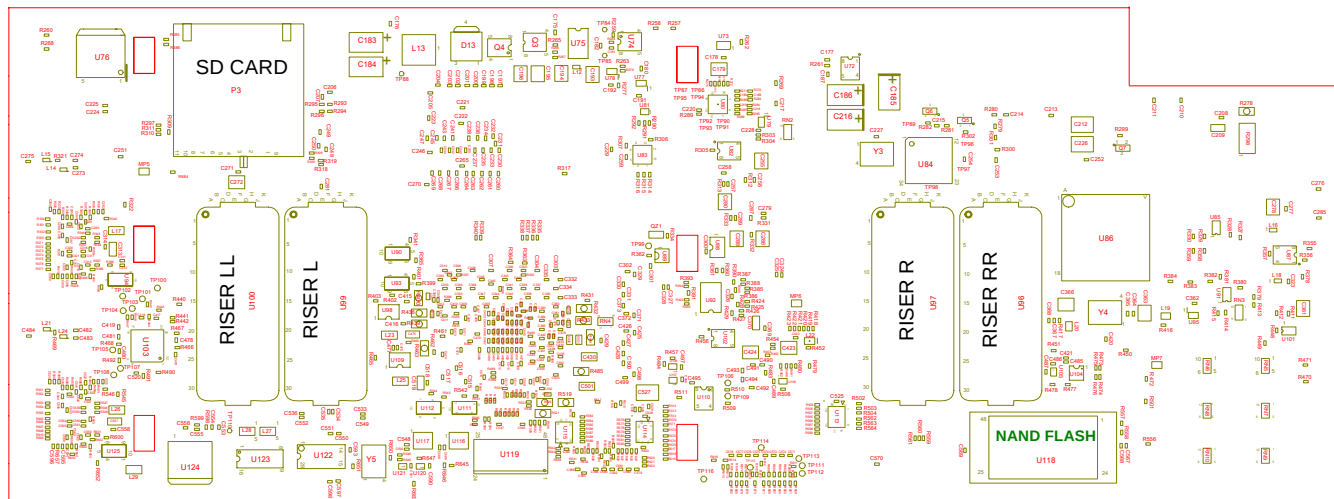


Figure 3. MPC8569E-MDS-PB Print Side (PS) View



## 6 Switch Default Settings

The MPC8569E-MDS-PB has dual-in-line package (DIP) switches; see Figure 5.

Default DIP switch positions establish MPC8569E-MDS-PB clock modes; see Table 4.

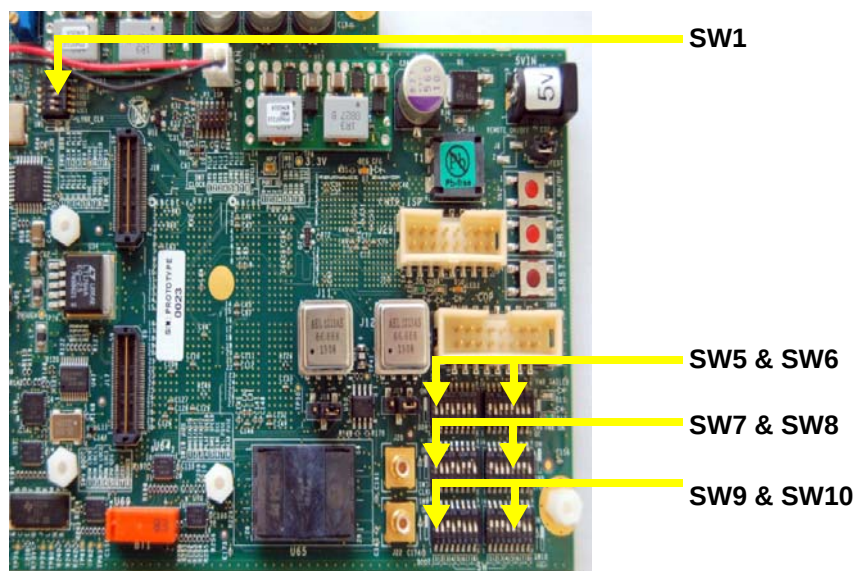
### NOTE!

Ensure DIP switches are set according to default values.

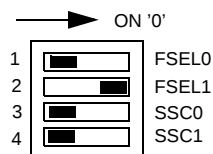
**Table 4. MPC8569E-MDS-PB Default Configurations**

| Mode                    | Value          |
|-------------------------|----------------|
| BVDD Voltage            | 3.3V only      |
| CCB Clock               | 533MHz         |
| SYSCLK (CLKIN)          | 66.67 MHz      |
| Core Clock              | 1067MHz MHz    |
| DDR CLK                 | 400 MHz (DDR3) |
| LVDD1 and LVDD2 Voltage | 2.5V           |
| PTP CLK                 | 66.67 MHz      |
| QE Clock                | 533MHz         |
| RTC CLK                 | 66.67 MHz      |
| SerDes REF CLK          | 100 MHz        |
| SRIO                    | 2.5 GBaud      |
| VDD Voltage             | 1.1V           |

**Figure 4. MPC8569E-MDS-PB DIP-Switch Locations**



## SW1 Configuration: SerDes CLK

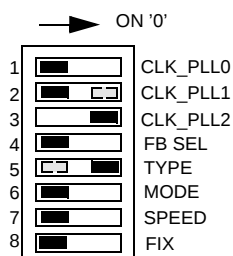


## SW1.1-SW1.4: SerDes Reference Clock

- Sets reference clock value for MPC8569 SerDes module.
- Sets reference clock values for external PEX/SRIO/SGMII interfaces.
- (Default) 100 MHz and no spread.

| FSEL0          | FSEL1         | Q0:Q1          | SSC0           | SSC1           | SPREAD%          |
|----------------|---------------|----------------|----------------|----------------|------------------|
| 0 (ON)         | 0 (ON)        | 25 MHz         | 0 (ON)         | 0 (ON)         | CENTER +/- 0.25  |
| <b>1 (OFF)</b> | <b>0 (ON)</b> | <b>100 MHz</b> | 1 (OFF)        | 0 (ON)         | DOWN -0.5        |
| 0 (ON)         | 1 (OFF)       | 125 MHz        | 0 (ON)         | 1 (OFF)        | DOWN -0.75       |
| 1 (OFF)        | 1 (OFF)       | 25 OMHz        | <b>1 (OFF)</b> | <b>1 (OFF)</b> | <b>NO SPREAD</b> |

## SW5 Configuration: DDR3



## SW5.1- SW5.3: DDR Complex Clock PLL Ratio

- Establish clock ratio between SYSCLK input and DDR complex clock.

| Value (Binary)                                | DDR Complex Clock:<br>SYSCLK Ratio |
|-----------------------------------------------|------------------------------------|
| 000                                           | 3:1                                |
| 001                                           | 4:1                                |
| 010                                           | 5:1                                |
| 011                                           | 6:1                                |
| 100                                           | 8:1                                |
| 101                                           | 10:1                               |
| 110                                           | (Default) 12:1                     |
| 111                                           | Synchronous Mode*                  |
| *Synchronous mode: DDR data rate = CCB clock. |                                    |

## NOTE!

Switch positions related to DDR2 usage are marked with the symbol:



## SW5.4: DDR PLL Feedback Select

- '0': Local/Shorter feedback path selected
- '1': (Default) Longer feedback path selected (matches insertion delay of DDR, QE and Platform)

## SW5.5: DDR SDRAM Type

- '0': (Default) DDR3, 1.5V, CKE low at reset.
- '1': DDR2, 1.8V, CKE low at reset.

## SW5.6: DRAM Mode

- '0': Primary and secondary DDR is enabled (32-bit width data bus).
- '1': (Default) Primary DDR is enabled (64-bit width data bus); secondary DDR is disabled.

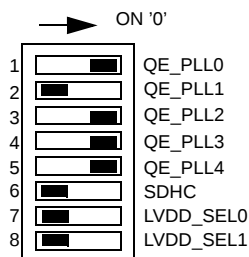
## SW5.7: DDR Speed

- '1': (Default) DDR clock frequency < 500MHz.
- '0': DDR clock frequency > or = to 500MHz.

## SW5.8: Disables DDR2 Phase Reset Logic

- '0': DDR controller disables MCKE at reset; a few cycles later MCK is disabled.
- '1': (Default) At reset, DDR controller simultaneously disables MCK and MCKE.

## SW6 Configuration: QE



### SW6.1-SW6.5: QUICC Engine PLL Configuration

- QUICC Engine Clock: defined by a multiplier & divisor applied to the SYSCLK input signal:  

$$\text{QUICC Engine clock} = \text{SYSCLK} * \text{cfg\_qe\_pll}[0:4]$$

| Value (Binary)*                       | Multiplier  |
|---------------------------------------|-------------|
| 0_0000                                | 16          |
| 0_0010                                | 2           |
| 0_0011                                | 3           |
| 0_0100                                | 4           |
| 0_0101                                | 5           |
| 0_0110                                | 6           |
| 0_0111                                | 7           |
| 0_1000                                | (Default) 8 |
| 0_1001                                | 9           |
| 0_1010                                | 10          |
| *All other combinations are reserved. |             |

### SW6.6: SDHC Card Detect Polarity Select

- '0': SDHC card-detect polarity is inverted.
- '1': (Default) SDHC card-detect polarity isn't inverted.

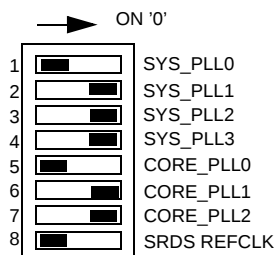
### SW6.7: QE UCC1 and UCC3 Voltage Select

- '0': QUICC Engine UCC1&3 GB Ethernet interface operates at 3.3V.
- '1': (Default) QUICC Engine UCC1&3 GB Ethernet interface operates at 2.5V.

### SW6.8: QE UCC2 and UCC4 Voltage Select

- '0': QUICC Engine UCC2&4 GB Ethernet interface operates at 3.3V.
- '1': (Default) QUICC Engine UCC2&4 GB Ethernet interface operates at 2.5V.

## SW7 Configuration: CLOCK



### SW7.1-SW7.4: CCB Clock PLL Ratio

- System PLL inputs establish the clock ratio between SYSCLK input and the Platform Clock (CCB) used by MPC8569E.

| Value (Binary) | CCB Clock:<br>SYSCLK Ratio |
|----------------|----------------------------|
| 0000           | Reserved                   |
| 0001           | Reserved                   |
| 0010           | 2:1                        |
| 0011           | 3:1                        |
| 0100           | 4:1                        |
| 0101           | 5:1                        |
| 0110           | 6:1                        |
| 0111           | 7:1                        |
| 1000           | (Default) 8:1              |
| 1001           | Reserved                   |
| 1010           | Reserved                   |
| 1011           | Reserved                   |
| 1100           | Reserved                   |
| 1101           | Reserved                   |
| 1110           | Reserved                   |
| 1111           | Reserved                   |

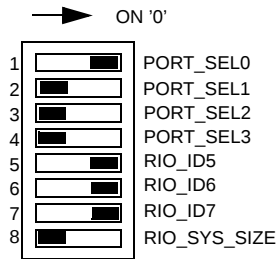
### SW7.5-SW7.7: e500 Core PLL Ratios

- Establish ratio between e500 core and e500 core complex bus (CCB) clocks.

| Value (Binary) | e500 Core:<br>CCB Clock Ratio |
|----------------|-------------------------------|
| 000            | 4:1                           |
| 001            | 9:2 (4.5:1)                   |
| 010            | 1:1                           |
| 011            | 3:2 (1.5:1)                   |
| 100            | (Default) 2:1                 |
| 101            | 5:2 (2.5:1)                   |
| 110            | 3:1                           |
| 111            | 7:2 (3.5:1)                   |

### SW7.8: SerDes Reference Clock Configuration

- '0': SerDes expects a 125 MHz reference clock frequency.
- '1': (Default) SerDes expects a 100 MHz reference clock frequency.

**SW8 Configuration: I/O****NOTE!**

100 MHz clock reference (set `cfg_srds_refclk` to 1).

125 MHz clock reference (set `cfg_srds_refclk` to 0).

**SW8.1-SW8.4: I/O Port Selection**

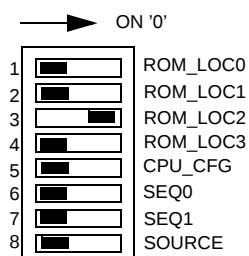
| Value (Binary) | Description                                                                                                                             | SerDes Reference Clock Speed |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| 0000           | - PCI Express x1 (2.5 Gbps), Lane A                                                                                                     | 100 MHz                      |
| 0001           | - SRIO1 1x (2.5 Gbps), Lane A<br>- SRIO2 1x (2.5 Gbps), Lane B<br>- SGMII x2 (1.25 Gbps; half-speed), Lanes E–F                         | 100 MHz                      |
| 0010           | - SRIO1 1x (2.5 Gbps; half-speed), Lane A<br>- SRIO2 1x (2.5 Gbps; half-speed), Lane B<br>- SGMII x2 (1.25 Gbps; half-speed), Lanes E–F | 100 MHz                      |
| 0011           | - SRIO1 1x (3.125 Gbps), Lane A<br>- SRIO2 1x (3.125 Gbps), Lane B                                                                      | 125 MHz                      |
| 0100           | - PCI Express x1 (2.5 Gbps), Lane A<br>- SGMII x2 (1.25 Gbps; half-speed), Lanes E–F                                                    | 100 MHz                      |
| 0101           | - PCI Express x2 (2.5 Gbps), Lanes A–B<br>- SGMII x2 (1.25 Gbps; half-speed), Lanes E–F                                                 | 100 MHz                      |
| 0110           | - PCI Express x1 (2.5 Gbps), Lane A<br>- SRIO1 1x (2.5 Gbps), Lane E<br>- SRIO2 1x (2.5 Gbps), Lane F                                   | 100 MHz                      |
| 0111 (Default) | - PCI Express x2 (2.5 Gbps), Lanes A–B<br>- SRIO1 1x (2.5 Gbps), Lane E<br>- SRIO2 1x (2.5 Gbps), Lane F                                | 100 MHz                      |
| 1000           | - PCI Express x2 (2.5 Gbps), Lanes A–B<br>- SRIO1 1x (2.5 Gbps—half speed), Lane E<br>- SRIO2 1x (2.5 Gbps—half speed), Lane F          | 100 MHz                      |
| 1001           | - SRIO1 4x (1.25 Gbps; half-speed), Lanes A–B, E–F                                                                                      | 100 MHz                      |
| 1010           | - SRIO1 4x (2.5 Gbps), Lanes A–B, E–F                                                                                                   | 100 MHz                      |
| 1011           | - SRIO1 4x (3.125 Gbps), Lanes A–B, E–F                                                                                                 | 125 MHz                      |
| 1100           | - PCI Express x1 (2.5 Gbps), Lane A<br>- SRIO2 x1 (2.5 Gbps; half-speed), Lane B<br>- SGMII x2 (1.25 Gbps; half-speed), Lanes E–F       | 100 MHz                      |
| 1101           | - Serdes disabled; Lanes A-B, E-F are powered-off                                                                                       | -                            |
| 1110           | - Reserved                                                                                                                              | -                            |
| 1111           | - PCI Express x4 (2.5 Gbps), Lanes A–B, E–F                                                                                             | 100 MHz                      |

**SW8.5-SW8.7: RapidIO Device ID of the MPC8569E**

- Specifies lower-order bits (3) for use by hosts on the RapidIO interface.
- (Default) If configured as a RapidIO host then the upper-order device ID bits default to '0'.
- If configured as a RapidIO agent then the upper-order device ID bits default to '1'.
- Regardless of host/agent mode configuration, unconnected `cfg_device_ID_1[n]` inputs default to '1'.

**SW8.8: RapidIO System Size**

- '0': Large system size with a maximum of 65,536 devices.
- '1': (Default) Small system size with a maximum of 256 devices.

**SW9 Configuration: BOOT****SW9.1-SW9.4: Boot ROM Location**

| Value (Binary) | Description                                  |
|----------------|----------------------------------------------|
| 0000           | PCI Express                                  |
| 0001           | Reserved                                     |
| 0010           | SRIO 1                                       |
| 0011           | SRIO 2                                       |
| 0100           | DDR Controller 1                             |
| 0101           | DDR Controller 2                             |
| 0110           | Reserved                                     |
| 0111           | ON-chip Boot ROM (eSDHC configuration)       |
| 1000           | Local bus FCM<br>8-bit NAND FLASH small page |
| 1001           | Reserved                                     |
| 1010           | Local bus FCM<br>8-bit NAND FLASH large page |
| 1011           | Reserved                                     |
| 1100           | Reserved                                     |
| 1101           | (Default) Local bus GPCM; 8-bit ROM          |
| 1110           | Local bus GPCM; 16-bit ROM                   |
| 1111           | Local bus GPCM; 16-bit ROM                   |

**SW9.5: CPU Boot Configuration**

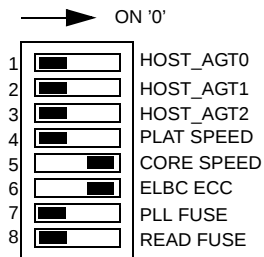
- '0': CPU boot hold-off mode. Until configured by an external master the e500 core can't boot.
- '1': (Default) Until configured by an external master the e500 core can't boot.

**SW9.6-SW9.7: Boot Sequencer Configuration**

- 00: Reserved
- 01: Uses normal I<sup>2</sup>C address mode. Boot sequencer is enabled. Loads configuration information from an I<sup>2</sup>C1 interface ROM; a valid ROM must be present.
- 10: Uses extended I<sup>2</sup>C address mode. Boot sequencer is enabled. Loads configuration information from an I<sup>2</sup>C1 interface ROM; a valid ROM must be present.
- 11: (Default) I<sup>2</sup>C ROMs not accessed. Boot sequencer is disabled.

**SW9.8: Reset Configuration Source**

- '0': RCW is read through I<sup>2</sup>C.
- '1': (Default) RCW is read through IO pin sampling.

**SW10 Configuration: AUX****SW10.1-SW10.3: Host/Agent Configuration**

| Value (Binary) | Description                                                              |
|----------------|--------------------------------------------------------------------------|
| 000            | MPC8569E acts as an Agent for PCI Express (EP) and both SRIO interfaces. |
| 001            | MPC8569E acts as an Agent for both SRIO interfaces.                      |
| 010            | Reserved                                                                 |
| 011            | Reserved                                                                 |
| 100            | Reserved                                                                 |
| 101            | Reserved                                                                 |
| 110            | MPC8569E acts as a PCI Express EP.                                       |
| 111            | (Default) MPC8569E acts as the Host-processor/RC.                        |

**SW10.4: Platform Speed**

- '0': CCB frequency is < 333 MHz.
- '1': (Default) CCB frequency is > or = to 333 MHz.

**SW10.5: Core speed**

- '1': Core clock frequency is < or = to 1000 MHz.
- '0': (Default) Core clock frequency is > 1000 MHz.

**SW10.6: eLBC ECC Enable**

- '0': (Default) eLBC ECC is disabled after POR.
- '1': eLBC ECC is enabled after POR.

**SW10.7: Fuse PLL Override Disable**

- '0': PLL parameters are controlled by fuse bits.
- '1': (Default) PLL parameters are controlled by plugs.

**SW10.8: Fuse Read Enable**

- '0': Fuse reads are disabled during the reset sequence.
- '1': (Default) Fuse reads are enabled during reset sequence.

## 7 Connector Default Settings

The below table, Table 5, lists factory default connector, header, and socket settings for the MPC8569E-MDS-PB. Figure 6 marks the location of the listed connector types.

**Table 5. MPC8569E-MDS-PB Connector Default Settings**

| #   | Type           | Description                        | Function                                                          |
|-----|----------------|------------------------------------|-------------------------------------------------------------------|
| J1  | Connector      | USB                                | (Default) OPEN                                                    |
| J2  | Socket         | DDR1 (64/32-bit)                   | SODIMM 64-bit/modified 32-bit if both MEMC1&2 controllers in use. |
| J3  | Socket         | DDR2 (32-bit)                      | SODIMM 64-bit if both MEMC1&2 controllers in use.                 |
| J4  | Header         | CPU FAN                            | MPC8569_5V_FAN                                                    |
| J5  | Header         | GETH4                              | (Default) OPEN                                                    |
| J6  | Header         | GETH2                              | (Default) OPEN                                                    |
| J7  | Header         | SerDes f                           | (Default) OPEN                                                    |
| J8  | Header         | Remote ON/OFF                      | (Default) Unassembled                                             |
| J9  | Header         | TEST                               | (Default) OPEN                                                    |
| J10 | Header         | SerDes a                           | (Default) OPEN                                                    |
| J11 | Socket         | System Clock Oscillator: 66.67 MHz | (Default) Inserted                                                |
| J12 | Socket         | PTP Clock Oscillator: 66.67 MHz    | (Default) Inserted                                                |
| J13 | 16-pin Header  | COP Interconnection                | External USB-TAP interconnection.                                 |
| J14 | Header         | GETH1                              | (Default) OPEN                                                    |
| J15 | Header         | GETH3                              | (Default) OPEN                                                    |
| J16 | Header         | SerDes e                           | (Default) OPEN                                                    |
| J17 | Header         | SerDes b                           | (Default) OPEN                                                    |
| J18 | Header         | System Clock Source Selection      | 1-2: External SYSCLK; 2-3: (Default) Onboard SYSCLK               |
| J19 | Header         | PTP Clock Source Selection         | 1-2: External SYSCLK; 2-3: (Default) Onboard SYSCLK               |
| J20 | SMB Connector  | External System Clock Source       | (Default) OPEN                                                    |
| J21 | 10-pin Header  | Dual RS-232 External Connection    | Interconnection with RS-232 adapter cable.                        |
| J22 | SMB Connector  | External PTP Clock Source          | (Default) OPEN                                                    |
| J23 | 3-pin Header   | POST FA_AND                        | (Default) Unassembled                                             |
| J24 | 3-pin Header   | POST FA_ANG                        | (Default) Unassembled                                             |
| J25 | 3-pin Header   | POST FA_VDD                        | (Default) Unassembled                                             |
| J26 | 3-pin Header   | IRSENSE                            | (Default) Unassembled                                             |
| J27 | MPC8569 Socket | MPI Socket; located on PS.         | (Default) Assembled                                               |

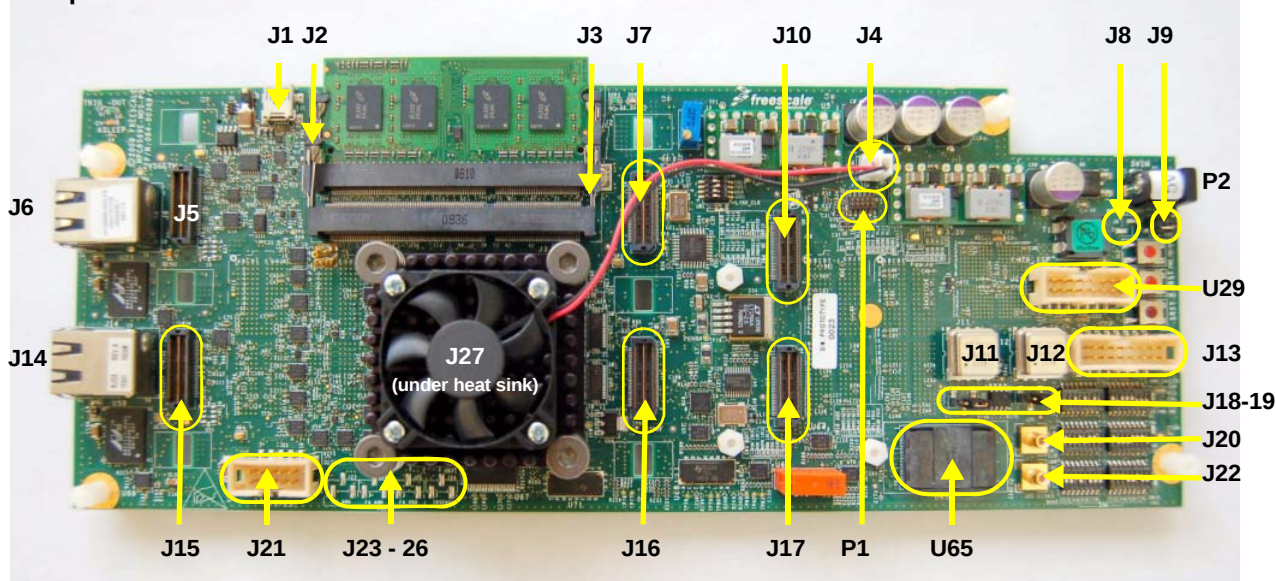
Table 5. MPC8569E-MDS-PB Connector Default Settings

| #                | Type          | Description                       | Function                            |
|------------------|---------------|-----------------------------------|-------------------------------------|
| U29 <sup>1</sup> | 16-pin Header | CNTR ISP                          | Used for BCSR programming.          |
| U65              | Socket        | NOR Flash Socket                  | (Default) Insert NOR Flash device.  |
| U118             | Socket        | NAND Flash Socket; located on PS. | (Default) Insert NAND Flash device. |
| P1               | 10-pin Header | PS ISP                            | Used for PS-cntr. PLD programming.  |
| P2               | Connector     | 5V IN power jack                  | MPC8569E-MDS-PB 5V power jack.      |
| P3               | Socket        | SD Card Slot; located on PS.      | Used for SD/MMC card insertion.     |

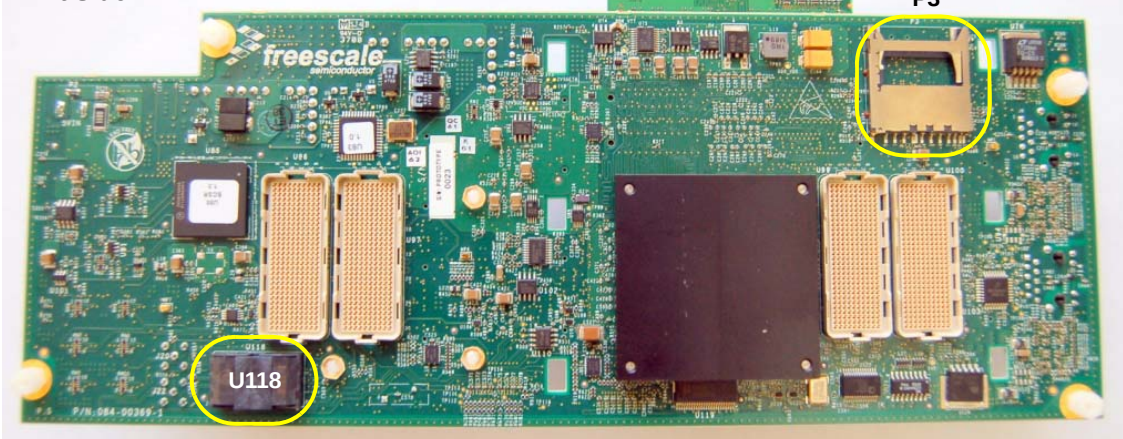
<sup>1</sup> An auxiliary connector (UTAP to CNTR-ISP) is used to reprogram the U86 onboard PLD Altera. Insert auxiliary connector into U29 header then attach USB TAP connector to auxiliary connector.

Figure 5. MPC8569E-MDS-PB Connectors

## Component Side



## Print Side



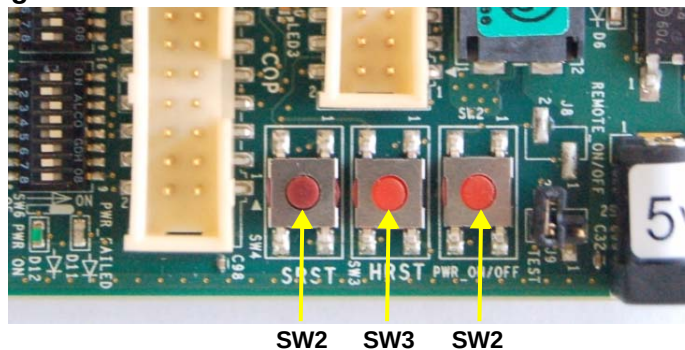
## 8 Push Buttons

Table 6 lists the functioning of MPC8569E-MDS-PB push buttons.

**Table 6. MPC8569E-MDS-PB Push Buttons**

| Push Button       | Position                                                                          | Description & Default                                                                                                                                                                                                                         |
|-------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SW2: POWER-ON/OFF |  | <ul style="list-style-type: none"> <li>Press SW2 to Power-ON/OFF all PB components.</li> <li>Powered from an external 5V power supply via the P2 power jack.</li> <li>Combined mode: +5V on PIB power supply via riser connectors.</li> </ul> |
| SW3: HRESET       |  | <ul style="list-style-type: none"> <li>Press SW3 for HRESET of the PB.</li> </ul>                                                                                                                                                             |
| SW4: SRESET       |  | <ul style="list-style-type: none"> <li>Press SW4 for SRESET of the PB.</li> <li>Retains clock and chip-select data contents despite the reset.</li> </ul>                                                                                     |

**Figure 6. MPC8569E-MDS-PB Push Button Locations**



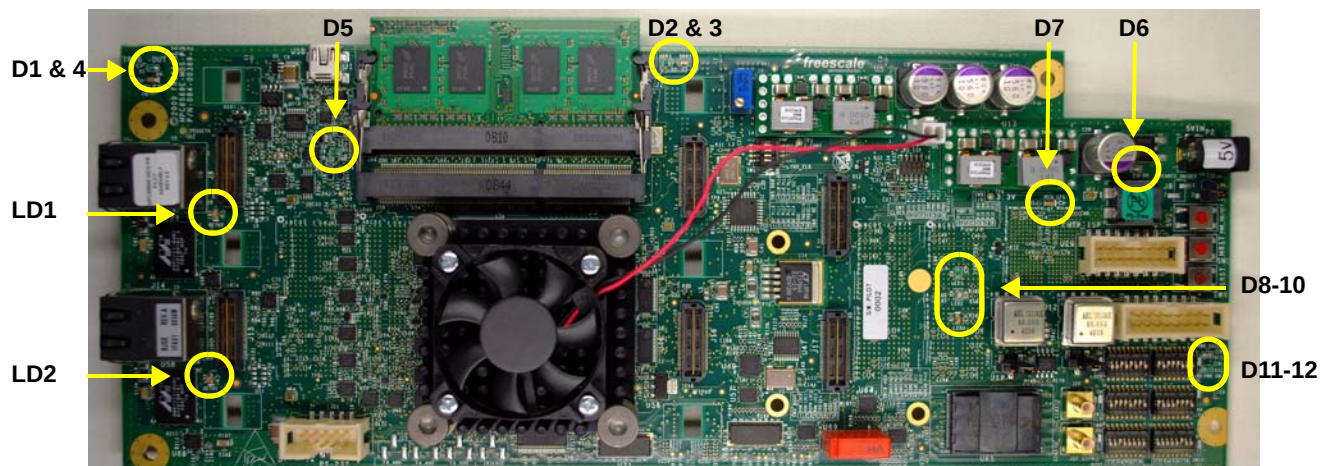
## 9 LED Lights

Table 7, below, lists the functioning of MPC8569E-MDS-PB LED lights. See Figure 8 for LED locations.

**Table 7. MPC8569E-MDS-PB LEDs**

| LED | Name       | Color  | LED ON                                                      | LED OFF                                                             |
|-----|------------|--------|-------------------------------------------------------------|---------------------------------------------------------------------|
| LD1 | GETH2      | Orange | • GETH2 enabled. BCSR8-[0] is high.                         | • BCSR8-[0] is low.                                                 |
| LD2 | GETH1      | Orange | • GETH1 enabled. BCSR7-[0] is high                          | • BCSR7-[0] is low.                                                 |
| D1  | TRIG OUT   | Green  | • Processor is in ready state.                              | • Processor NOT in ready state; or<br>• Processor is in debug mode. |
| D2  | DDR3       | Green  | • DDR3 (1.5V) voltage supply.                               | • Board is OFF (no power); or<br>• DDR2 voltage supply.             |
| D3  | DDR2       | Yellow | • DDR2 (1.8V) voltage supply.                               | • Board is OFF (no power); or<br>• DDR3 voltage supply.             |
| D4  | ASLEEP     | Orange | • MPC8569 HRESET is asserted.                               | • MPC8569 HRESET isn't asserted.                                    |
| D5  | USB POWER  | Green  | • BCSR17-[2] is low; USB power applied to J1 USB connector. | • BCSR17-[2] is high; USB power isn't applied to USB connector.     |
| D6  | 5VIN       | Yellow | • 5V input power applied to board.                          | • No power supplied to the board.                                   |
| D7  | REG CFG    | Orange | • MPC8569 configurable from BCSR.                           | • MPC8569 configurable from DIP-switches.                           |
| D8  | LED1       | Green  | • BCSR11-[1] is low.                                        | • BCSR11-[1] is high.                                               |
| D9  | LED2       | Yellow | • BCSR11-[2] is low.                                        | • BCSR11-[2] is high.                                               |
| D10 | LED3       | Orange | • BCSR11-[3] is low.                                        | • BCSR11-[3] is high.                                               |
| D11 | PWR FAILED | Red    | • Internal power supply fail.                               | • Internal power supply is good; or<br>• Board is OFF (no power).   |
| D12 | PWR ON     | Green  | • Internal power supply is good.                            | • Internal power supply is good; or<br>• Board is OFF (no power).   |

**Figure 7. MPC8569E-MDS-PB LEDs**



## 10 Board Control Status Registers (BCSR)

### 10.1 BCSR0

Table 8. BCSR0 Register

| Bit   | Config Signals    | Function                                                                                                                                                                       | Default                                   | Att |
|-------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-----|
| [0:3] | CFG_SYS_PLL[0:3]  | Establishes clock ratio between SYSCLK and CCB.                                                                                                                                | SW7[1:4] sampled at HRESET. <b>[1000]</b> | R,W |
| [4:6] | CFG_CORE_PLL[0:2] | Sets ratio between e500 Core PLL clock and CCB.                                                                                                                                | SW7[5:7] sampled at HRESET <b>[100]</b>   | R,W |
| [7]   | CFG_SRDS_REFCLK   | <ul style="list-style-type: none"> <li>0: SerDes expects 125 MHz reference clock frequency.</li> <li>1 (Default): SerDes expects 100 MHz reference clock frequency.</li> </ul> | SW7[8] sampled at HRESET <b>[1]</b>       | R,W |

### 10.2 BCSR1

Table 9. BCSR1 Register

| Bit   | Config Signals       | Function                                                                                                                                                                                                                                               | Default                                                                   | Att |
|-------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-----|
| [0:2] | CFG_DDR_CLK_PLL[0:2] | Configure DDR PLL ratio.                                                                                                                                                                                                                               | SW5[1:3] sampled at HRESET.<br>• DDR2 <b>[100]</b><br>• DDR3 <b>[110]</b> | R,W |
| [3]   | CFG_DDR_FB_SEL       | DDR QE and Platform PLL Feedback Select<br><ul style="list-style-type: none"> <li>0: gclk-matched/long DDR, QE, and Platform PLLs feedback path.</li> <li>1 (Default): local/short DDR PLL feedback path.</li> </ul>                                   | SW5[4] sampled at HRESET <b>[1]</b>                                       | R,W |
| [4]   | CFG_DDR_TYPE         | DDR Dram Type (DDR2 or DDR3)<br><ul style="list-style-type: none"> <li>0: DDR3 of 1.5V and low CKE at reset.</li> <li>1 (Default): DDR2 of 1.8V and low CKE at reset.</li> </ul>                                                                       | SW5[5] sampled at HRESET.<br>• DDR3 <b>[0]</b><br>• DDR2 <b>[1]</b>       | R,W |
| [5]   | CFG_DDR_MODE         | DDR Dram Mode (1x64 or 2x32)<br><ul style="list-style-type: none"> <li>0: Primary and Secondary DDR is enabled (32-bit width data bus).</li> <li>1 (Default): Primary DDR is enabled (64-bit width data bus) but secondary DDR is disabled.</li> </ul> | SW5[6] sampled at HRESET <b>[1]</b>                                       | R,W |
| [6]   | CFG_DDR_SPEED        | DDR speed configuration input configures internal logic for proper operation of the DDR.<br><ul style="list-style-type: none"> <li>0: DDR clock frequency &lt; 500MHz.</li> <li>1: DDR clock frequency is &gt; or = 500MHz.</li> </ul>                 | SW5[7] sampled at HRESET <b>[0]</b>                                       | R,W |
| [7]   | DDR_FIX              | <ul style="list-style-type: none"> <li>1: At reset, DDR disables both MCK and MCKE.</li> <li>0: DDR disables MCKE at reset; a few cycles later MCK is disabled.</li> </ul>                                                                             | SW5[8] sampled at HRESET <b>[1]</b>                                       | R,W |

## 10.3 BCSR2

Table 10. BCSR2 Register

| Bit   | Config Signals     | Function                                                                                                                                                                                                                  | Default                            | Att |
|-------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-----|
| [0:4] | CFG_QE_PLL[0:4]    | <ul style="list-style-type: none"> <li>A multiplier and divisor, applied to SYSCLK input, define the QE clock: <ul style="list-style-type: none"> <li>QE Clock=SYSCLK*(CFG QE PLL[0:4]/CFG_QE_CLK)</li> </ul> </li> </ul> | SW6[1:5] sampled at HRESET [01000] | R,W |
| [5]   | SDHC               | SDHC Card Detect Polarity Select <ul style="list-style-type: none"> <li>0: SDHC card-detect polarity is inverted.</li> <li>1 (Default): SDHC card-detect polarity isn't inverted.</li> </ul>                              | SW6[6] sampled at HRESET [1]       | R,W |
| [6:7] | CFG_LVDD_VSEL[0:1] | Voltage Select Dedicated Pins <ul style="list-style-type: none"> <li>QE UCC1 and UCC3 Voltage Select</li> <li>QE UCC2 and UCC4 Voltage Select</li> </ul>                                                                  | SW6[6:7] sampled at HRESET [11]    | R,W |

## 10.4 BCSR3

Table 11. BCSR3 Register

| Bit   | Config Signals    | Function                                                                                                                                                                                  | Default                           | Att |
|-------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----|
| [0:3] | CFG_PORT_SEL[0:3] | IO Select Configuration for SerDes.                                                                                                                                                       | SW8[1:4] sampled at HRESET [0111] | R,W |
| [4:6] | CFG_RIO_ID[5:7]   | RapidIO Device ID [5:7].                                                                                                                                                                  | SW8[5:7] sampled at HRESET [000]  | R,W |
| [7]   | CFG_RIO_SYS_SIZE  | RapidIO System Size <ul style="list-style-type: none"> <li>0: Large system size with a maximum of 65,536 devices.</li> <li>1: Small system size with a maximum of 256 devices.</li> </ul> | SW8[8] sampled at HRESET [1]      | R,W |

## 10.5 BCSR4

Table 12. BCSR4 Register

| Bit   | Config Signals    | Function                                                                                                                                                                                                                                                         | Default                           | Att |
|-------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----|
| [0:3] | CFG_ROM_LOC[0:3]  | Selects physical location of boot ROM.                                                                                                                                                                                                                           | SW9[1:4] sampled at HRESET [1101] | R,W |
| [4]   | CFG_BOOT_CPU      | Specifies Boot Configuration Mode: <ul style="list-style-type: none"> <li>0: CPU Boot Hold-off Mode; e500 core boots after configuration by an external master.</li> <li>1 (Default): e500 core boots without being configured by an external master.</li> </ul> | SW9[5] sampled at HRESET [1]      | R,W |
| [5:6] | CFG_BOOT_SEQ[0:1] | Boot Sequencer <ul style="list-style-type: none"> <li>Allows Boot Sequencer to load serial ROM (on I<sup>2</sup>C1 port) configuration data before the host configures the MPC8569E.</li> </ul>                                                                  | SW9[6:7] sampled at HRESET [11]   | R,W |

| Bit | Config Signals | Function                                                                                                                                                                                                  | Default                      | Att |
|-----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----|
| [7] | CFG_SOURCE     | Reset Configuration Source bit lets users select RCW source.<br><ul style="list-style-type: none"> <li>0: RCW is read through I<sup>2</sup>C.</li> <li>1: RCW is read through IO pin sampling.</li> </ul> | SW9[8] sampled at HRESET [1] | R/W |

## 10.6 BCSR5

Table 13. BCSR5 Register

| Bit   | Config Signals    | Function                                                                                                                                                                                                                                                     | Default                           | Att |
|-------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----|
| [0:2] | CFG_HOST_AGT[0:2] | MPC8569E configured to act as a host or agent to another interface master (PEX and SRIO).                                                                                                                                                                    | SW10[1:3] sampled at HRESET [111] | R,W |
| [3]   | CFG_PLAT_SPEED    | Platform speed configuration input configures internal logic for proper operation with CCB frequencies.<br><ul style="list-style-type: none"> <li>0: CCB frequency &lt; 333 MHz</li> <li>1: CCB frequency &gt; or = 333 MHz.</li> </ul>                      | SW10[4] sampled at HRESET [1]     | R,W |
| [4]   | CFG_CORE_SPEED    | Core speed configuration input configures internal logic for proper operation with core clock frequencies.<br><ul style="list-style-type: none"> <li>0: Core clock frequency &lt; or = to 1000MHz.</li> <li>1: Core clock frequency &gt; 1000MHz.</li> </ul> | SW10[5] sampled at HRESET [1]     | R,W |
| [5]   | CFG_ELBC_ECC      | POR configuration input enables eLBC ECC checking on booted external local bus interface.<br><ul style="list-style-type: none"> <li>0: eLBC ECC disabled after POR.</li> <li>1: eLBC ECC enabled after POR.</li> </ul>                                       | SW10[5] sampled at HRESET [0]     | R,W |
| [6]   | CFG_FUSE_OVR_DIS  | <ul style="list-style-type: none"> <li>0: Fuse PLL override is enabled.</li> <li>1: Fuse PLL override is disabled.</li> </ul>                                                                                                                                | SW10[6] sampled at HRESET [1]     | R,W |
| [7]   | CFG_FUSE_READ     | Fuse Read Enable<br><ul style="list-style-type: none"> <li>0: Fuse reads are disabled during reset sequence.</li> <li>1 (Default): Fuse reads are enabled during reset sequence.</li> </ul>                                                                  | SW10[7] sampled at HRESET [1]     | R,W |

## 10.7 BCSR6

Table 14. BCSR6 Register description

| Bit | Config Signals | Function                                                                                                                                                                                                                                   | Default | Att |
|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | UPC1_EN        | <ul style="list-style-type: none"> <li>1: Enable UPC1, ATM, or POS</li> <li>0: Disable UPC1 <b>OR</b> enable TDM1A, TDM1B, TDM1E, TDM1F, TDM1G, TDM1H, TDM2A, TDM2C, TDM2D, TDM2E, RMII5, RMII7, RMII8, TDM2G, TDM2F, and RMII6</li> </ul> | [1]     | R,W |
| [1] | RUPC1POS_EN    | <ul style="list-style-type: none"> <li>1: Enable UPC1POS</li> <li>0: Disable UPC1POS <b>OR</b> enable TDM2A and TDM1B</li> </ul>                                                                                                           | [1]     | R,W |

| Bit | Config Signals | Function                                                                                                                                                                                                                        | Default | Att |
|-----|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [2] | RUPC1ADDR_EN   | <ul style="list-style-type: none"> <li>1: Enable UPC1ADDR, ATM, or POS</li> <li>0: Disable UPC1ADDR (Unsupported: SMII8 and SMII6)</li> </ul>                                                                                   | [1]     | R,W |
| [3] | RUPC1DEV2      | <ul style="list-style-type: none"> <li>1: Enable UPC1DEV2, ATM, or POS</li> <li>0: Disable UPC1DEV2 <b>OR</b> enable TDM2C and UCC3</li> </ul>                                                                                  | [1]     | R,W |
| [4] | SD_CARD_1bit   | <ul style="list-style-type: none"> <li>1: Enable SD serial mode <b>AND</b> disable I<sup>2</sup>C2</li> <li>0: Disable SD serial mode <b>AND</b> enable I<sup>2</sup>C2</li> </ul>                                              | [0]     | R,W |
| [5] | SD_CARD_4bits  | <ul style="list-style-type: none"> <li>1: Enable SD Card nibble mode (SD_CARD_1bit should be "1") <b>AND</b> disable DUART0 and I<sup>2</sup>C2 bus</li> <li>0: Enable DUART0 <b>AND</b> disable SD Card nibble mode</li> </ul> | [0]     | R,W |
| [6] | TDM2G          | <ul style="list-style-type: none"> <li>UPC1_EN = 0(BCSR6[7], disable)</li> <li>If bit =1, TDM2G is enabled</li> <li>RMII7(BCSR6[7] should be = 0</li> </ul>                                                                     | [1]     | R,W |
| [7] | RMII7          | <ul style="list-style-type: none"> <li>UPC1_EN = 0((BCSR6[7], disable)</li> <li>If bit =1, RMII7 is enabled</li> <li>TDM2G(BCSR6[6] should be = 0)</li> </ul>                                                                   | [1]     | R,W |

## 10.8 BCSR7

**Table 15. BCSR7 Register description**

| Bit | Config Signals    | Function                                                                                                                                                      | Default | Att |
|-----|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | UCC1_GETH         | <ul style="list-style-type: none"> <li>1: Enable UCC1_GETH, RGMII, or RTBI</li> <li>0: Disable UCC1_GETH <b>OR</b> enable UCC1_RMII (RMII1) on PIB</li> </ul> | [1]     | R,W |
| [1] | UCC1_RGMII        | <ul style="list-style-type: none"> <li>1: Enable RGMII</li> <li>0: Disable RTBI <b>AND</b> enable RMII on PIB</li> </ul>                                      | [1]     | R,W |
| [2] | UCC1_RTBI         | <ul style="list-style-type: none"> <li>1: Enable RTBI</li> <li>0: Disable RGMII <b>AND</b> enable RMII on PIB</li> </ul>                                      | [0]     | R,W |
| [3] | G1DIS_125         | <ul style="list-style-type: none"> <li>1: Disable PHY1 clock_out 125MHz</li> <li>0: Enable</li> </ul>                                                         | [0]     | R,W |
| [4] | G1ENA_XC          | <ul style="list-style-type: none"> <li>1: Enable</li> <li>0: Disable</li> </ul>                                                                               | [0]     | R,W |
| [5] | UCC1/UCC2 GETHRST | <ul style="list-style-type: none"> <li>1: Normal operation</li> <li>0: Reset (nMVRST) Marvel UCC1 and UCC2</li> </ul>                                         | [1]     | R,W |
| [6] | BRDWP             | <ul style="list-style-type: none"> <li>BRD (EEPROM I<sup>2</sup>C Memory): write protected for I<sup>2</sup>C Flash</li> <li>0: Not protected</li> </ul>      | [1]     | R,W |
| [7] | BOOTWP            | <ul style="list-style-type: none"> <li>1: Not protected.</li> <li>Boot write protected</li> </ul>                                                             | [0]     | R,W |

## 10.9 BCSR8

Table 16. BCSR8 Register

| Bit | Config Signals        | Function                                                                                                                                                      | Default | Att |
|-----|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | UCC2_GETH             | <ul style="list-style-type: none"> <li>1: Enable UCC2_GETH, RGMII, or RTBI</li> <li>0: Disable UCC2_GETH <b>OR</b> enable UCC2_RMII (RMII2) on PIB</li> </ul> | [1]     | R,W |
| [1] | UCC2_RGMII            | <ul style="list-style-type: none"> <li>1: Enable RGMII</li> <li>0: Disable RTBI <b>AND</b> enable RMII on PIB</li> </ul>                                      | [1]     | R,W |
| [2] | UCC2_RTBI             | <ul style="list-style-type: none"> <li>1: Enable RTBI</li> <li>0: Disable RGMII <b>AND</b> enable RMII on PIB</li> </ul>                                      | [0]     | R,W |
| [3] | G2DIS_125             | <ul style="list-style-type: none"> <li>1: Disable PHY2 clock_out 125MHz</li> <li>0: Enable PHY2 clock_out 125MHz</li> </ul>                                   | [0]     | R,W |
| [4] | G2ENA_XC              | <ul style="list-style-type: none"> <li>1: Enable</li> <li>0: Disable</li> </ul>                                                                               | [0]     | R,W |
| [5] | CS_NOR                | <ul style="list-style-type: none"> <li>1: Boot from NAND_FLASH</li> <li>0: Boot from NOR_FLASH</li> </ul>                                                     | [0]     | R,W |
| [6] | UEM Marvell PHY RESET | <ul style="list-style-type: none"> <li>1: RESET UEM3 (UCC3) and UEM4 (UCC4)</li> <li>0: Normal operation</li> </ul>                                           | [0]     | R,W |
| [7] | DDRDRV_SEL            | <ul style="list-style-type: none"> <li>1: MEMC1,2: MDIC0,1=36.5OHm</li> <li>0: MEMC1,2: MDIC0,1=18OHm</li> </ul>                                              | [1]     | R,W |

## 10.10 BCSR9

Table 17. BCSR9 Register

| Bit | Config Signals | Function                                                                                                                                                                                                                                                                                                               | Default | Att |
|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | UCC3_GETH      | <ul style="list-style-type: none"> <li>1: Enable UCC3_GETH <ul style="list-style-type: none"> <li>– Use UEM module on PB for RGMII or RTBI.</li> </ul> </li> <li>0: Disable UCC3_GETH <b>OR</b> enable (depending upon UCC3_RMII bit) UCC3_RMII (RMII3) on PIB or TDM1C</li> </ul>                                     | [1]     | R,W |
| [1] | UCC3_RGMII     | <ul style="list-style-type: none"> <li>1: Enable RGMII on UEM</li> <li>0: Disable RTBI on UEM <b>AND</b> enable RMII3 on PIB</li> </ul>                                                                                                                                                                                | [1]     | R,W |
| [2] | UCC3_RTBI      | <ul style="list-style-type: none"> <li>1: Enable RTBI on UEM</li> <li>0: Disable RGMII on UEM <b>AND</b> enable RMII3 on PIB</li> </ul>                                                                                                                                                                                | [0]     | R,W |
| [3] | UCC3_RMII      | <ul style="list-style-type: none"> <li>If UCC3_GETH = 0 <ul style="list-style-type: none"> <li>– then bit = 1 enables UCC3_RMII on PIB</li> <li>– then bit =0 enables TDM1C and UPC1_DEV2</li> </ul> </li> <li>If UCC3_GETH = 1 <ul style="list-style-type: none"> <li>– then bit has no effect</li> </ul> </li> </ul> | [0]     | R,W |

| Bit | Config Signals | Function                                                                                                                                 | Default | Att |
|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [4] | RMII3__nSMII3  | <ul style="list-style-type: none"> <li>1: Enable RMII on PB (UEM)</li> <li>0: Enable SMII on PB (UEM) UCC6 (SMII unsupported)</li> </ul> | [1]     | R,W |
| [5] | R_SMII3_nRMII3 | <ul style="list-style-type: none"> <li>1: Enable SMII on PB (UEM) UCC6 (SMII unsupported)</li> <li>0: Enable RMII on PB (UEM)</li> </ul> | [0]     | R,W |
| [6] | RESERVED       | RESERVED                                                                                                                                 | [1]     | R,W |
| [7] | nMVPHY_MICPHY3 | Select UEM-assembled Marvell PHY or Micrel PHY. <ul style="list-style-type: none"> <li>1: Micrel</li> <li>0: Marvel</li> </ul>           | [0]     | R,W |

## 10.11 BCSR10

Table 18. BCSR10 Register

| Bit | Config Signals  | Function                                                                                                                                                                                       | Default | Att |
|-----|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | UCC4_GETH       | <ul style="list-style-type: none"> <li>1: Enable UCC4_GETH Use UEM module on PB for RGMII or RTBI.</li> <li>0: Disable UCC4_GETH <b>OR</b> enable UCC4_RMII (RMII4) on PIB or TDM1C</li> </ul> | [1]     | R,W |
| [1] | UCC4_RGMII      | <ul style="list-style-type: none"> <li>1: Enable RGMII on UEM</li> <li>0: Disable RTBI on UEM <b>AND</b> enable RMII3 on PIB</li> </ul>                                                        | [1]     | R,W |
| [2] | UCC4_RTBI       | <ul style="list-style-type: none"> <li>1: Enable RTBI on UEM</li> <li>0: Disable RGMII on UEM <b>AND</b> enable RMII3 on PIB</li> </ul>                                                        | [0]     | R,W |
| [3] | RMII4__nSMII4   | <ul style="list-style-type: none"> <li>1: Enable RMII on PB (UEM)</li> <li>0: Enable SMII on PB (UEM) UCC8 (SMII unsupported)</li> </ul>                                                       | [1]     | R,W |
| [4] | R_SMII4_nRMII4  | <ul style="list-style-type: none"> <li>0: Enable RMII on PB (UEM)</li> <li>1: Enable SMII on PB (UEM) UCC8 (SMII unsupported)</li> </ul>                                                       | [0]     | R,W |
| [5] | nMVPHY_MICPHY4  | Select UEM assembled Marvell PHY or Micrel PHY.                                                                                                                                                | [0]     | R,W |
| [6] | RnMICRST        | <ul style="list-style-type: none"> <li>0: Micrel PHY Reset on both UCC3- &amp; UCC4-connected UEMs</li> <li>1: Normal operation</li> </ul>                                                     | [0]     | R,W |
| [7] | RMV_SEL_FREQ_34 | <ul style="list-style-type: none"> <li>1: Marvell PHY, UCC3 &amp; UCC4 have 25MHz input on UEM</li> <li>0: Marvell PHY, UCC3 &amp; UCC4 have 125MHz input on UEM</li> </ul>                    | [0]     | R,W |

## 10.12 BCSR11

Table 19. BCSR11 Register

| Bit     | Config Signals  | Function                                                                                                                                                                                                                                                                                                                                                                                                         | Default         | Att  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
|---------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----------|--------|--------|-----------------|---------|--------|-----------|--------|---------|------------|---------|---------|-----------|-----|-----|---|-----|-----|
| [0]     | REGISTER_CONFIG | <ul style="list-style-type: none"><li>• 0: Board configured through DIP-switches</li><li>• 1: Board configured through BCSR registers</li></ul>                                                                                                                                                                                                                                                                  | [0]             | R,W  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [1]     | LED1            | 1: LED ON                                                                                                                                                                                                                                                                                                                                                                                                        | [0]             | R,W  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [2]     | LED2            | 1: LED ON                                                                                                                                                                                                                                                                                                                                                                                                        | [0]             | R,W  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [3]     | LED3            | 1: LED ON                                                                                                                                                                                                                                                                                                                                                                                                        | [0]             | R,W  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [4]     | R_SLEW0         | <div>Select slew rate for GETH input clock.</div> <table><thead><tr><th colspan="2">Setting</th><th>Slew Rate</th></tr><tr><th>SLEW0</th><th>SLEW1</th><th>(V/ns)</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>4</td></tr><tr><td>1</td><td>0</td><td>3</td></tr><tr><td>0</td><td>1</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table>                                           | Setting         |      | Slew Rate | SLEW0  | SLEW1  | (V/ns)          | 0       | 0      | 4         | 1      | 0       | 3          | 0       | 1       | 2         | 1   | 1   | 1 | [0] | R,W |
| Setting |                 |                                                                                                                                                                                                                                                                                                                                                                                                                  | Slew Rate       |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| SLEW0   | SLEW1           |                                                                                                                                                                                                                                                                                                                                                                                                                  | (V/ns)          |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 0       | 0               |                                                                                                                                                                                                                                                                                                                                                                                                                  | 4               |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 1       | 0               |                                                                                                                                                                                                                                                                                                                                                                                                                  | 3               |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 0       | 1               | 2                                                                                                                                                                                                                                                                                                                                                                                                                |                 |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 1       | 1               | 1                                                                                                                                                                                                                                                                                                                                                                                                                |                 |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [5]     | R_SLEW          |                                                                                                                                                                                                                                                                                                                                                                                                                  | [1]             | R,W  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [6]     | SSC0            | <div>Select SerDes clock synthesizer spread spectrum mode.</div> <table><thead><tr><th>SSC0</th><th>SSC1</th><th>SPREAD%</th></tr></thead><tbody><tr><td>0 (ON)</td><td>0 (ON)</td><td>CENTER +/- 0.25</td></tr><tr><td>1 (OFF)</td><td>0 (ON)</td><td>DOWN -0.5</td></tr><tr><td>0 (ON)</td><td>1 (OFF)</td><td>DOWN -0.75</td></tr><tr><td>1 (OFF)</td><td>1 (OFF)</td><td>NO SPREAD</td></tr></tbody></table> | SSC0            | SSC1 | SPREAD%   | 0 (ON) | 0 (ON) | CENTER +/- 0.25 | 1 (OFF) | 0 (ON) | DOWN -0.5 | 0 (ON) | 1 (OFF) | DOWN -0.75 | 1 (OFF) | 1 (OFF) | NO SPREAD | [1] | R,W |   |     |     |
| SSC0    | SSC1            |                                                                                                                                                                                                                                                                                                                                                                                                                  | SPREAD%         |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 0 (ON)  | 0 (ON)          |                                                                                                                                                                                                                                                                                                                                                                                                                  | CENTER +/- 0.25 |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 1 (OFF) | 0 (ON)          |                                                                                                                                                                                                                                                                                                                                                                                                                  | DOWN -0.5       |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 0 (ON)  | 1 (OFF)         |                                                                                                                                                                                                                                                                                                                                                                                                                  | DOWN -0.75      |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| 1 (OFF) | 1 (OFF)         | NO SPREAD                                                                                                                                                                                                                                                                                                                                                                                                        |                 |      |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |
| [7]     | SSC1            |                                                                                                                                                                                                                                                                                                                                                                                                                  | [1]             | R,W  |           |        |        |                 |         |        |           |        |         |            |         |         |           |     |     |   |     |     |

## 10.13 BCSR12

Table 20. BCSR12 Register

| Bit | Config Signals | Function                                                                                                                                                | Default | Att |
|-----|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | PCIE_CLKDIS    | <ul style="list-style-type: none"> <li>1: Enable PEX clock</li> <li>0: Disable PEX clock</li> </ul>                                                     | [1]     | R,W |
| [1] | TRIGIN         | For internal use only (0)                                                                                                                               | [Z]     | R,W |
| [2] | RMII6          | <ul style="list-style-type: none"> <li>1: Enable RMII6 (on PIB) and TDM2F<sup>1</sup></li> <li>0: Disable RMII6 <b>AND</b> enable ATM or POS</li> </ul> | [1]     | R,W |
| [3] | RMII8          | <ul style="list-style-type: none"> <li>1: Enable RMII8 (on PIB)</li> <li>0: Disable RMII8 <b>AND</b> enable TDM1H</li> </ul>                            | [0]     | R,W |

| Bit | Config Signals | Function                                                                                                                                                                | Default | Att |
|-----|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [4] | TDM2D_2F_DIS   | <ul style="list-style-type: none"> <li>1: For RMII6 on PIB</li> <li>0: For UPC1 or TDM2D or TDM2F</li> </ul>                                                            | [0]     | R,W |
| [5] | RGETH_CLKSEL   | <ul style="list-style-type: none"> <li>1: UEM ref clk = 125MHz</li> <li>0: UEM ref clk = 50MHz</li> </ul>                                                               | [1]     | R,W |
| [6] | RESET_PIB      | <ul style="list-style-type: none"> <li>1: RESET RMII PHY, TDM framer, and/ or ATM PHY</li> <li>0: Normal operation for RMII PHY, TDM framer, and/ or ATM PHY</li> </ul> | [0]     | R,W |
| [7] | ISOLATE_GPIO   | <ul style="list-style-type: none"> <li>1: For RMII6 and RMII7 operation</li> <li>0: For UPC1 operation</li> </ul>                                                       | [0]     | R,W |

<sup>1</sup> I<sup>2</sup>C PCA9555 address 26H should drive output register 1[0] to 1.

## 10.14 BCSR13

Table 21. BCSR13 Register

| Bit   | Config Signals | Function          | Default | Att |
|-------|----------------|-------------------|---------|-----|
| [0:7] | R_PS[0:7]      | Internal Use Only | [1:1]   | R,W |

## 10.15 BCSR14

Table 22. BCSR14 Register

| Bit   | Config Signals | Function                                                                                                   | Default | Att |
|-------|----------------|------------------------------------------------------------------------------------------------------------|---------|-----|
| [0:4] | R_PS[8:12]     | Internal Use Only                                                                                          | [11111] | R,W |
| [5]   | TDM1G_EN       | <ul style="list-style-type: none"> <li>1: TDM1G_EN enabled</li> <li>0: TDM1G_EN disabled</li> </ul>        | [0]     | R,W |
| [6]   | PRESENCE 3     | UEM inserted into J15 <ul style="list-style-type: none"> <li>1: Present</li> <li>0: Not present</li> </ul> | [X]     | R   |
| [7]   | PRESENCE 4     | UEM inserted into J5 <ul style="list-style-type: none"> <li>1: Present</li> <li>0: Not present</li> </ul>  | [X]     | R   |

## 10.16 BCSR15

Table 23. BCSR15 Register

| Bit | Config Signals | Function                                                                        | Default | Att |
|-----|----------------|---------------------------------------------------------------------------------|---------|-----|
| [0] | G3ENA_XC       | <ul style="list-style-type: none"> <li>1: Enable</li> <li>0: Disable</li> </ul> | [0]     | R,W |

| Bit | Config Signals | Function                                                                                                                                                                     | Default | Att |
|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [1] | G4ENA_XC       | <ul style="list-style-type: none"> <li>1: Enable</li> <li>0: Disable</li> </ul>                                                                                              | [0]     | R,W |
| [2] | G3DIS_125      | <ul style="list-style-type: none"> <li>1: Disable PHY3 clock_out 125MHz</li> <li>0: Enable PHY3 clock_out 125MHz</li> </ul>                                                  | [0]     | R,W |
| [3] | G4DIS_125      | <ul style="list-style-type: none"> <li>1: Disable PHY4 clock_out 125Mhx</li> <li>0: Enable</li> </ul>                                                                        | [0]     | R,W |
| [4] | SMII6 DIS      | <ul style="list-style-type: none"> <li>1: Disable SMII6 <b>AND</b> enable RMII6, TDM1C, UPC1 Dev2, and UCC3</li> <li>0: Enable SMII6 and TDM2D (SMII unsupported)</li> </ul> | [1]     | R,W |
| [5] | SMII8 DIS      | <ul style="list-style-type: none"> <li>1: Enable UCC8 RMII on PIB and TDM1H <b>AND</b> disable SMII8.</li> <li>0: Enable SMII8 (SMII unsupported)</li> </ul>                 | [1]     | R,W |
| [6] | TDM1F          | <ul style="list-style-type: none"> <li>1: Enable TDM1F</li> <li>0: Disable TDM1F</li> </ul>                                                                                  | [1]     | R,W |
| [7] | RUART1_nQEUART | <ul style="list-style-type: none"> <li>1: Enable QE_UART</li> <li>0: Enable UART1, TDM1D, and TDM2B</li> </ul>                                                               | [0]     | R,W |

## 10.17 BCSR16

Table 24. BCSR16 Register

| Bit | Config Signals | Function                                                                                                                                                                                                                                                        | Default | Att |
|-----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | PORESET        | PWR_ON Reset/HRESET <ul style="list-style-type: none"> <li>0: Active</li> </ul>                                                                                                                                                                                 | [1]     | R,W |
| [1] | TSEC0MST       | Reserved                                                                                                                                                                                                                                                        | [1]     | R,W |
| [2] | TSEC1MST       | Reserved                                                                                                                                                                                                                                                        | [1]     | R,W |
| [3] | TSEC2MST       | Reserved                                                                                                                                                                                                                                                        | [1]     | R,W |
| [4] | TSEC3MST       | Reserved                                                                                                                                                                                                                                                        | [1]     | R,W |
| [5] | TSEC4MST       | Reserved                                                                                                                                                                                                                                                        | [1]     | R,W |
| [6] | TDM1C_DEV2     | <ul style="list-style-type: none"> <li>1: Enable UPC1 Device2</li> <li>0: Disable UPC1 Device 2 <b>OR</b> enable RMII3 on PIB,TDM1C and TDM2C</li> <li>If bit = 0 then RMII3 is enabled</li> <li>Dev2- RxEN_B[2]</li> <li>TDM2c-TSYNC</li> <li>TDM1c</li> </ul> | [0]     | R,W |
| [7] | RESERVED       | -                                                                                                                                                                                                                                                               | [0]     | R,W |

## 10.18 BCSR17

Table 25. BCSR17 Register

| Bit | Config Signals | Function                                                                                                                                                                                                                                                                                                                                              | Default | Att |
|-----|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|
| [0] | RnUSBEN        | <ul style="list-style-type: none"> <li>1: Disable USB <b>AND</b> enable TDM1B</li> <li>0: Enable USB</li> </ul>                                                                                                                                                                                                                                       | [1]     | R,W |
| [1] | RnUSBLOWSPD    | <ul style="list-style-type: none"> <li>1: USB full-speed (12Mb/s)</li> <li>0: USB low-speed (1.5Mb/s)</li> </ul>                                                                                                                                                                                                                                      | [0]     | R,W |
| [2] | RnUSBVCC       | <ul style="list-style-type: none"> <li>0: USB acts as Device               <ul style="list-style-type: none"> <li>– USB powered from an external host</li> <li>– Enables RMII6 and TDM1G</li> </ul> </li> <li>1: USB acts as Host               <ul style="list-style-type: none"> <li>– USB supplies power to external device</li> </ul> </li> </ul> | [0]     | R,W |
| [3] | RUSB_MODE      | USB Mode <ul style="list-style-type: none"> <li>1: Host</li> <li>0: Device</li> </ul>                                                                                                                                                                                                                                                                 | [0]     | R,W |
| [4] | RPRESENCE_F    | UEM inserted into J7 <ul style="list-style-type: none"> <li>1: Present</li> <li>0: Not present</li> </ul>                                                                                                                                                                                                                                             | [x]     | R   |
| [5] | RPRESENCE_E    | UEM inserted into J16 <ul style="list-style-type: none"> <li>1: Present</li> <li>0: Not present</li> </ul>                                                                                                                                                                                                                                            | [x]     | R   |
| [6] | RFLASH_RDY     | <ul style="list-style-type: none"> <li>1: Ready</li> <li>0: Busy</li> </ul>                                                                                                                                                                                                                                                                           | [x]     | R   |
| [7] | FLASH_nWP      | <ul style="list-style-type: none"> <li>0: FLASH Write Protect</li> <li>1: FLASH normal operation</li> </ul>                                                                                                                                                                                                                                           | [0]     | R,W |

## 10.19 BCSR18

Table 26. BCSR18 Register

| Bit   | Config Signals | Function                                                                                              | Value           | Att |
|-------|----------------|-------------------------------------------------------------------------------------------------------|-----------------|-----|
| [0:3] | REV            | <ul style="list-style-type: none"> <li>BCSR revision</li> <li>Four bit revision coding</li> </ul>     | current version | R,W |
| [4:7] | SUBREV         | <ul style="list-style-type: none"> <li>BCSR SUB revision</li> <li>Four bit revision coding</li> </ul> | sub version     | R,W |

# 11 Memory Map

## 11.1 MPC8569E PB Memory Map

### NOTE!

The memory map has NOT been finalized.

Access to MPC8569 memory slaves is controlled by the MPC8569 memory controller. [Table 27](#) is only a recommended memory map; it is a "soft" map device. Users are free to move addresses around the map.

**Table 27.** MPC8569E-MDS-PB Memory Map (with NOR Flash as Boot Source)

| ADDRESS RANGE         | Block                       | Allocation                            | Port Size |
|-----------------------|-----------------------------|---------------------------------------|-----------|
| 00000000 - 1FFFFFFF   | DDR3/DDR3 Memory Controller | MEMC1 (512MB)                         | 32        |
| 00000000 - 3FFFFFFF   |                             | MEMC1 (Integrated Mode) 1GB           | 64        |
| 20000000 - 3FFFFFFF   |                             | MEMC2 (512MB)                         | 32        |
| 40000000 - 7FFFFFFF   | Reserved                    | 1GB                                   |           |
| 80000000 - 9FFFFFFF   | SRIO1                       | Outbound Window (512 MB)              | x4 lane   |
| A0000000 - BFFFFFFF   | SRIO2                       | Outbound Window (512 MB)              | x4 lane   |
| C0000000 - DFFFFFFF   | PEX                         | Outbound Window (512 MB)              | x4 lane   |
| E0000000 - E0FFFFFF   | MPC8569 Internal Map        | Internal Memory Register Space (1 MB) | 32        |
| E0100000 - E03FFFFFFF | Reserved                    | For future MPC8569 derivatives (3 MB) | -         |
| E0400000 - E047FFFF   | L2SRAM                      | 1MB                                   |           |
| E0480000 - F7FFFFFF   | Reserved                    | 400MB                                 |           |
| F8000000 - F8007FFF   | BCSR on CS1                 | Altera (32KB)                         | 8         |
| F8008000 - F800FFFF   | CS4                         | PIB (32KB)                            | 8         |
| F8010000 - F8017FFF   | CS5                         | PIB (32KB)                            | 8         |
| FA018000 - FFFFFFFF   | Reserved                    | 100MB                                 |           |
| FC000000 - FFFFFFFF   | NAND Flash on CS3/CS0       | Samsung: K9F5608U0D-PCB0 (32MB)       | 8         |
| FE000000 - FFFFFFFF   | NOR Flash on CS0/CS3        | Spansion: S29GL256N11TFIV2O (32MB)    | 8         |

## 12 Working Environment

**Table 28. MPC8569E-MDS-PB Working Environment Modes**

| Mode                                       | Optional Expansion                                                                                                                                                                                                                                                            | Description                                                                                                                                                                                                     |
|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Standalone<br>PEX RC                       | Includes the noted modules: <ul style="list-style-type: none"> <li>• GETH3 &amp; 4 UEM</li> <li>• SerDes Lane e, f SRIOx1 or UEM (SGMII mode)</li> <li>• SerDes Lane a, b SRIOx1</li> <li>• SerDes Lane a, b PEXx2</li> <li>• 1xDDR3 SODIMMx64 or 2xDDR3x32 SODIMM</li> </ul> | <ul style="list-style-type: none"> <li>• PB powered, via P2, by an external 5V power supply (included in kit).</li> <li>• [Option] PEX EP powered, via P2 of PEXx2, by an external 12V power supply.</li> </ul> |
| PIB-combined Mode<br>MPC9569-MDS-PB on PIB | Includes the noted modules: <ul style="list-style-type: none"> <li>• GETH3 &amp; 4 UEM</li> <li>• SerDes Lane e, f SRIOx1 or UEM (SGMII mode)</li> <li>• SerDes Lane a, b SRIOx1</li> <li>• SerDes Lane a, b PEXx2</li> <li>• 1xDDR3 SODIMMx64 or 2xDDR3x32 SODIMM</li> </ul> | <ul style="list-style-type: none"> <li>• PB powered from PIB via bottom riser connectors.</li> <li>• [Option] PEX EP powered, via P2 of PEXx2, from an external 12V power supply.</li> </ul>                    |

## 13 Getting Started Procedures

This section outlines “Getting Started” procedures for the MPC8569E-MDS-PB including use of the JTAG connectivity unit. Optional modules are detailed in Section 12.

**Procedure 1: Check hardware kit contents (Section 4).**

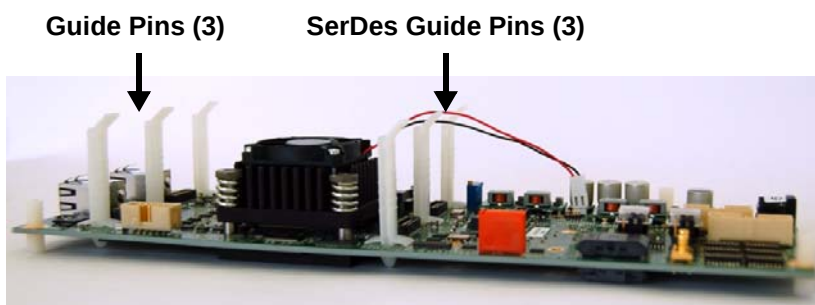
**Procedure 2: Check PB default switch settings (Section 6).**

**Procedure 3: Check PB default connector settings (Section 7).**

**Procedure 4: Establish working environment (Section 12).**

**Procedure 5: Insert plastic guide pins into PB.**

1. Insert three guide pins. Pins hold UEM modules used in RGMII and RTBI modes.
2. Insert three guide pins. Pins hold UEM modules (SGMII mode) used for SerDes Options 1, 2 and 3. See Section 12, Set-up 1.

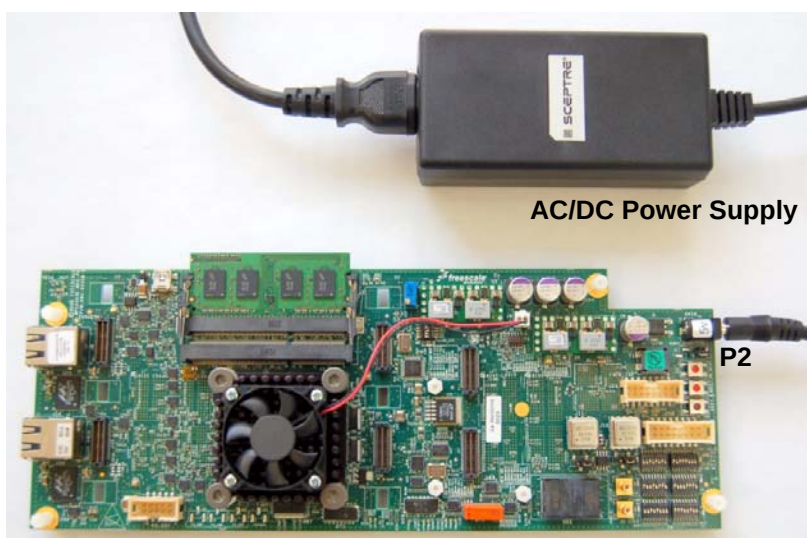


**Procedure 6: Assemble and connect 5V power supply.**

**NOTE!**

Ensure Power-OFF.

1. Assemble AC/DC power supply kit:
  - a) Cable with country-specific wall outlet plug.
  - b) Power supply unit and cable with plug (for board connection).
2. Connect the AC/DC power supply cable to the 5V IN on-board jack (P2).
3. Plug the power cable into the wall outlet.



**Procedure 7: Perform initial board power-up and check LEDs (Section 7-8).****CAUTION!**

Prevent damage to the USB TAP; connect only after initial board reset.

1. Power PB via an external 5V power supply; LED D6 glows yellow.
2. Press SW2 to Power-ON all PB components.
3. Check for completion of PRESET sequence; indicated by steady lights from LEDs D1, D2 or D3, and D12.
4. Press SW2 to Power-OFF all PB components.

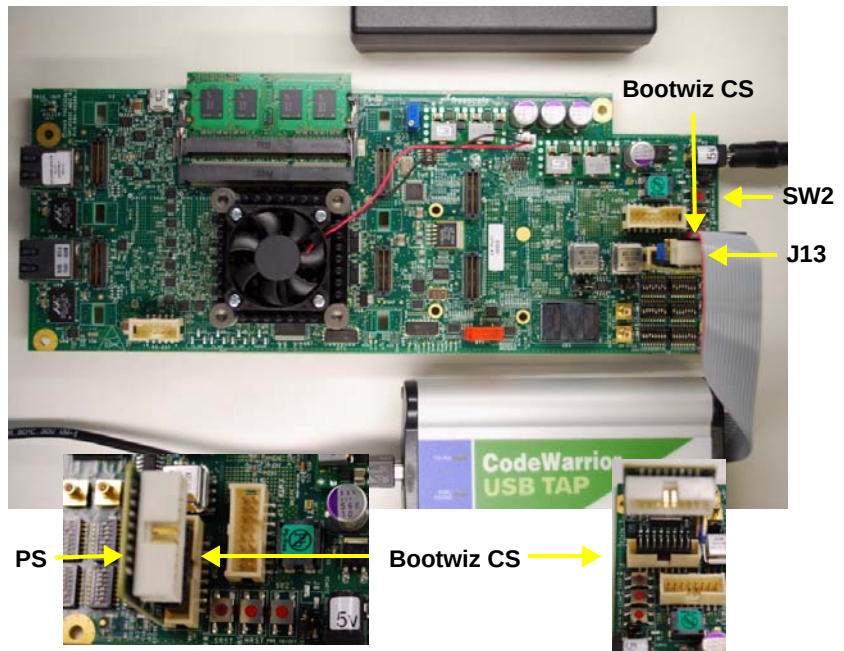
**Procedure 8: Connect CodeWarrior USB TAP to the PB.****CAUTION!**

To avoid damage, follow steps for aligning and connecting the Bootwiz.

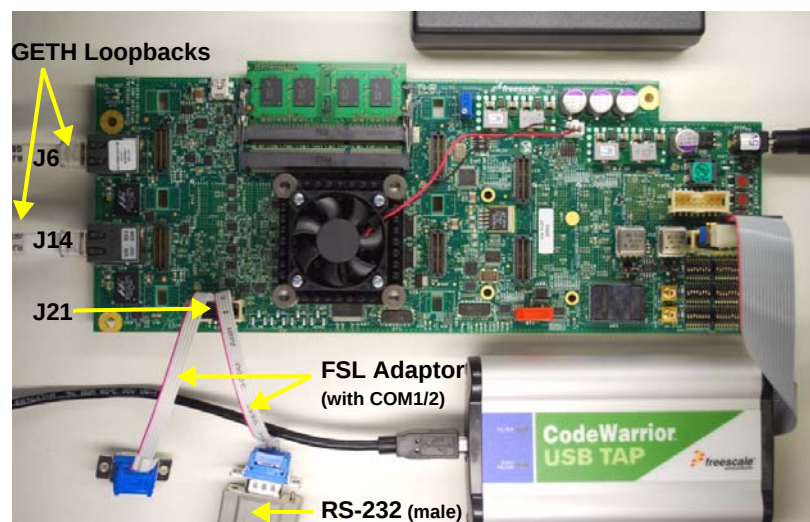
**NOTE!**

Freescale's CodeWarrior USB TAP enables CodeWarrior IDE software to work with the PB.

1. Align Bootwiz module with its CS facing the board's printed "COP" text. The PS must face switches SW5 - SW10.
2. Connect the Bootwiz module to the J13 COP board connector.
3. Attach the USB-TAP cable to the Bootwiz module's J2 connector.
4. Press button SW2 to Power-ON all PB components.
5. Check for completion of the reset sequence.

**Procedure 9: Attach cables per user development needs and planned board use.**

1. Connect FSL adaptor cable to J21 on PB.
2. Connect RS-232 (male) cable to COM1/2 (UART0/1) of FSL adaptor cable.
3. Connect RS-232 (female) to a PC.
4. Connect GETH loopback (shown in picture) or ETH cables with RJ45 connectors to the Ethernet ports:
  - J14 for GETH1
  - J6 for GETH2
5. Continue as per CodeWarrior Kit Configuration Guide instructions.



# 14 SerDes Module Set-ups

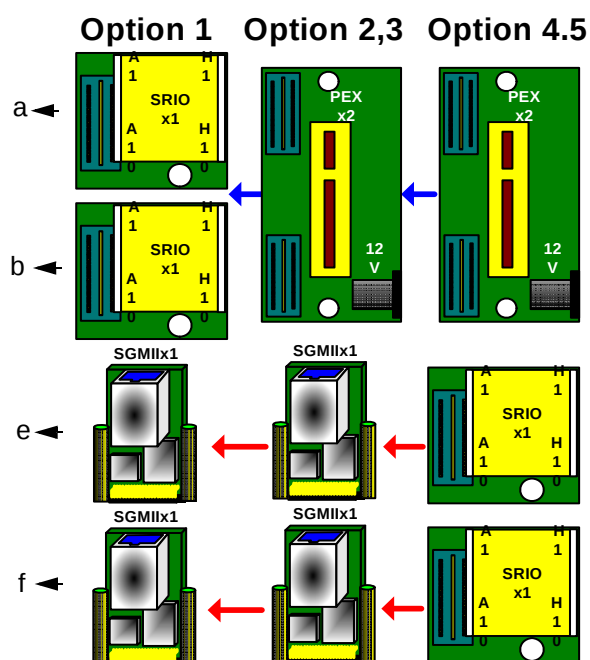
This section details SerDes options

## SerDes Options

1. Select a configuration scenario from the available options
2. Follow the steps for a given option, Options 1 through 5, below.
3. Plug 5V power cable into P2.
4. Press SW2 to Power-ON.

### NOTE!

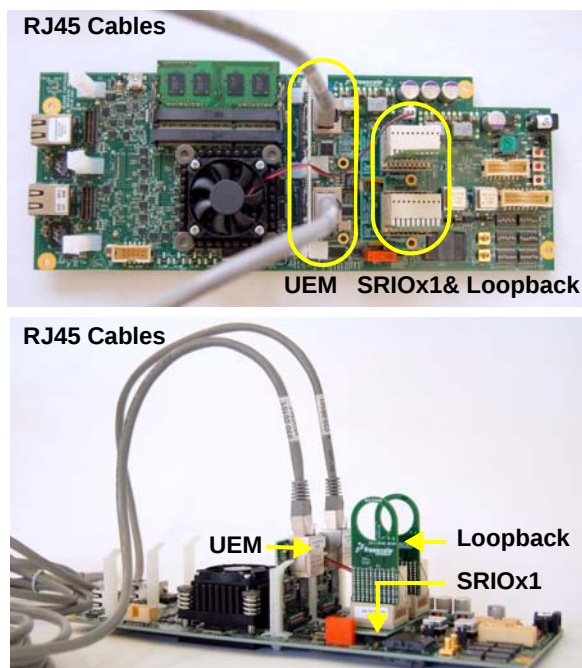
Options 2 through 5: PEX EP board 12V DC power is supplied via the corresponding PEX-expansion module power jack.



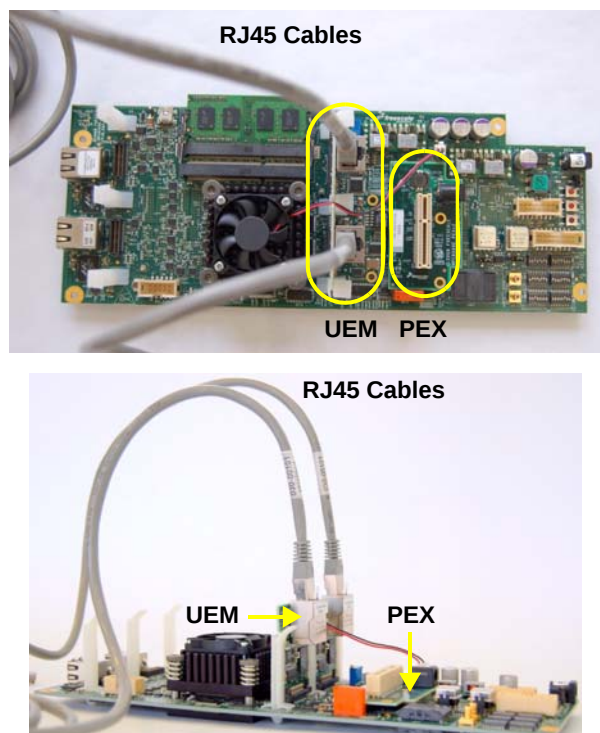
| Option | Lanes    |          |          |          | Frequency Information |
|--------|----------|----------|----------|----------|-----------------------|
|        | f        | e        | b        | a        |                       |
| 1      | SGMII    | SGMII    | x1 SRIO2 | x1 SRIO1 | SRIO at 2.5Gbaud      |
| 2      | SGMII    | SGMII    | -        | x1 PEX   | PEX at 2.5Gbaud       |
| 3      | SGMII    | SGMII    | x2 PEX   |          | PEX at 2.5Gbaud       |
| 4      | x1 SRIO2 | x1 SRIO1 | -        | x1 PEX   | 2.5Gbaud              |
| 5      | x1 SRIO2 | x1 SRIO1 | x2 PEX   |          | 2.5Gbaud              |

**SerDes Option 1: two UEM & two SRIOx1**

- a) Insert UEM (used in SGMII mode) modules into J16 and J7.
- b) Connect ETH RJ45 cables to UEM modules.
- a) Insert SRIOx1 modules into J10 and J17; stabilize with plastic screws.
- b) Insert SRIO loopback into assembled SRIOx1 modules.

**SerDes Option 2: two UEM & one PEXx1 (x1 mode)**

- a) Insert UEM modules into J16 and J7.
- b) Connect ETH RJ45 cables to UEM modules.
- c) Insert PEXx2 into J10 and J17.
- d) PEX slot now available as RC port x1.

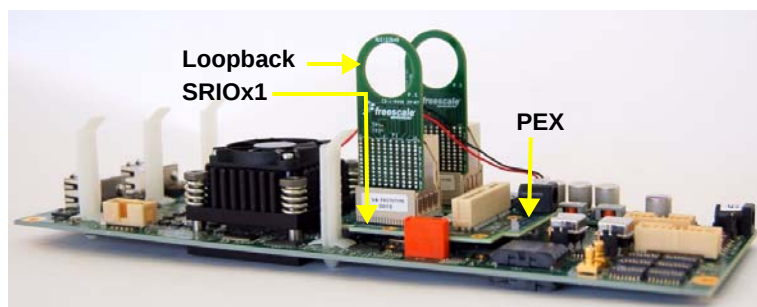
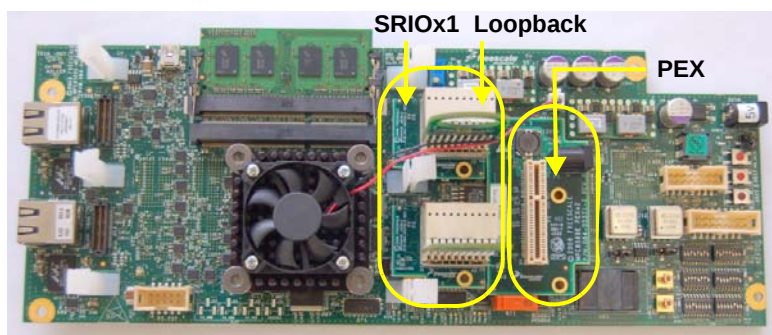
**SerDes Option 3: two UEM & one PEXx2 (x2 mode)**

- a) Repeat first three steps of Option 2.
- b) PEX slot now available as RC port x2.

See SerDes Option 2 photos.

**SerDes Option 4: two SRIOx1 & one PEXx1 (x1 mode)**

- a) Insert SRIOx1 modules into J16 and J17.
- b) Insert SRIO loopback into SRIOx1 modules.
- c) Insert PEXx2 into J10 and J17.
- d) PEX slot now available as RC port x1.

**SerDes Option 5: two SRIOx1 & one PEXx2 (x2 mode)**

- a) Repeat first three steps of Option 4.
- b) PEX slot now available as RC port x2.

See SerDes Option 4 photos.



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