

HD74LS273

Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

REJ03D0473-0300

Rev.3.00

Jul.15.2005

The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

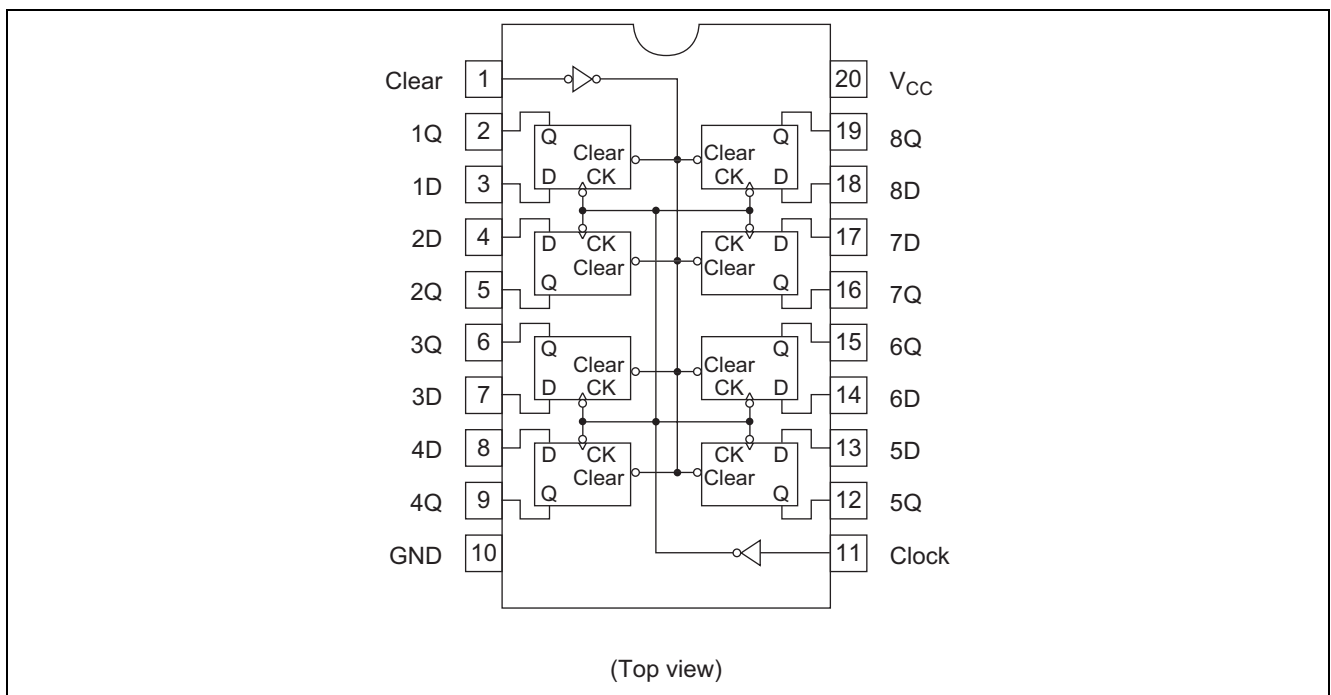
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS273P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS273FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS273RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

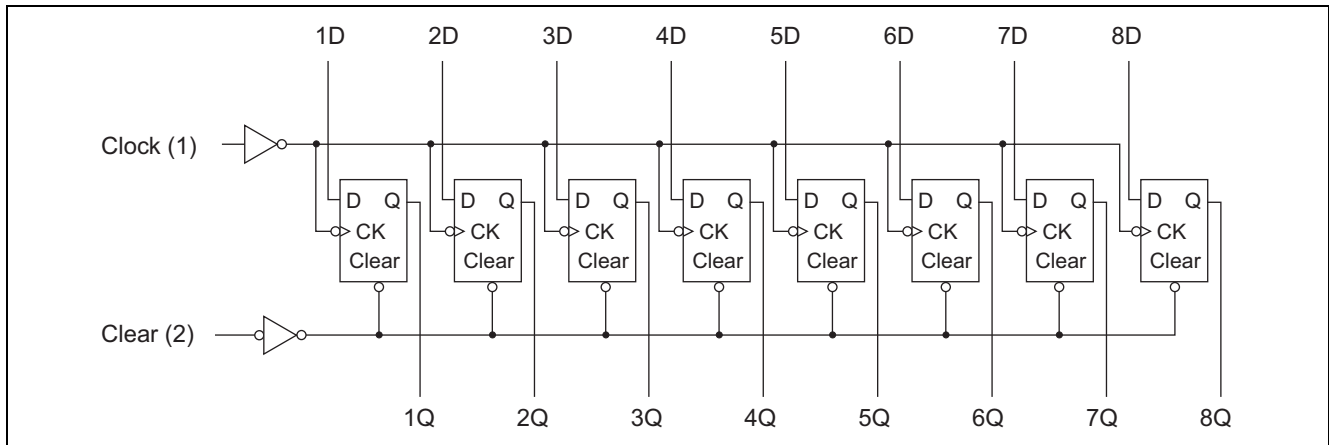
Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

Notes: H; high level, L; low level, X; irrelevant

↑; transition from low to high level

Q₀; level of Q before the indicated steady-state input conditions were established.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	T _{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output current	I _{OH}	—	—	-400	μA
	I _{OL}	—	—	8	mA
Operating temperature	T _{opr}	-20	25	75	°C
Clock frequency	f _{clock}	0	—	30	MHz
Clock pulse width	t _{w (clock)}	20	—	—	ns
Clear pulse width	t _{w (clear)}	20	—	—	ns
Data setup time	t _{su (data)}	20↑	—	—	ns
Clear (inactive-state) setup time	t _{su (clear)}	25↑	—	—	ns
Data hold time	t _{h (data)}	5↑	—	—	ns

Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V _{IH}	2.0	—	—	V	
	V _{IL}	—	—	0.8	V	
Output voltage	V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA
	V _{OL}	—	—	0.5	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V
		—	—	0.4		
						I _{OL} = 8 mA
Input current	I _{IH}	—		20	μA	V _{CC} = 5.25 V, V _I = 2.7 V
	I _{IL}	—		-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	I _I	—		0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
Short-circuit output current	I _{OS}	-20	—	-100	mA	V _{CC} = 5.25 V
Supply current	I _{CC} **	—	17	27	mA	V _{CC} = 5.25 V
Input clamp voltage	V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V is applied to clock.

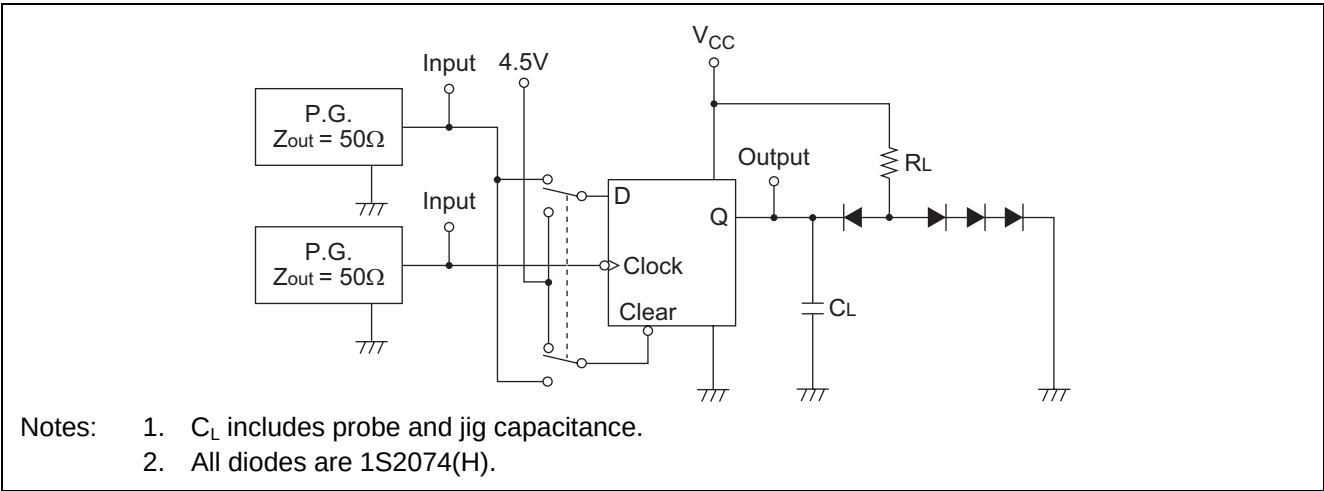
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

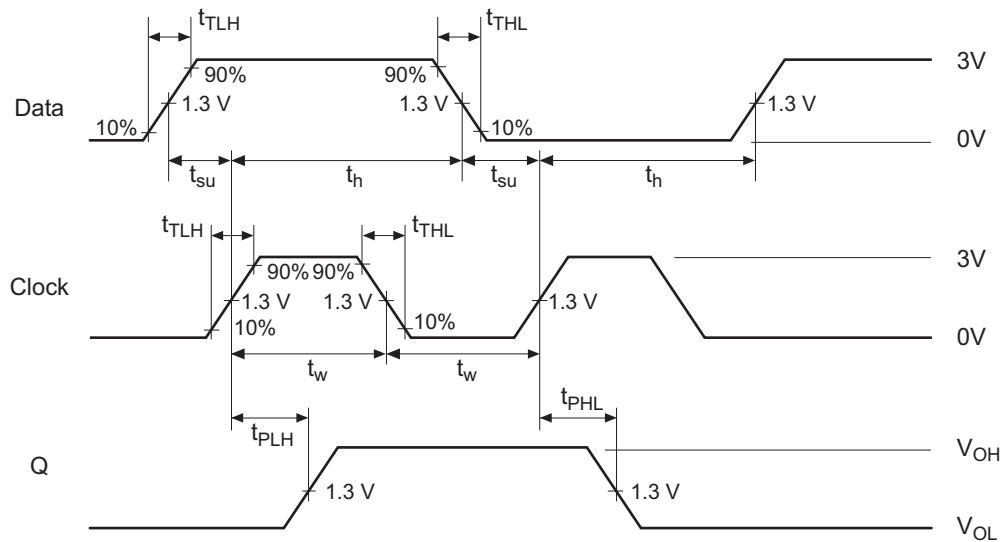
Item	Symbol	Inputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{\max}$	Clock	30	40	—	MHz	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$
Propagation delay time	t_{PHL}	Clear	—	18	27	ns	
	t_{PLH}	Clock	—	17	27		
	t_{PHL}		—	18	27		

Testing Method

Test Circuit

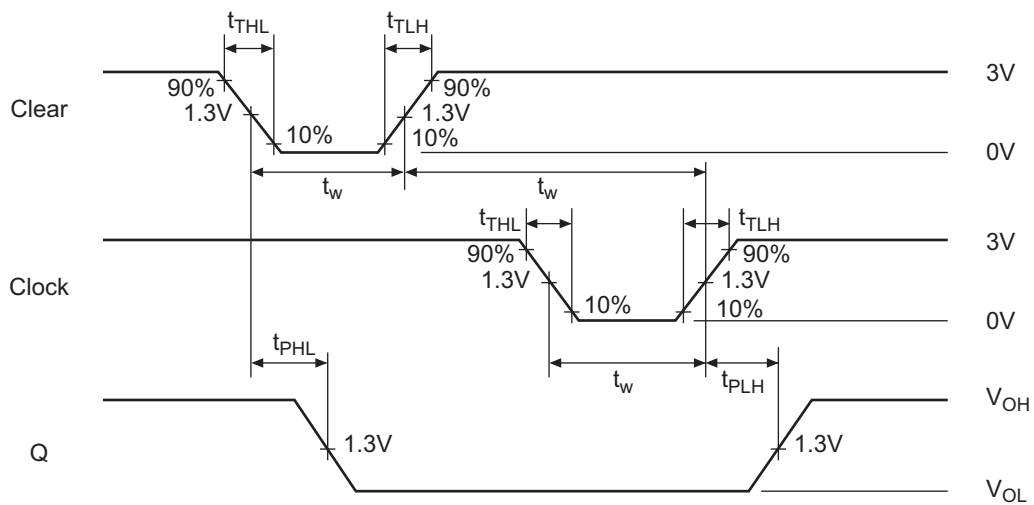


Waveforms 1



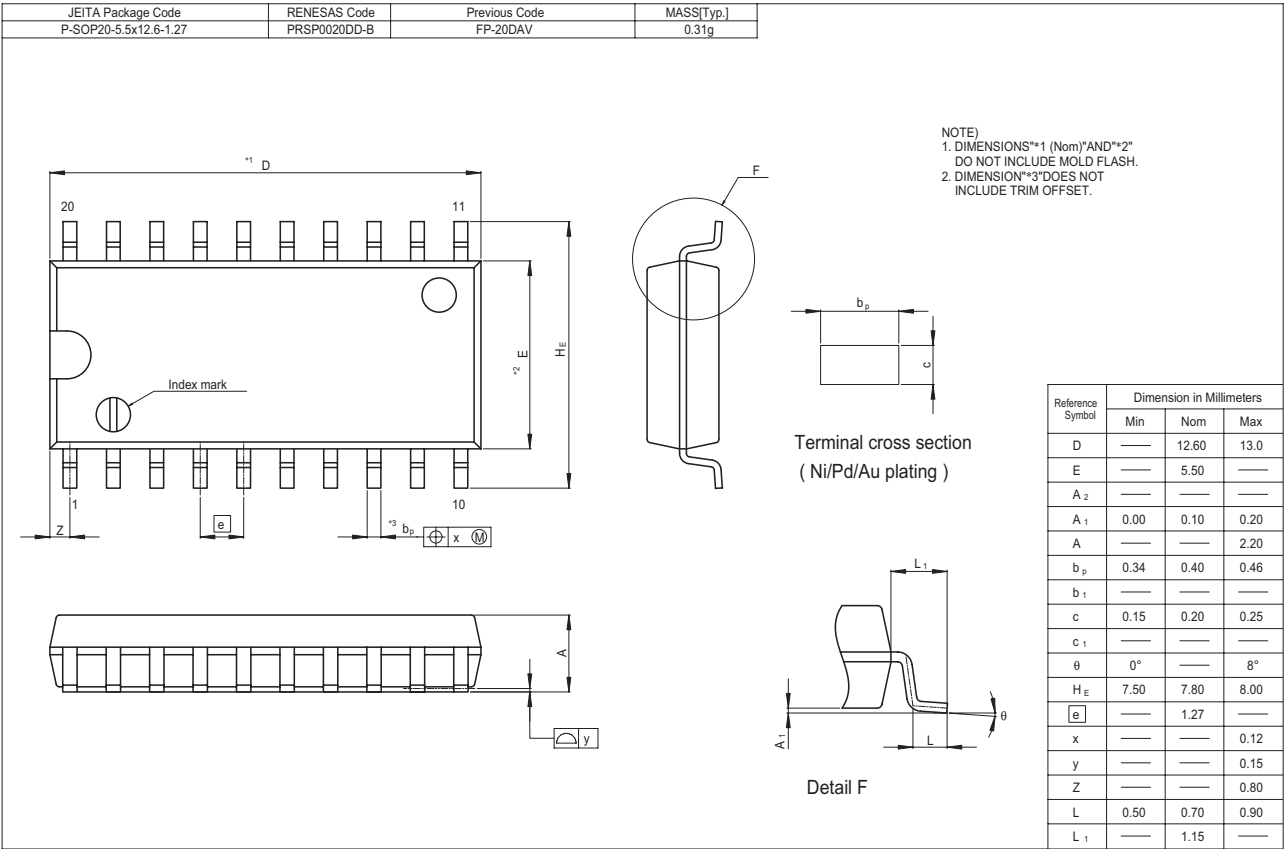
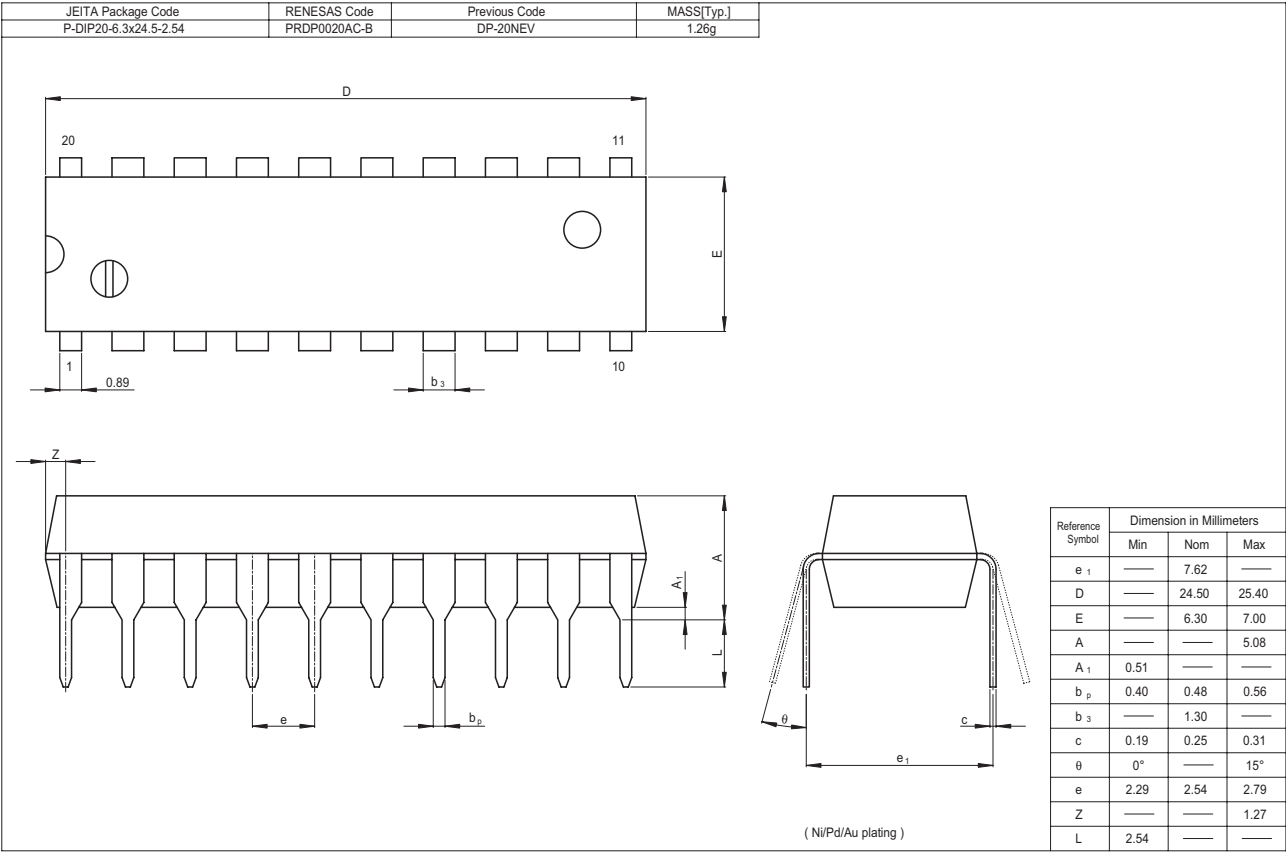
Notes: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns,
 Clock input; PRR = 1 MHz, duty cycle 50%
 Data input; PRR = 500 kHz, duty cycle 50%

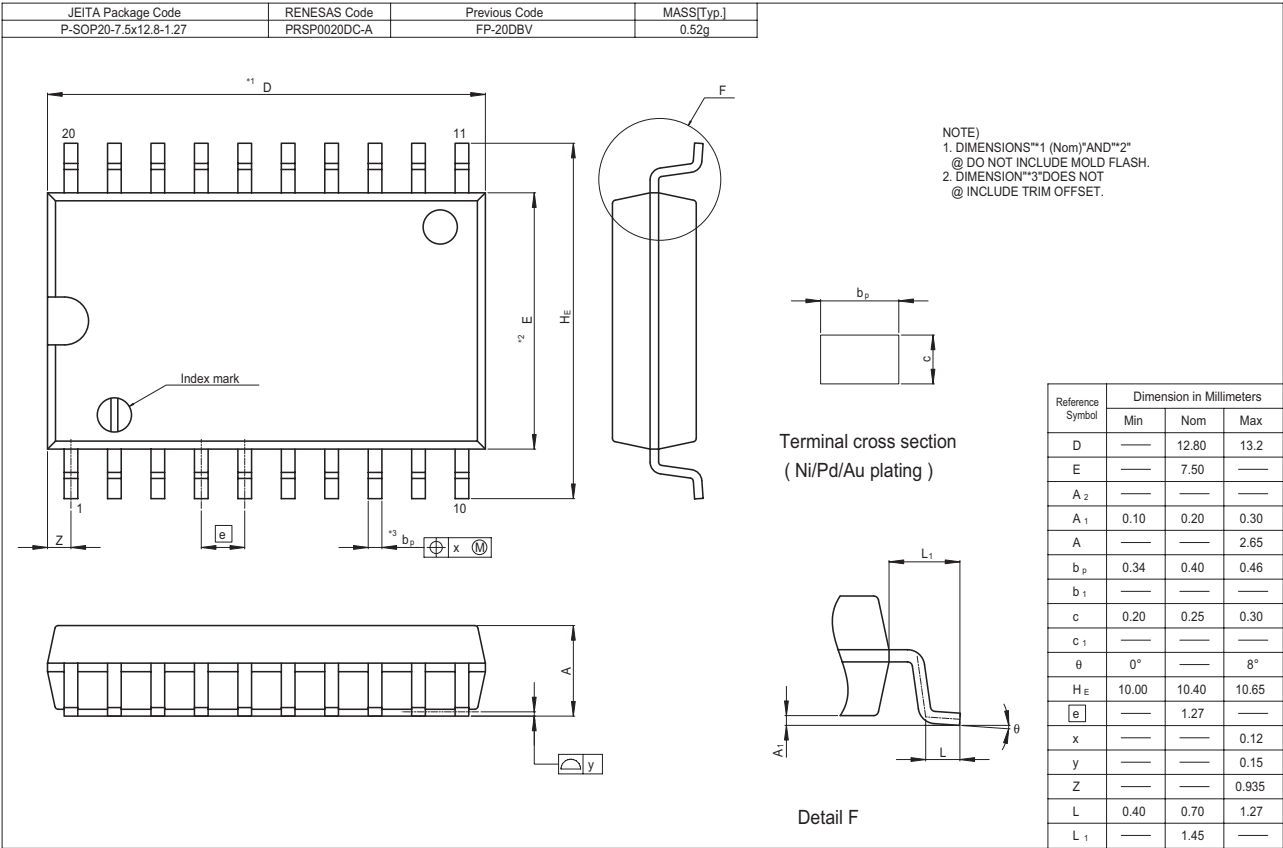
Waveforms 2



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz.

Package Dimensions





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