FAIRCHILD SEMICONDUCTOR®

May 2005

FMS6501
12 Input 9 Output Video Switch Matrix with Input Clamp, Input Bias Circuitry, and Output Drivers

Features

- 12 x 9 Crosspoint Matrix
- Supports SD, PS, and HD 1080i/1080p Video
- Input Clamp / Bias Circuitry
- AC or DC-Coupled Inputs
- AC or DC-Coupled Outputs
- Dual Load(75Ω) Output Drivers with High Impedance Disable
- One-to-One or One-to-Many Input to Output Switching
- Programmable Gain: +6, +7, +8 or +9dB
- I^2C^{TM} Compatible Digital Interface, Standard Mode
- 3.3V or 5V single supply operation
- Lead (Pb) Free SSOP-28 Package

Applications

- Cable and Satellite set top boxes
- TV and HDTV Sets
- A/V Switchers
- Personal Video Recorders (PVR)
- Security / Surveillance
- Video Distribution
- Automotive (In-Cabin Entertainment)

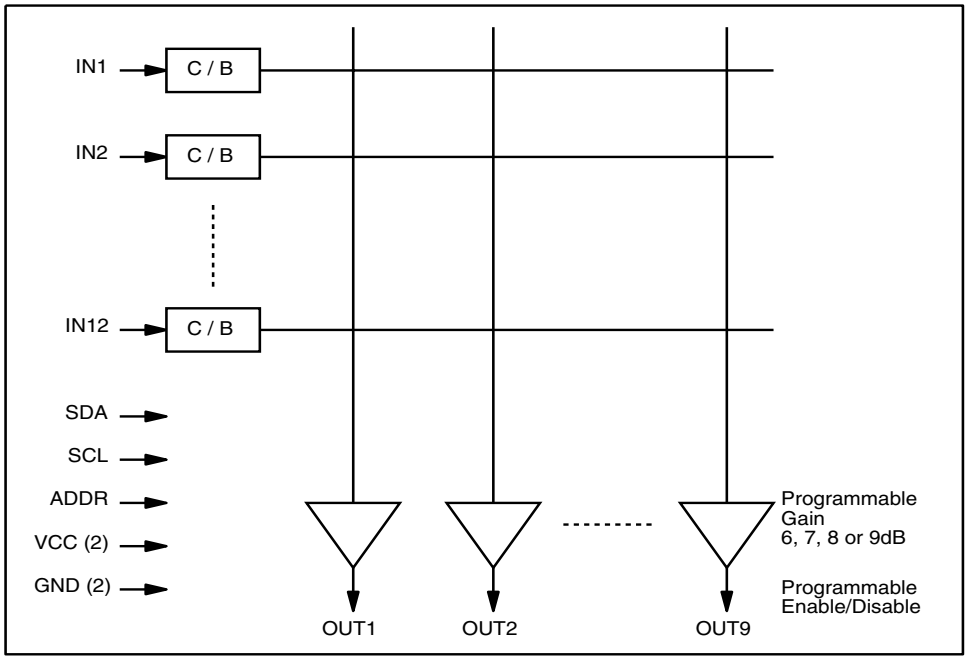
Description

The FMS6501 provides 12 inputs which can be routed to any of 9 outputs. Each input can be routed to one or more outputs but only one input may be routed to any output. The input to output routing is controlled via an I^2C compatible digital interface.

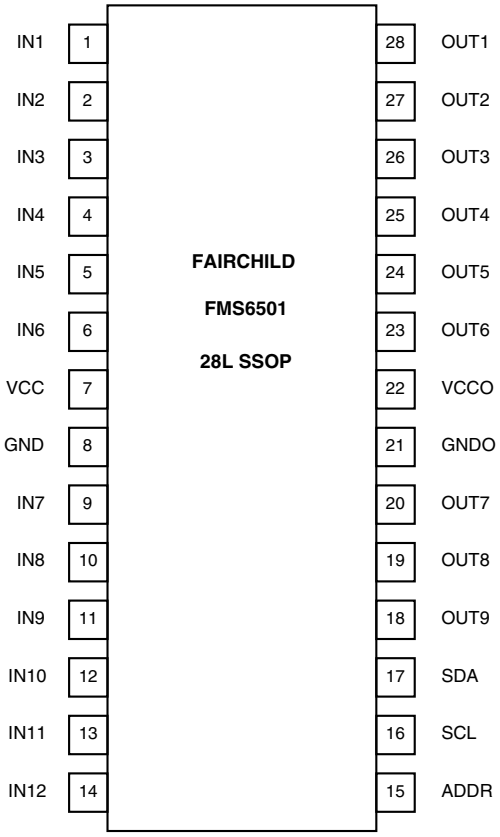
Each input supports an integrated clamp option to set the output sync tip level of video with sync to ~300mV. Alternatively, the input may be internally biased to center signals without sync (Chroma, Pb, Pr) at ~1.25V. These DC output levels are for the 6dB gain setting. Higher gain settings will increase the DC output levels accordingly. The input clamp / bias mode is selected via I^2C.

Unused outputs may be powered down to reduce power dissipation.

Block Diagram



Pin Configuration



Pin Assignments

Pin#	Pin	Type	Description
1	IN1	Input	Input, channel 1
2	IN2	Input	Input, channel 2
3	IN3	Input	Input, channel 3
4	IN4	Input	Input, channel 4
5	IN5	Input	Input, channel 5
6	IN6	Input	Input, channel 6
7	VCC	Input	Positive power supply
8	GND	Input	Must be tied to Ground
9	IN7	Input	Input, channel 7
10	IN8	Input	Input, channel 8
11	IN9	Input	Input, channel 9
12	IN10	Input	Input, channel 10
13	IN11	Input	Input, channel 11
14	IN12	Input	Input, channel 12
15	ADDR	Input	Selects I^2C address. “0” = 0x06 (0000 0110), ‘1” = 0x86 (1000 0110)
16	SCL	Input	Serial Clock for I^2C Port
17	SDA	Input	Serial Data for I^2C Port
18	OUT9	Output	Output, channel 9
19	OUT8	Output	Output, channel 8
20	OUT7	Output	Output, channel 7
21	GNDO	Input	Must be tied to Ground
22	VCCO	Input	Positive power supply for Output Drivers
23	OUT6	Output	Output, channel 6
24	OUT5	Output	Output, channel 5
25	OUT4	Output	Output, channel 4
26	OUT3	Output	Output, channel 3
27	OUT2	Output	Output, channel 2
28	OUT1	Output	Output, channel 1

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{cc} + 0.3	V
Output Current Any One Channel, Do Not Exceed		40	mA

Reliability Information

Parameter	Min.	Typ.	Max.	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance ($Theta_{JA}$), JEDEC Standard Multi-Layer Test Boards, Still Air		50		°C/W

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	0		85	°C
Supply Voltage Range	3.135	5.0	5.25	V

Digital Interface

The I^2C compatible interface is used to program output enables, input to output routing, input clamp / bias and output gain. The I^2C address of the FMS6501 is 0x06 (0000 0110) with the ability to offset it to 0x86 (1000 0110) by tying the ADDR pin high.

Both data and address data of eight bits each are written to the FMS6501 I^2C address to access all the control functions.

There are separate internal addresses for each output. Each output's address includes bits to select an input channel, adjust the output gain, and enable or disable the output amplifier. More than one output can select the same input channel for one-to-many routing. When the outputs are disabled they are placed in a high-impedance state. This allows multiple FMS6501 devices to be paralleled to create a larger switch matrix. Typical output power-up times will be less than 500ns.

The clamp / bias control bits are written to their own internal address since they should always remain the same regardless of signal routing. They are set based on the input signal connected to the FMS6501.

All undefined addresses may be written without effect.

Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Enable	1 bit	Write	0	7	Channel Enable: 1=Enable, 0=Power Down[1]
Gain	2 bits	Write	0	6:5	Channel Gain: 00=6dB, 01=7dB, 10=8dB, 11=9dB
In	5 bits	Write	0	4:0	Input selected to drive this output: 00000=OFF[2], 00001=IN1, 00010=IN2,..., 01100=IN12

Output Control Register MAP

Register Name	Address	Bit 7	Bit 6	Bit5	Bit4[3]	Bit3	Bit2	Bit1	Bit0
OUT1	0x01	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT2	0x02	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT3	0x03	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT4	0x04	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT5	0x05	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT6	0x06	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT7	0x07	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT8	0x08	Enable	Gain1	Gain0	In4	In3	In2	In1	In0
OUT9	0x09	Enable	Gain1	Gain0	In4	In3	In2	In1	In0

Clamp Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Clmp	1 bit	Write	0	7:0	Clamp / Bias selection: 1 = Clamp, 0 = Bias

Clamp Control Register Map

Register Name	Address	Bit 7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLAMP1	0x1D	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1
CLAMP2	0x1E	Resv'd	Resv'd	Resv'd	Resv'd	Clmp12	Clmp11	Clmp10	Clmp9

Notes:

1. Power Down places the output in a high impedance state so multiple FMS6501 devices may be paralleled. Power Down also de-selects any input routed to the specified output.
2. When all inputs are OFF, the amplifier input will be tied to approximately 150mV and the output will go to approximately 300mV with the 6dB gain setting.
3. In4 is provided for forward compatibility and should always be written as '0' in the FMS6501.

DC Electrical Characteristics

T_c = 25°C, V_{cc} = 5V, V_{in} = 1V_{pp}, input bias mode, one-to-one routing, 6dB gain, all inputs AC coupled with 0.1uF, unused inputs AC-terminated through 75Ω to GND, all outputs AC coupled with 220uF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{CC}	Supply Current[1]	No load, all outputs enabled		80	100	mA
V_{OUT}	Video Output Range			2.8		V_{pp}
R_{OFF}	Off Channel Output Impedance	Output disabled		3.0		kΩ
V_{clamp}	DC Output Level[1]	Clamp mode	0.2	0.3	0.4	V
V_{bias}	DC Output Level[1]	Bias mode	1.15	1.25	1.35	V
PSRR	Power Supply Rejection Ratio	All channels, DC		50		dB

AC Electrical Characteristics

T_c = 25°C, V_{cc} = 5V, V_{in} = 1V_{pp}, input bias mode, one-to-one routing, 6dB gain, all inputs AC coupled with 0.1uF, unused inputs AC-terminated through 75Ω to GND, all outputs AC coupled with 220uF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
AV_{SD}	Channel Gain[1] Error	All Channels, All Gain Settings, DC	-0.2	0	+0.2	dB
AV_{STEP}	Gain Step[1]	All Channels, DC	0.9	1	1.1	dB
f_{+1dB}	1dB Peaking Bandwidth	V_{OUT} = 1.4V_{pp}		65		MHz
f_{-1dB}	-1dB Bandwidth	V_{OUT} = 1.4V_{pp}		90		MHz
f_C	-3dB Bandwidth	V_{OUT} = 1.4V_{pp}		115		MHz
dG	Differential Gain	3.58MHz		0.1		%
dP	Differential Phase	3.58MHz		0.2		deg
THD_{SD}	SD Output Distortion	V_{OUT} = 1.4V_{pp}, 5MHz		0.05		%
THD_{HD}	HD Output Distortion	V_{OUT} = 1.4V_{pp}, 22MHz		0.6		%
X_{TALK1}	Input Crosstalk	1MHz, V_{OUT} = 2V_{pp}[2]		-72		dB
X_{TALK2}	Input Crosstalk	15MHz, V_{OUT} = 2V_{pp}[2]		-50		dB
X_{TALK3}	Output Crosstalk	1MHz, V_{OUT} = 2V_{pp}[3]		-68		dB
X_{TALK4}	Output Crosstalk	15MHz, V_{OUT} = 2V_{pp}[3]		-61		dB
X_{TALK5}	Multi-Channel Crosstalk	Standard Video, V_{OUT} = 2V_{pp}[4]		-45		dB
SNR_{SD}	Signal-to-Noise Ratio[5]	NTC-7 weighting, 4.2MHz LP, 100kHz HP		73		dB
V_{NOISE}	Channel Noise	400kHz to 100MHz, Input referred		20		nV/rtHz
AMP_{ON}	Amplifier Recovery Time	Post I^2C programming		300		ns

Notes:

1. 100% tested at 25°C.
2. Adjacent input pair to adjacent output pair. Interfering input is through an open switch.
3. Adjacent input pair to adjacent output pair. Interfering input is through a closed switch.
4. Crosstalk of eight synchronous switching outputs onto single, asynchronous switching output.
5. SNR = 20 * log (714mV / rms noise)

I²C BUS Characteristics

T_c = 25°C, V_{cc} = 5V; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{il}	Digital Input Low[1]	SDA, SCL, ADDR	0		1.5	V
V_{ih}	Digital Input High[1]	SDA, SCL, ADDR	3.0		V_{cc}	V
f_{scl}	Clock Frequency	SCK		100		kHz
tr	Input Rise Time	1.5V to 3V		1000		nS
tf	Input Fall Time	1.5V to 3V		300		nS
t_{low}	Clock Low Period			4.7		uS
t_{high}	Clock High Period			4.0		uS
$t_{SU,DAT}$	Data Set-up Time			300		nS
$t_{HD,DAT}$	Data Hold Time			0		nS
$t_{SU,STO}$	Set-up Time from Clock High to Stop			4		uS
t_{BUF}	Start Set-up Time following a Stop			4.7		uS
$t_{HD,STA}$	Start Hold Time			4		uS
$t_{SU,STA}$	Start Set-up Time following Clock Low to High			4.7		uS

Notes:

1. 100% tested at 25°C

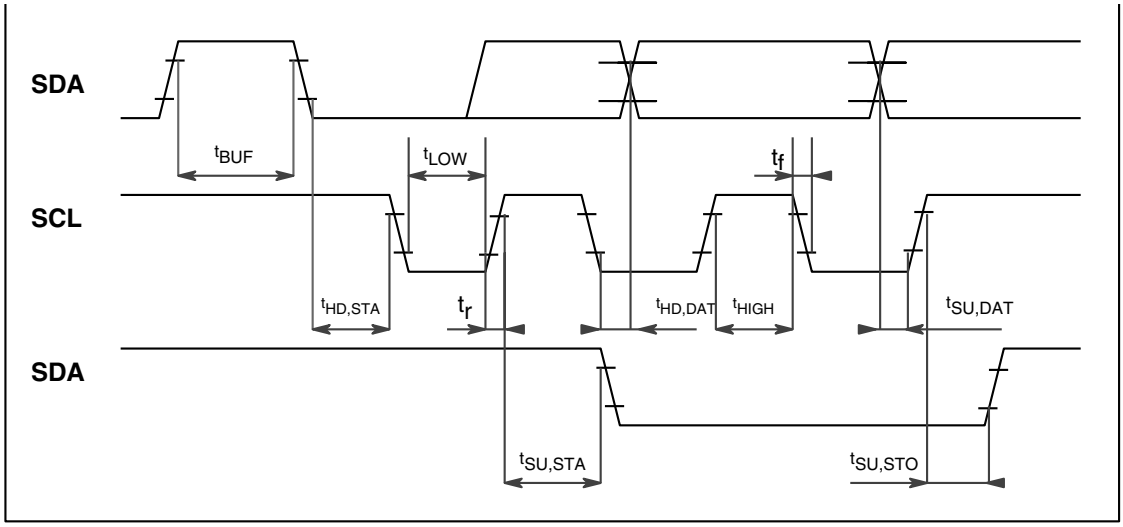


Figure 1: I²C Bus Timing

I²C Interface

Operation

The I²C compatible interface conforms to the I²C spec for Standard Mode. Individual addresses may be written. There is no read capability. The interface consists of two lines. These are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply through an external resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line during this time will be interpreted as a control signal.

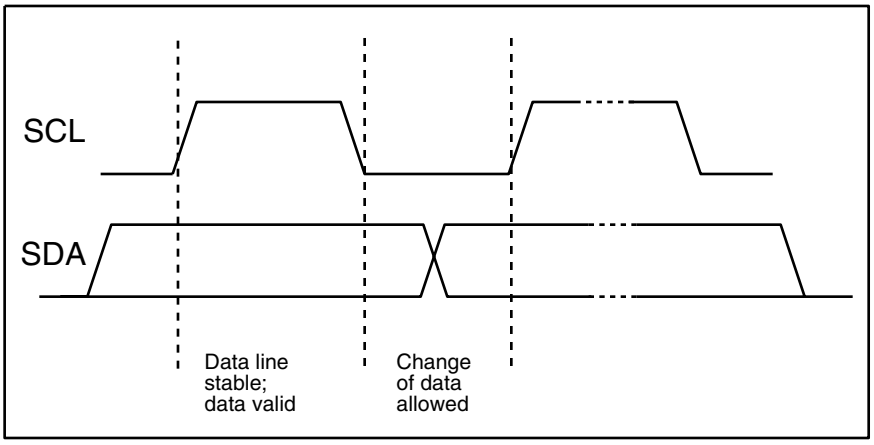


Figure 2: Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH is defined as the stop condition (P).

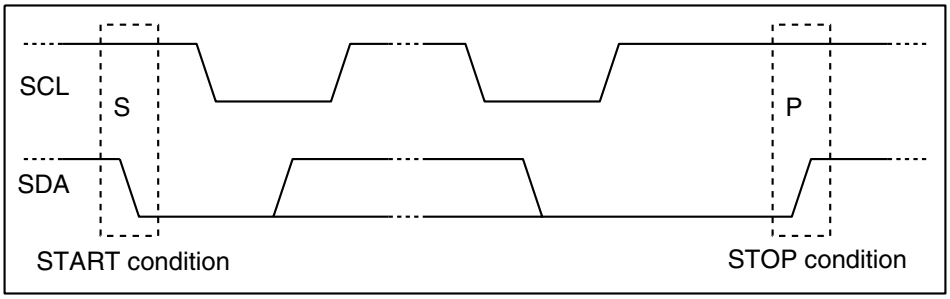


Figure 3: Definition of START and STOP conditions.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

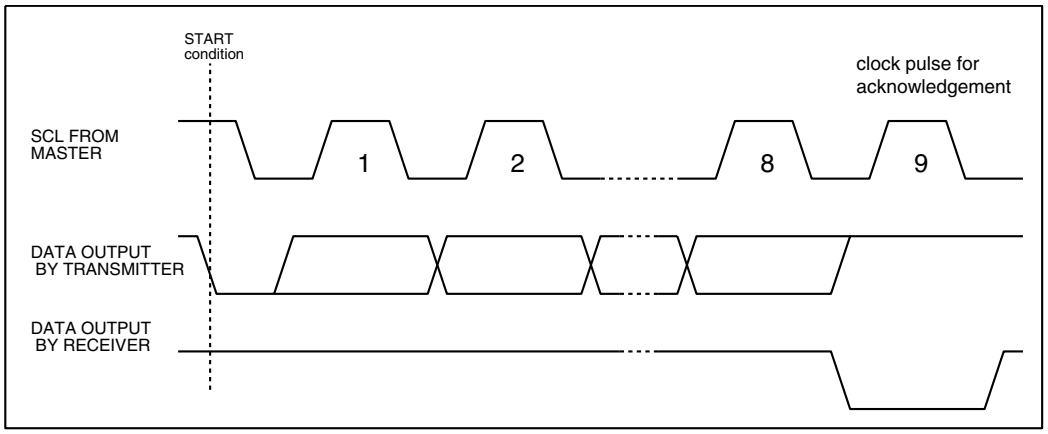


Figure 4: Acknowledgement on the I^2C Bus

I^2C Bus Protocol

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I^2C bus configuration for a data write to the FMS6501 is shown below in figure 5:

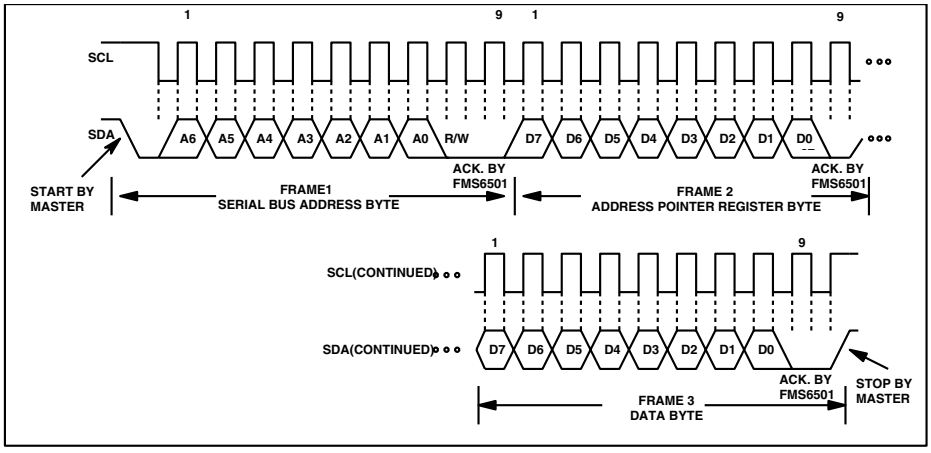


Figure 5: Write a register address to the pointer register, then write data to the selected register

Applications Information

Input Clamp / Bias Circuitry

The FMS6501 can accommodate either AC or DC coupled inputs.

Internal clamping and bias circuitry are provided to support AC coupled inputs. These are selectable through the CLMP bits via the I^2C compatible interface.

For DC coupled inputs, the device should be programmed to use the 'bias' input configuration. In this configuration, the input is internally biased to 625mV through a 100kΩ resistor. Distortion is optimized with the output levels set between 250mV above ground and 500mV below the power supply. These constraints along with the desired channel gain need to be considered when configuring the input signal levels for input DC coupling.

With AC coupled inputs, the FMS6501 uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync, (Y,CV,R,G,B) the lowest voltage at the output pins will be clamped to approximately 300mV above ground when the 6dB gain setting is selected.

If symmetric AC coupled input signals are used, (chroma,Pb,Pr,Cb,Cr) the bias circuit mentioned above can be used to center them within the input common range. The average DC value at the output will be approximately 1.27V with a 6dB gain setting. This value will change, depending upon the selected gain setting.

Gain Setting	Clamp Voltage	Bias Voltage
6dB	300mV	1.27V
7dB	330mV	1.43V
8dB	370mV	1.60V
9dB	420mV	1.80V

The following diagram shows the clamp mode input circuit and the internally controlled voltage at the input pin for AC coupled inputs:

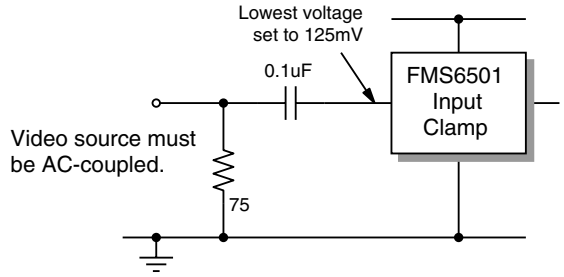


Figure 1. Clamp Mode Input Circuit

The following diagram shows the bias mode input circuit and the internally controlled voltage at the input pin for AC coupled inputs.

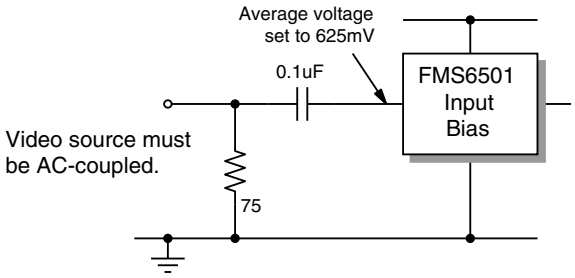


Figure 2. Bias Mode Input Circuit

Output Configuration

The FMS6501 outputs may be either AC or DC coupled. Resistive output loads can be as low as 75Ω, representing a dual, doubly terminated video load. High impedance, capacitive loads up to 20pF can also be driven without loss of signal integrity. For standard 75Ω video loads, a 75Ω matching resistor should be placed in series to allow for a doubly terminated load. DC coupled outputs should be connected as follows:

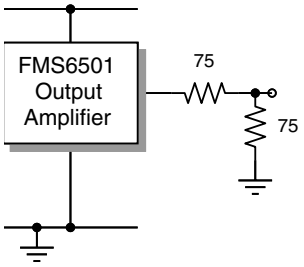


Figure 3. DC-Coupled Load Connection

If multiple, low impedance loads are DC coupled, increased power and thermal issues will need to be addressed. In this case, the use of a multilayer board with a large ground plane to help dissipate heat is recommended. If a 2 layer board is used under these conditions, use of an extended ground plane directly under the device is recommended. This plane should extend at least 0.5" beyond the device. Other PC board layout issues are covered in the Layout Considerations section below.

AC-coupled loads should be configured as follows:

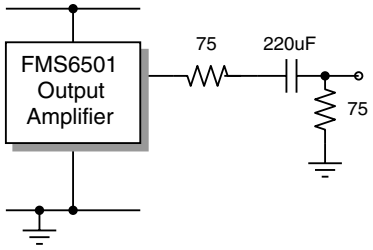


Figure 4. AC-Coupled Load Connection

Thermal issues are significantly reduced with AC coupled outputs, alleviating the need for special PC layout requirements.

Each of the FMS6501 outputs can be independently powered down and placed in a high impedance state with the ENABLE bit. This function can be used to mute video signals, to parallel multiple FMS6501 outputs, or to save power. When the output amplifier is disabled, the high impedance output presents a 3kΩ load to ground. The output amplifier will typically enter and recover from the power down state in less than 300ns after being programmed.

When an output channel is not connected to an input, the input to that particular channels amplifier is forced to approximately 150mV. The output amplifier is still active, unless specifically disabled by the I^2C interface. Voltage output levels will depend on the programmed gain for that channel.

Crosstalk

Crosstalk is an important consideration when using the FMS6501. Input and output crosstalk are defined to represent the two major coupling modes that may be present in a typical application. Input crosstalk is crosstalk in the input pins and switches when the interfering signal drives an open switch. It is dominated by inductive coupling in the package lead frame between adjacent leads. It decreases rapidly as the interfering signal moves farther away from the pin adjacent to the input signal selected. Output crosstalk is coupling from one driven output to another active output. It decreases with increasing load impedance as it is caused mainly by ground and power coupling between output amplifiers. So if a signal is driving an open switch, its crosstalk will be mainly input crosstalk. If it is driving a load through an active output, its crosstalk will be mainly output crosstalk.

Input and output crosstalk measurements are performed with the test configuration shown below:

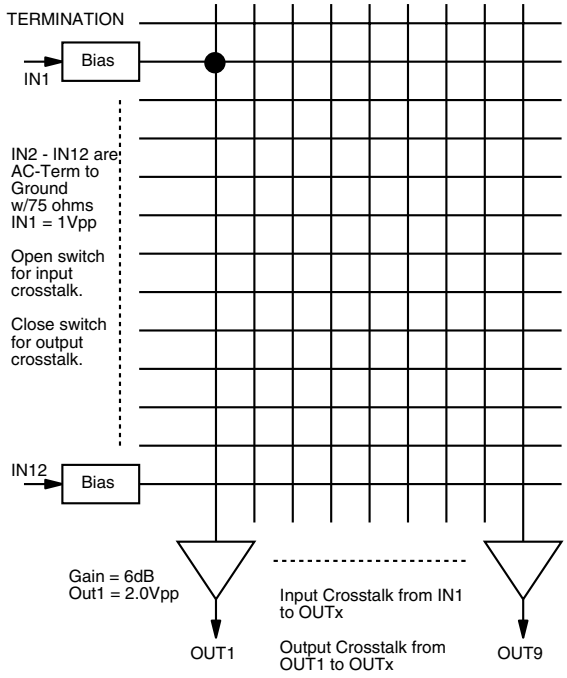


Figure 5: Test Configuration for Crosstalk

For input crosstalk, the switch is open. All inputs are in bias mode. Channel 1 input is driven with a $1V_{pp}$ signal, while all other inputs are AC terminated with 75 ohms. All outputs are enabled, and crosstalk is measured from IN1 to any output.

For output crosstalk, the switch is closed. Crosstalk from OUT1 to any output is measured.

Crosstalk from multiple sources into a given channel was measured with the setup shown in figure 6. Here, Input In1 is driven with a $1V_{pp}$ pulse source and is connected to outputs Out1 to Out8. Input In9 is driven with a secondary, asynchronous gray field video signal, and is connected to Out9. All other inputs are AC terminated with 75 ohms. Crosstalk effects on the gray field are then measured and calculated with respect to a standard $1V_{pp}$ output measured at the load.

If all inputs and outputs are not needed, avoid using adjacent channels where possible to reduce crosstalk. Disable all unused channels to further reduce crosstalk as well as power dissipation.

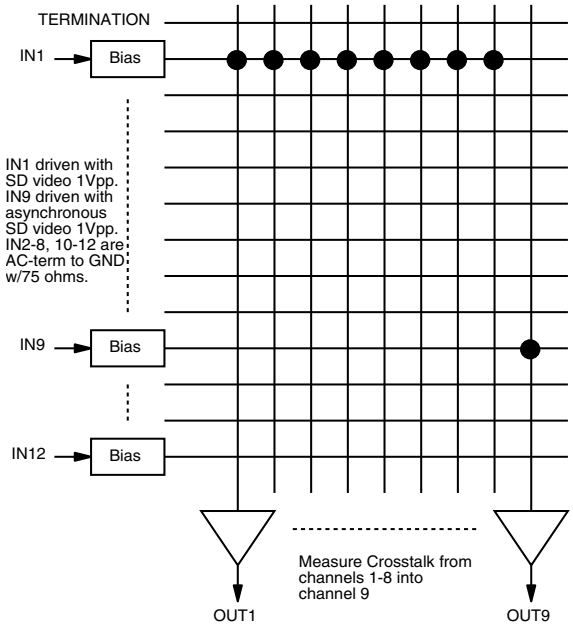


Figure 6: Test Configuration for Multi-Channel Crosstalk

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6501DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6501DEMO is a 4-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 10μF and 0.1μF bypass capacitors
- Place the 10μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.
- Layout channel connections to reduce mutual trace inductance
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs.

If using multiple, low impedance DC coupled outputs, special layout techniques may be employed to help dissipate heat.

If a multilayer board is used, a large ground plane directly under the device will help reduce package case temperature.

For dual layer boards, an extended plane can be used.

Worse case additional die power due to DC loading can be estimated at ($V_{cc}^2/4R_{load}$) per output channel. This assumes a constant DC output voltage of $V_{cc}/2$. For 5V V_{cc} with a dual DC video load, add 25/(4*75) = 83mW, per channel.

Applications for the FMS6501 Video Switch Matrix

The increased demand for consumer multimedia systems has created a large challenge for system designers to provide cost-effective solutions to capitalize on the growth potential in graphics display technologies. These applications will require cost effective video switching and filtering solutions to deploy high-quality display technologies rapidly and effectively to the target audience. Areas of specific interest include HDTV, Media Centers, and Automotive Infotainment(includes navigation, in cabin entertainment, and back up camera). In all cases, the advantages the integrated video switch matrix provides are high quality video switching specific to the application as well as video input clamps and on chip low impedance output cable drivers with switchable gain.

Generally the largest application for a video switch is for the front end of an HDTV. This is used to take multiple inputs and route them to their appropriate signal paths (main picture and picture in picture - PiP). These are normally routed into ADCs that are followed by decoders. There are many different technologies for HDTV including: LCD,Plasma, and CRT that have similar analog switching circuitry.

An example of a potential HDTV application is shown in figure 7 below. This system combines a video switch matrix and 2 - three channel switchable anti-aliasing filters. This is done as there are two 3-channel signal paths in the system - One is for the main picture, and the other is the path for “Picture in Picture”.

VIPDEMO™ Control Software

The FMS6501 is configured via an I^2C compatible digital interface. In order to facilitate ease of demonstration, Fairchild Semiconductor had developed the VIPDEMO™ GUI based control software to write to the FMS6501 register map. This software is included when ordering an FMS6501DEMO kit. Also included is a Parallel port I^2C adapter and an interface cable to connect to the demo board. Besides using the full FMS6501 interface, the VIPDEMO™ can also be used to control single register read and writes for I^2C.

Figures 8 and 9 below show the control panel for the VIPDEMO™ control software and the FMS6501 device evaluation board.

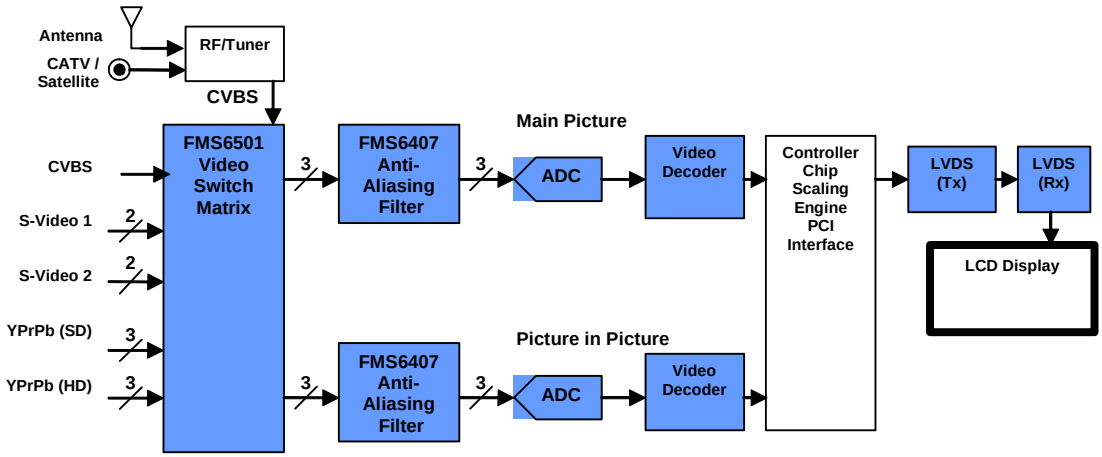


Figure 7: HDTV Application using the FMS6501 Video Switch Matrix

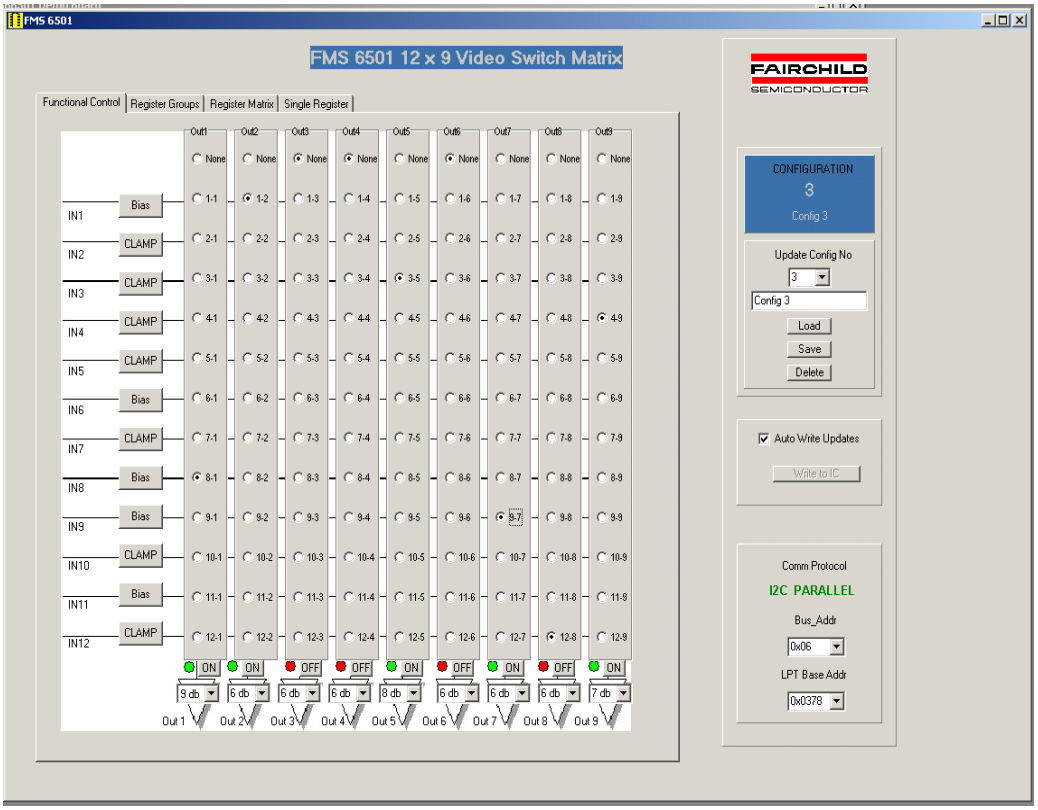


Figure 8: Control Panel for VIPDEMO™ Control Software

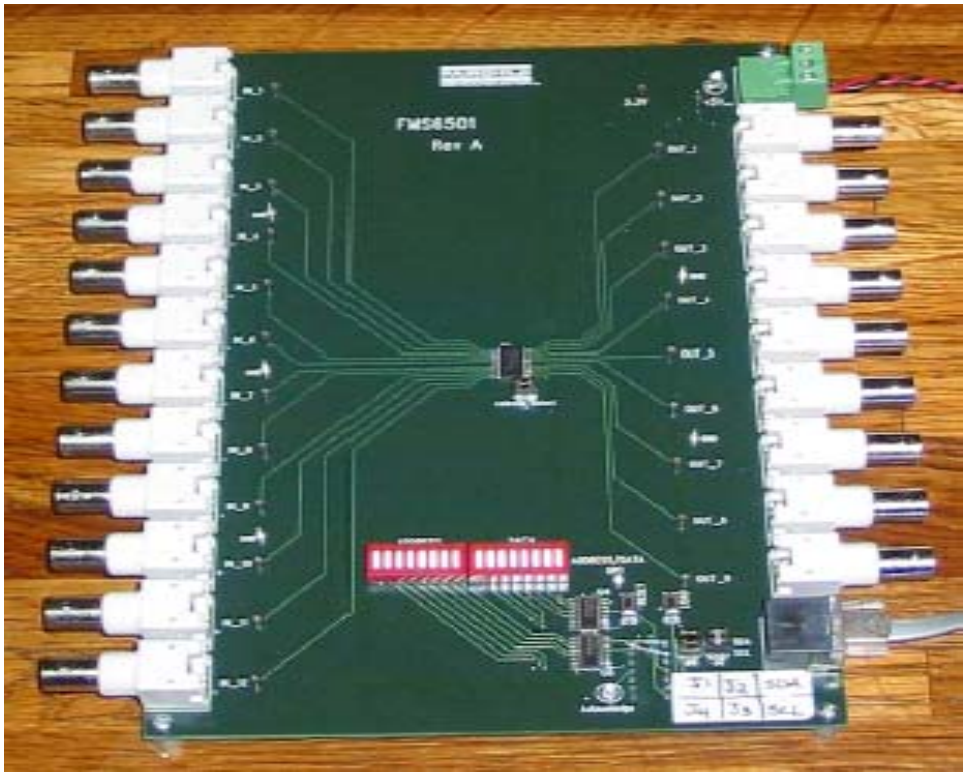
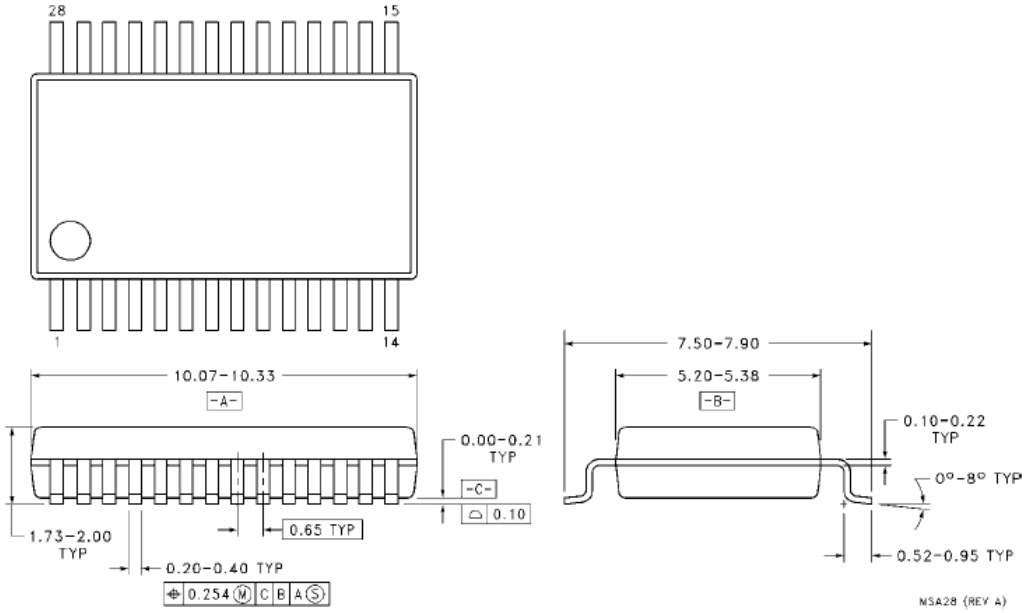


Figure 9: FMS6501 Evaluation Board for use with the VIPDEMO™ Control Software.

Mechanical Dimensions

SSOP-28



Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty
FMS6501	FMS6501MSA28	Yes	SSOP-28	Rail	47
FMS6501	FMS6501MSA28X	Yes	SSOP-28	Reel	2000

Temperature range for all parts: 0°C to 85°C.

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Bottomless™	FASTr™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
CoolFET™	FPS™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	FRFET™	MicroPak™	QS™	SyncFET™
DOME™	GlobalOptoisolator™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
EcoSPARK™	GTO™	MSX™	Quiet Series™	TINYOPTO™
E²CMOS™	HiSeC™	MSXPro™	RapidConfigure™	TruTranslation™
EnSigna™	I²C™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	UltraFET®
Across the board. Around the world.™		OPTOLOGIC®	SMART START™	VCX™
The Power Franchise™		OPTOPLANAR™	SPM™	
Programmable Active Droop™		PACMAN™	Stealth™	

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PRODUCT STATUS DEFINITIONS

Definition of Terms

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