



# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## General Description

The MAX4249–MAX4257 low-noise, low-distortion operational amplifiers offer Rail-to-Rail® outputs and single-supply operation down to 2.4V. They draw 400µA of quiescent supply current per amplifier while featuring ultra-low distortion (0.0002% THD), as well as low input voltage-noise density (7.9nV/√Hz) and low input current-noise density (0.5fA/√Hz). These features make the devices an ideal choice for portable/battery-powered applications that require low distortion and/or low noise.

For additional power conservation, the MAX4249/MAX4251/MAX4253/MAX4256 offer a low-power shutdown mode that reduces supply current to 0.5µA and puts the amplifiers' outputs into a high-impedance state. The MAX4249–MAX4257's outputs swing rail-to-rail and their input common-mode voltage range includes ground. The MAX4250–MAX4254 are unity-gain stable with a gain-bandwidth product of 3MHz. The MAX4249/MAX4255/MAX4256/MAX4257 are internally compensated for gains of 10V/V or greater with a gain-bandwidth product of 22MHz. The single MAX4250/MAX4255 are available in space-saving 5-pin SOT23 packages. The MAX4252 is available in an 8-pin ultra chip-scale package (UCSP™) and the MAX4253 is available in a 10-pin UCSP.

## Applications

Wireless Communications Devices  
PA Control  
Portable/Battery-Powered Equipment  
Medical Instrumentation  
ADC Buffers  
Digital Scales/Strain Gauges

## Features

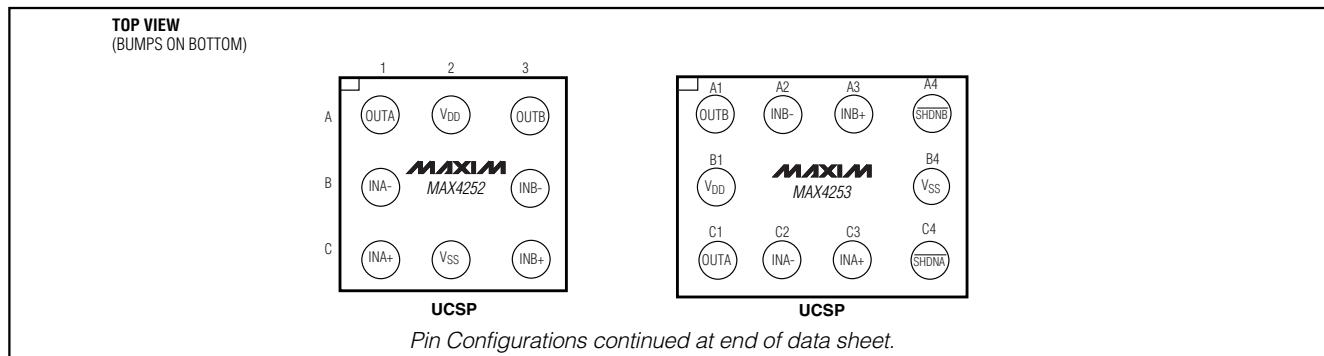
- ◆ Available in Space-Saving UCSP, SOT23, and µMAX Packages
- ◆ Low Distortion: 0.0002% THD (1kΩ load)
- ◆ 400µA Quiescent Supply Current per Amplifier
- ◆ Single-Supply Operation from 2.4V to 5.5V
- ◆ Input Common-Mode Voltage Range Includes Ground
- ◆ Outputs Swing Within 8mV of Rails with a 10kΩ Load
- ◆ 3MHz GBW Product, Unity-Gain Stable (MAX4250–MAX4254)  
22MHz GBW Product, Stable with  $A_V \geq 10V/V$  (MAX4249/MAX4255/MAX4256/MAX4257)
- ◆ Excellent DC Characteristics  
 $V_{OS} = 70\mu V$   
 $I_{BIAS} = 1pA$   
Large-Signal Voltage Gain = 116dB
- ◆ Low-Power Shutdown Mode:  
Reduces Supply Current to 0.5µA  
Places Outputs in a High-Impedance State
- ◆ 400pF Capacitive-Load Handling Capability

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4249ESD	-40°C to +85°C	14 SO	—
MAX4249EUB	-40°C to +85°C	10 µMAX	—
MAX4250EUK-T	-40°C to +85°C	5 SOT23-5	ACCI

Ordering Information continued at end of data sheet.  
Selector Guide appears at end of data sheet.

## Pin Configurations



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

UCSP is a trademark of Maxim Integrated Products, Inc.



Maxim Integrated Products 1

**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

MAX4249–MAX4257

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage ( $V_{DD}$  to  $V_{SS}$ ) .....+6.0V to -0.3V  
 Analog Input Voltage ( $IN_+$ ,  $IN_-$ )....( $V_{DD} + 0.3V$ ) to ( $V_{SS} - 0.3V$ )  
 $\overline{SHDN}$  Input Voltage .....6.0V to ( $V_{SS} - 0.3V$ )  
 Output Short-Circuit Duration to Either Supply .....Continuous  
 Continuous Power Dissipation ( $T_A = +70^\circ C$ )  
   5-Pin SOT23 (derate 7.1mW/ $^\circ C$  above  $+70^\circ C$ ) .....571mW  
   8-Pin  $\mu$ MAX (derate 4.5mW/ $^\circ C$  above  $+70^\circ C$ ) .....362mW  
   8-Pin SO (derate 5.88mW/ $^\circ C$  above  $+70^\circ C$ ) .....471mW  
   8-Pin UCSP (derate 4.7mW/ $^\circ C$  above  $+70^\circ C$ ) .....379mW  
   10-Pin UCSP (derate 6.1mW/ $^\circ C$  above  $+70^\circ C$ ) .....484mW

10-Pin  $\mu$ MAX (derate 5.6mW/ $^\circ C$  above  $+70^\circ C$ ) .....444mW  
 14-Pin SO (derate 8.33mW/ $^\circ C$  above  $+70^\circ C$ ) .....667mW  
 Operating Temperature Range .....-40 $^\circ C$  to +85 $^\circ C$   
 Junction Temperature .....+150 $^\circ C$   
 Storage Temperature Range .....-65 $^\circ C$  to +150 $^\circ C$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ C$   
 Bump Temperature (soldering) (Note 1)  
   Infrared (15s) .....+220 $^\circ C$   
   Vapor Phase (60s) .....+215 $^\circ C$

**Note 1:** This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection Reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = 5V$ ,  $V_{SS} = 0$ ,  $V_{CM} = 0$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ ,  $\overline{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	(Note 4)		2.4		5.5	V
Quiescent Supply Current Per Amplifier	$I_Q$	Normal mode	$V_{DD} = 3V$		400		$\mu A$
			$V_{DD} = 5V$		420	575	
			$V_{DD} = 5V$ , UCSP only		420	655	
		Shutdown mode ( $\overline{SHDN} = V_{SS}$ ) (Note 2)			0.5	1.5	
Input Offset Voltage (Note 5)	$V_{OS}$				$\pm 0.07$	$\pm 0.75$	mV
Input Offset Voltage Tempco	$TCV_{OS}$				0.3		$\mu V/^\circ C$
Input Bias Current	$I_B$	(Note 6)			$\pm 1$	$\pm 100$	pA
Input Offset Current	$I_{OS}$	(Note 6)			$\pm 1$	$\pm 100$	pA
Differential Input Resistance	$R_{IN}$				1000		G $\Omega$
Input Common-Mode Voltage Range	$V_{CM}$	Guaranteed by CMRR test		-0.2		$V_{DD} - 1.1$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} - 0.2V \leq V_{CM} \leq V_{DD} - 1.1V$		70	115		dB
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.4$ to $5.5V$		75	100		dB
Large-Signal Voltage Gain	$A_v$	$R_L = 10k\Omega$ to $V_{DD}/2$ ; $V_{OUT} = 25mV$ to $V_{DD} - 4.97V$		80	116		dB
		$R_L = 1k\Omega$ to $V_{DD}/2$ ; $V_{OUT} = 150V$ to $V_{DD} - 4.75V$		80	112		
Output Voltage Swing	$V_{OUT}$	$ V_{IN+} - V_{IN-}  \geq 10mV$ $R_L = 10k\Omega$ to $V_{DD}/2$	$V_{DD} - V_{OH}$		8	25	mV
			$V_{OL} - V_{SS}$		7	20	

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

MAX4249-MAX4257

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 5V$ ,  $V_{SS} = 0$ ,  $V_{CM} = 0$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ ,  $\overline{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	$V_{OUT}$	$ V_{IN+} - V_{IN-}  \geq 10mV$ , $R_L = 1k\Omega$ to $V_{DD}/2$	$V_{DD} - V_{OH}$ $V_{OL} - V_{SS}$		77 47	200 100	mV
Output Short-Circuit Current	$I_{SC}$				68		mA
Output Leakage Current	$I_{LEAK}$	Shutdown mode ( $\overline{SHDN} = V_{SS}$ ), $V_{OUT} = V_{SS}$ to $V_{DD}$ (Note 2)			0.001	1.0	$\mu A$
$\overline{SHDN}$ Logic Low	$V_{IL}$	(Note 2)				$0.2 \times V_{DD}$	V
$\overline{SHDN}$ Logic High	$V_{IH}$	(Note 2)		$0.8 \times V_{DD}$			V
$\overline{SHDN}$ Input Current	$I_{IL}/I_{IH}$	$\overline{SHDN} = V_{SS} = V_{DD}$ (Note 2)			0.5	1.5	$\mu A$
Input Capacitance					11		pF
Gain-Bandwidth Product	GBW	MAX4250-MAX4254			3		MHz
		MAX4249/MAX4255/MAX4256/MAX4257			22		
Slew Rate	SR	MAX4250-MAX4254			0.3		V/ $\mu s$
		MAX4249/MAX4255/MAX4256/MAX4257			2.1		
Peak-to-Peak Input-Noise Voltage	$e_{nP-P}$	$f = 0.1Hz$ to $10Hz$			760		nV <sub>P-P</sub>
Input Voltage-Noise Density	$e_n$	$f = 10Hz$			2.7		nV/ $\sqrt{Hz}$
		$f = 1kHz$			8.9		
		$f = 30kHz$			7.9		
Input Current-Noise Density	$i_n$	$f = 1kHz$			0.5		fA/ $\sqrt{Hz}$
Total Harmonic Distortion Plus Noise	THD + N	MAX4250-MAX4254 $A_V = 1V/V$ , $V_{OUT} = 2V_{P-P}$ , $R_L = 1k\Omega$ to GND (Note 7)	$f = 1kHz$		0.0004		%
			$f = 20kHz$		0.006		
		MAX4249/MAX4255/ MAX4256/MAX4257 $A_V = 1V/V$ , $V_{OUT} = 2V_{P-P}$ , $R_L = 1k\Omega$ to GND (Note 7)	$f = 1kHz$		0.0012		
			$f = 20kHz$		0.007		
Capacitive-Load Stability		No sustained oscillations			400		pF
Gain Margin	GM	MAX4250-MAX4254, $A_V = 1V/V$			10		dB
		MAX4249/MAX4255/MAX4256/MAX4257, $A_V = 10V/V$			12.5		
Phase Margin	$\Phi_M$	MAX4250-MAX4254, $A_V = 1V/V$			74		degrees
		MAX4249/MAX4255/MAX4256/MAX4257, $A_V = 10V/V$			68		

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 5V$ ,  $V_{SS} = 0$ ,  $V_{CM} = 0$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ ,  $\overline{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Settling Time		To 0.01%, $V_{OUT} = 2V$ step	MAX4250-MAX4254		6.7		$\mu s$
			MAX4249/MAX4255/ MAX4256/MAX4257		1.6		
Delay Time to Shutdown	$t_{SH}$	$I_{VDD} = 5\%$ of normal operation	MAX4251/MAX4253		0.8		$\mu s$
			MAX4249/MAX4256		1.2		
Delay Time to Enable	$t_{EN}$	$V_{OUT} = 2.5V$ , $V_{OUT}$ settles to 0.1%	MAX4251/MAX4253		8		$\mu s$
			MAX4249/MAX4256		3.5		
Power-Up Delay Time	$t_{PU}$	$V_{DD} = 0$ to $5V$ step, $V_{OUT}$ stable to 0.1%			6		$\mu s$

**Note 2:**  $\overline{SHDN}$  is available on the MAX4249/MAX4251/MAX4253/MAX4256 only.

**Note 3:** All device specifications are 100% tested at  $T_A = +25^\circ C$ . Limits over temperature are guaranteed by design.

**Note 4:** Guaranteed by the PSRR test.

**Note 5:** Offset voltage prior to reflow on the UCSP.

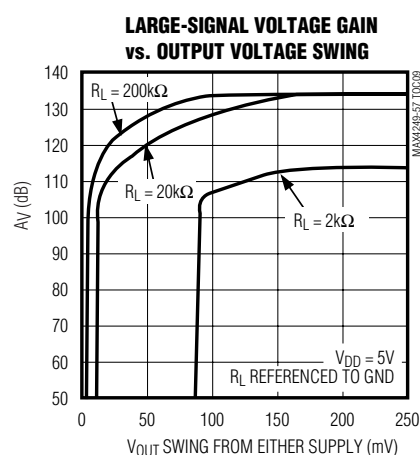
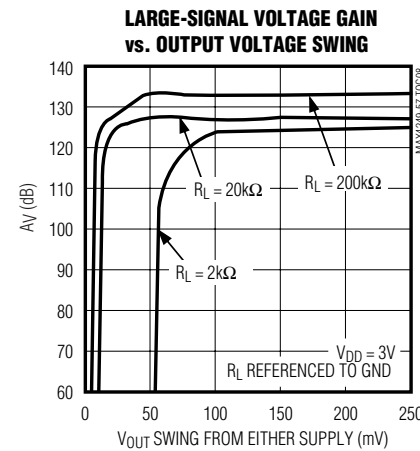
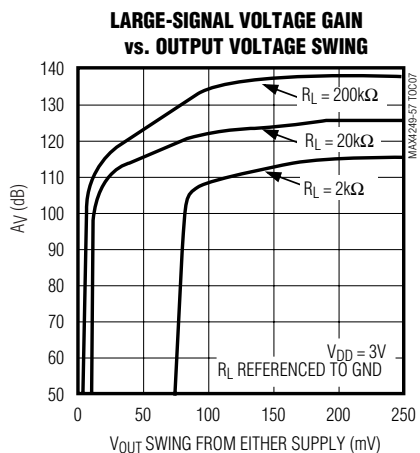
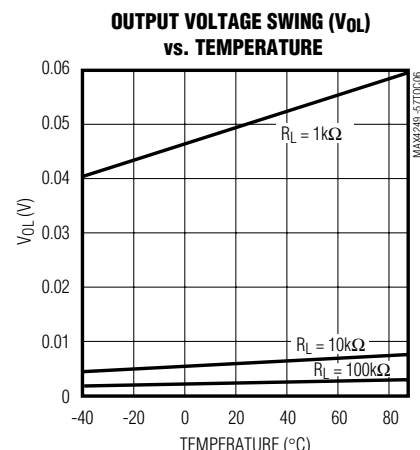
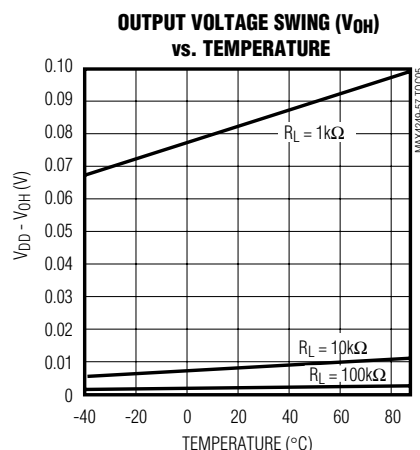
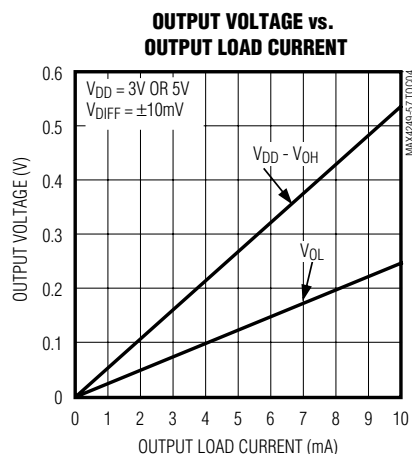
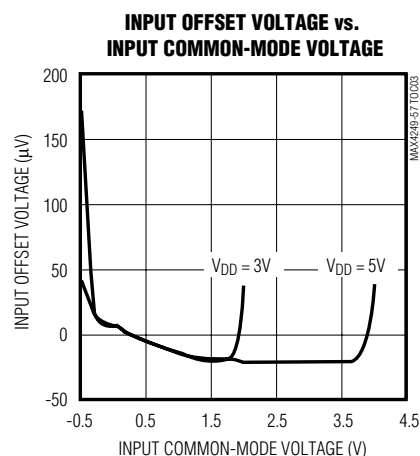
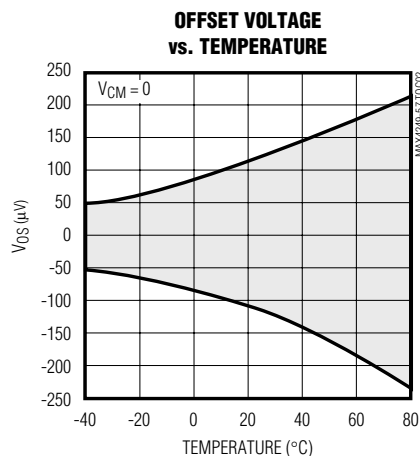
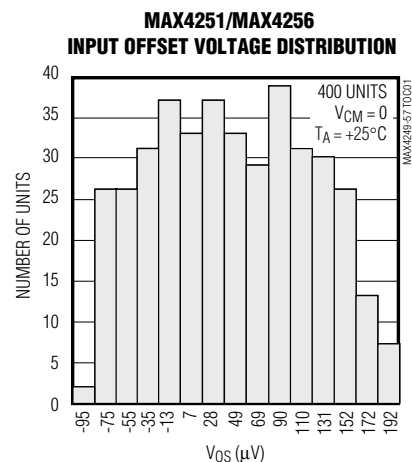
**Note 6:** Guaranteed by design.

**Note 7:** Lowpass-filter bandwidth is 22kHz for  $f = 1kHz$  and 80kHz for  $f = 20kHz$ . Noise floor of test equipment =  $10nV/\sqrt{Hz}$ .

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Typical Operating Characteristics

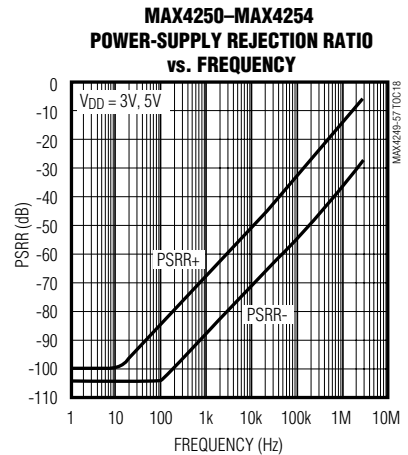
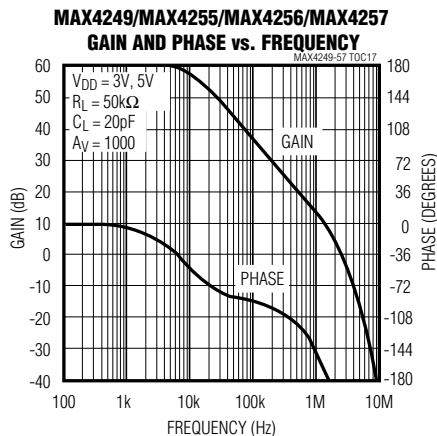
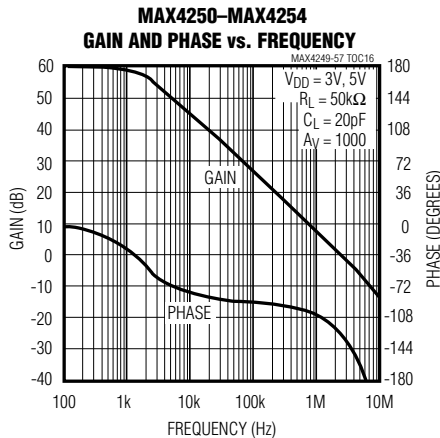
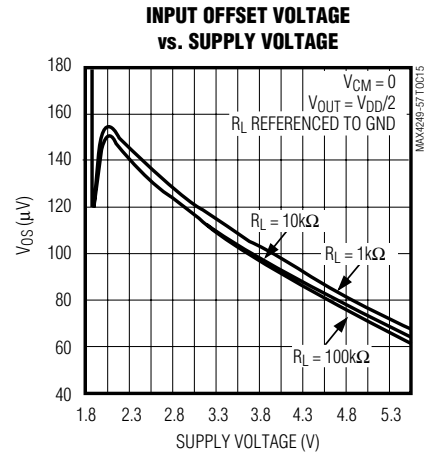
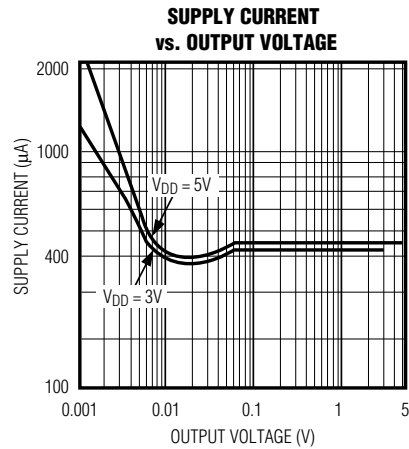
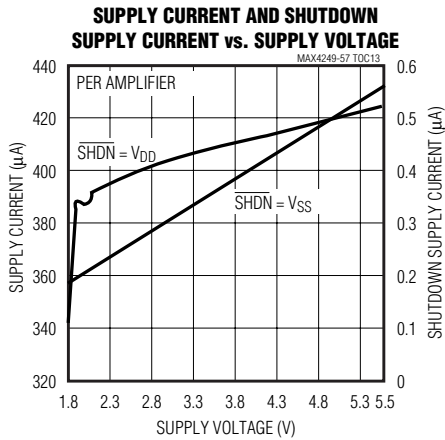
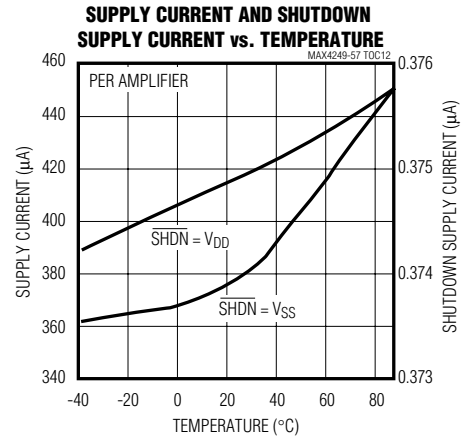
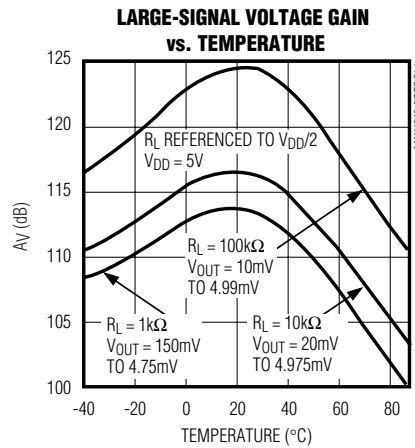
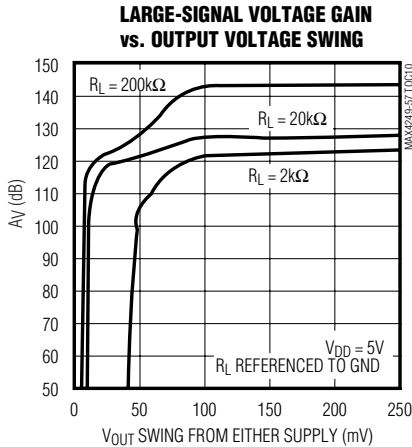
( $V_{DD} = 5V$ ,  $V_{SS} = 0$ ,  $V_{CM} = V_{OUT} = V_{DD}/2$ , input noise floor of test equipment =  $10nV/\sqrt{Hz}$  for all distortion measurements,  $T_A = +25^\circ C$ , unless otherwise noted.)



# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Typical Operating Characteristics (continued)

( $V_{DD} = 5V$ ,  $V_{SS} = 0$ ,  $V_{CM} = V_{OUT} = V_{DD}/2$ , input noise floor of test equipment =  $10nV/\sqrt{Hz}$  for all distortion measurements,  $T_A = +25^\circ C$ , unless otherwise noted.)

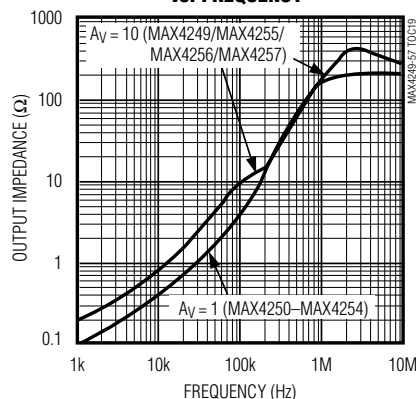


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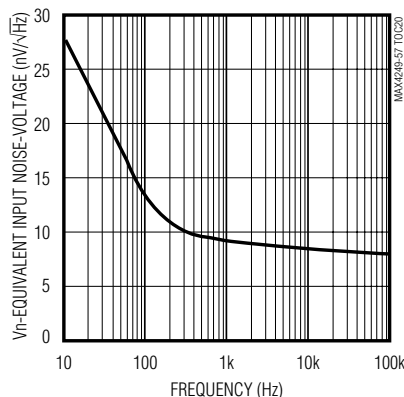
## Typical Operating Characteristics (continued)

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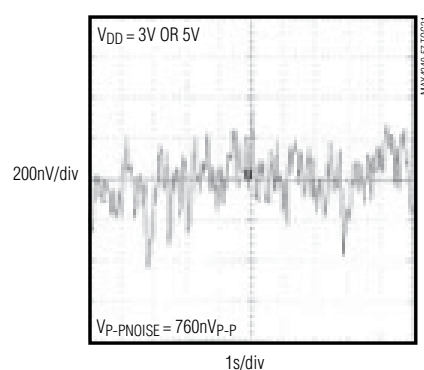
**OUTPUT IMPEDANCE vs. FREQUENCY**



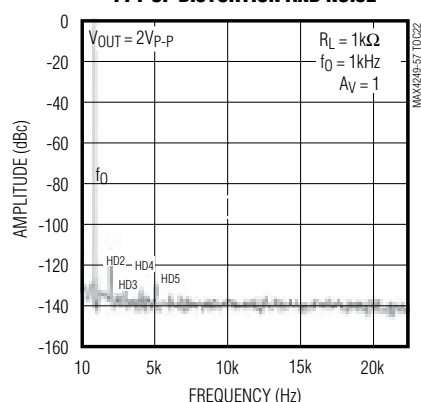
**INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY**



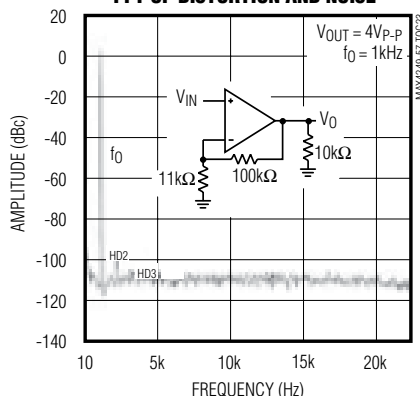
**0.1Hz TO 10Hzp-p NOISE**



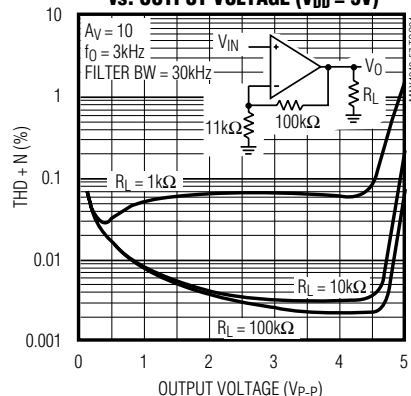
**MAX4250-MAX4254  
FFT OF DISTORTION AND NOISE**



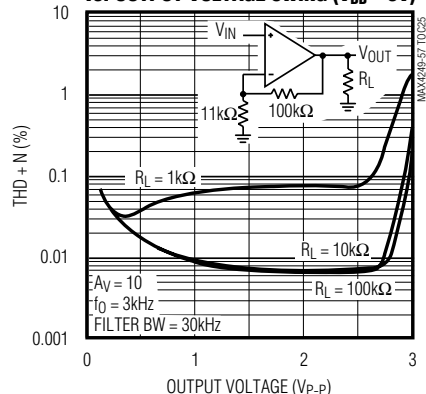
**MAX4249/MAX4255/MAX4256/MAX4257  
FFT OF DISTORTION AND NOISE**



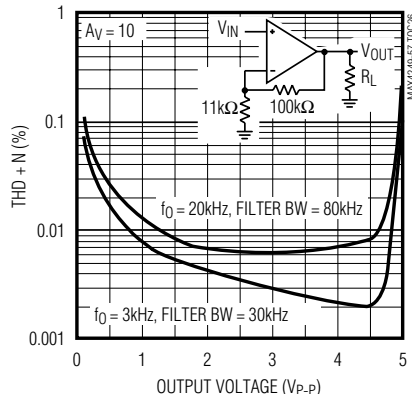
**MAX4250-MAX4254  
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE ( $V_{DD} = 5V$ )**



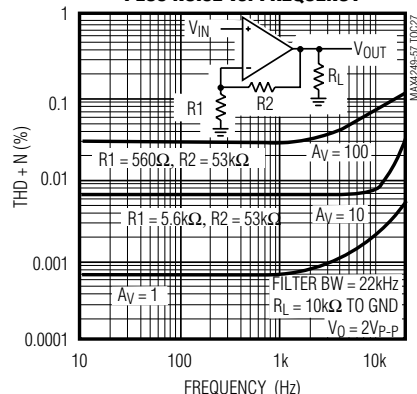
**MAX4250-MAX4254  
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING ( $V_{DD} = 3V$ )**



**MAX4249/MAX4255/MAX4256/MAX4257  
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING**



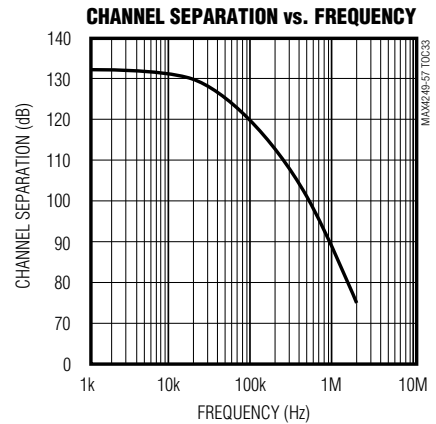
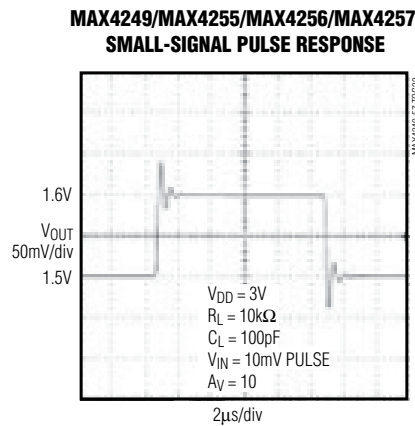
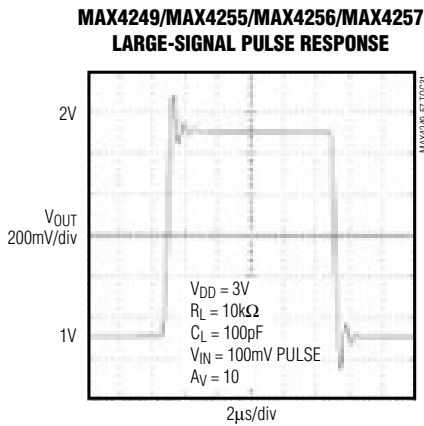
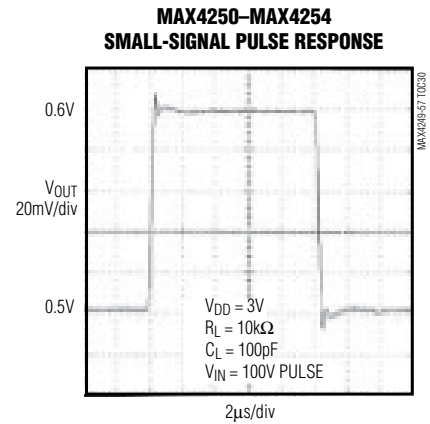
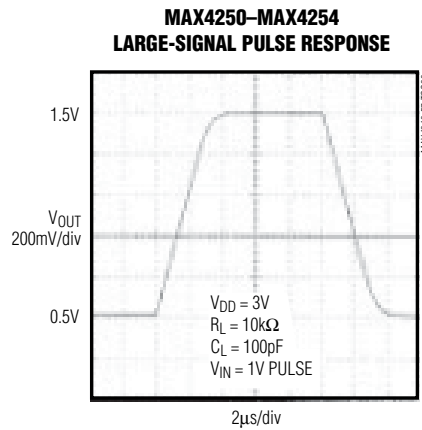
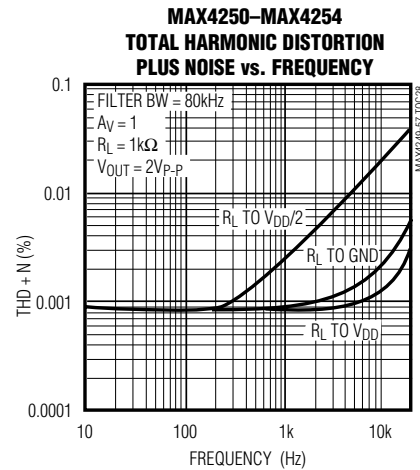
**MAX4250-MAX4254  
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Typical Operating Characteristics (continued)

( $V_{DD} = 5V$ ,  $V_{SS} = 0$ ,  $V_{CM} = V_{OUT} = V_{DD}/2$ , input noise floor of test equipment =  $10nV/\sqrt{Hz}$  for all distortion measurements,  $T_A = +25^\circ C$ , unless otherwise noted.)





# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Pin Description

MAX4249-MAX4257

PIN/BUMP								NAME	FUNCTION
MAX4250/ MAX4255	MAX4251/ MAX4256	MAX4252/ MAX4257	MAX4252	MAX4249/ MAX4253			MAX4254		
5-Pin SOT23	8-Pin SO/μMAX	8-Pin SO/μMAX	8-Pin UCSP	10-Pin UCSP	10-Pin μMAX	14-Pin SO	14-Pin SO		
1	6	1, 7	A1, A3	A1, C1	1, 9	1, 13	1, 7, 8, 14	OUT, OUTA, OUTB, OUTC, OUTD	Amplifier Output
2	4	4	C2	B4	4	4	11	Vss	Negative Supply. Connect to ground for single-supply operation
3	3	3, 5	C1, C3	A3, C3	3, 5	3, 11	3, 5, 10, 12	IN+, INA+, INB+, INC+, IND+	Noninverting Amplifier Input
4	2	2, 6	B1, B3	A2, C2	2, 6	2, 12	2, 6, 9, 13	IN-, INA-, INB-, INC-, IND-	Inverting Amplifier Input
5	7	8	A2	B1	8	14	4	VDD	Positive Supply
—	8	—	—	A4, C4	—	5, 9	—	$\overline{\text{SHDN}}$ , $\overline{\text{SHDNA}}$ , $\overline{\text{SHDNB}}$	Shutdown Input, Connect to VDD or leave unconnected for normal operation (amplifier(s) enabled).
—	1, 5	—	—	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	—	—	B2	B2, B3	—	—	—	—	Not populated with solder sphere

## Detailed Description

The MAX4249–MAX4257 single-supply operational amplifiers feature ultra-low noise and distortion while consuming very little power. Their low distortion and low noise make them ideal for use as preamplifiers in wide dynamic-range applications, such as 16-bit analog-to-digital converters (see *Typical Operating Circuit*). Their high-input impedance and low noise are also useful for signal conditioning of high-impedance sources, such as piezoelectric transducers.

These devices have true rail-to-rail output operation, drive loads as low as 1kΩ while maintaining DC accuracy,

and can drive capacitive loads up to 400pF without oscillation. The input common-mode voltage range extends from V<sub>DD</sub> - 1.1V to 200mV beyond the negative rail. The push-pull output stage maintains excellent DC characteristics, while delivering up to ±5mA of current.

The MAX4250–4254 are unity-gain stable, whereas, the MAX4249/MAX4255/MAX4256/MAX4257 have a higher slew rate and are stable for gains ≥ 10V/V. The MAX4249/MAX4251/MAX4253/MAX4256 feature a low-power shutdown mode, which reduces the supply current to 0.5μA and disables the outputs.

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Low Distortion

Many factors can affect the noise and distortion that the device contributes to the input signal. The following guidelines offer valuable information on the impact of design choices on Total Harmonic Distortion (THD).

Choosing proper feedback and gain resistor values for a particular application can be a very important factor in reducing THD. In general, the smaller the closed-loop gain, the smaller the THD generated, especially when driving heavy resistive loads. Large-value feedback resistors can significantly improve distortion. The THD of the part normally increases at approximately 20dB per decade, as a function of frequency. Operating the device near or above the full-power bandwidth significantly degrades distortion.

Referencing the load to either supply also improves the part's distortion performance, because only one of the MOSFETs of the push-pull output stage drives the output. Referencing the load to midsupply increases the part's distortion for a given load and feedback setting. (See the Total Harmonic Distortion vs. Frequency graph in the *Typical Operating Characteristics*.)

For gains  $\geq 10\text{V/V}$ , the decompensated devices MAX4249/MAX4255/MAX4256/MAX4257 deliver the best distortion performance, since they have a higher slew rate and provide a higher amount of loop gain for a given closed-loop gain setting. Capacitive loads below 400pF, do not significantly affect distortion results. Distortion performance remains relatively constant over supply voltages.

## Low Noise

The amplifier's input-referred, noise-voltage density is dominated by flicker noise at lower frequencies, and by thermal noise at higher frequencies. Because the thermal noise contribution is affected by the parallel combination of the feedback resistive network ( $R_F \parallel R_G$ , Figure 1), these resistors should be reduced in cases where the system bandwidth is large and thermal noise is dominant. This noise contribution factor decreases, however, with increasing gain settings.

For example, the input noise-voltage density of the circuit with  $R_F = 100\text{k}\Omega$ ,  $R_G = 11\text{k}\Omega$  ( $A_V = 10\text{V/V}$ ) is  $e_n = 15\text{nV}/\sqrt{\text{Hz}}$ ,  $e_n$  can be reduced to  $9\text{nV}/\sqrt{\text{Hz}}$  by choosing  $R_F = 10\text{k}\Omega$ ,  $R_G = 1.1\text{k}\Omega$  ( $A_V = 10\text{V/V}$ ), at the expense of greater current consumption and potentially higher distortion. For a gain of  $100\text{V/V}$  with  $R_F = 100\text{k}\Omega$ ,  $R_G = 1.1\text{k}\Omega$ , the  $e_n$  is low ( $9\text{nV}/\sqrt{\text{Hz}}$ ).

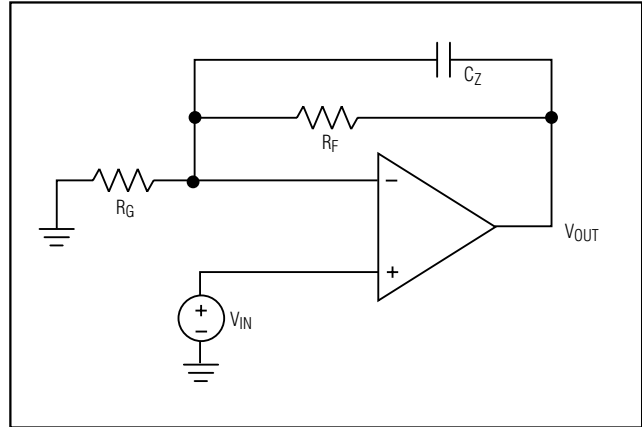


Figure 1. Adding Feed-Forward Compensation

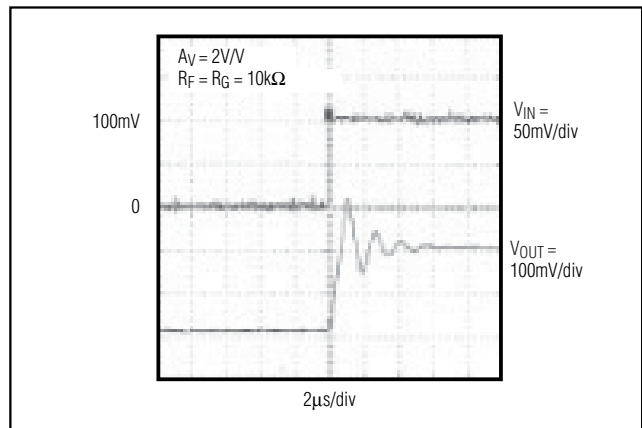


Figure 2a. Pulse Response with No Feed-Forward Compensation

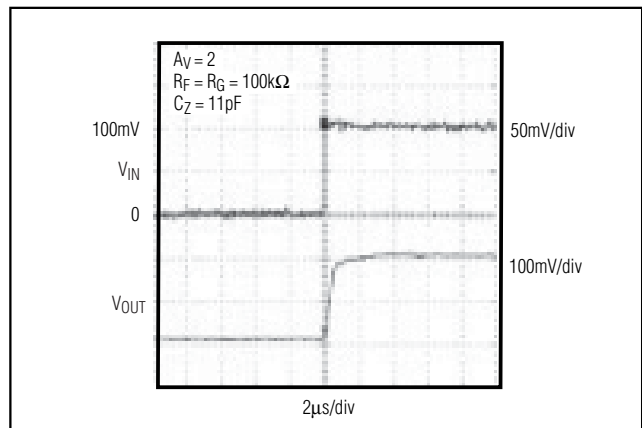


Figure 2b. Pulse Response with 10pF Feed-Forward Compensation

## UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

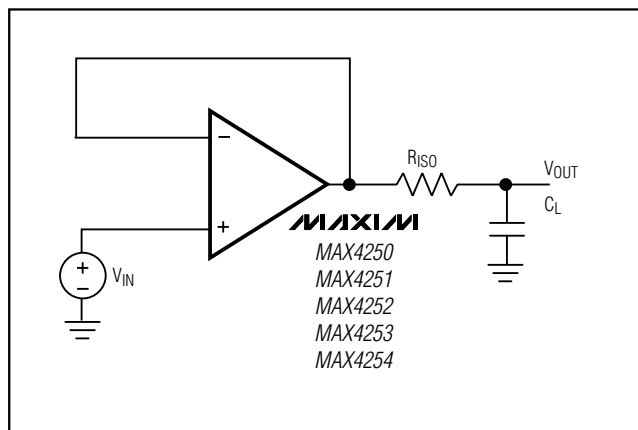


Figure 3. Overdriven Input Showing No Phase Reversal

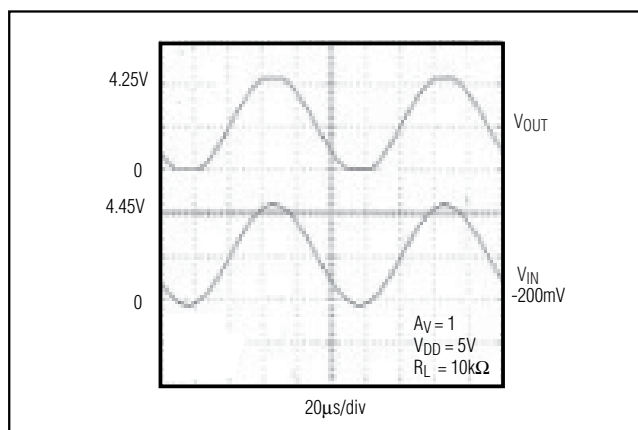


Figure 4. Rail-to-Rail Output Operation

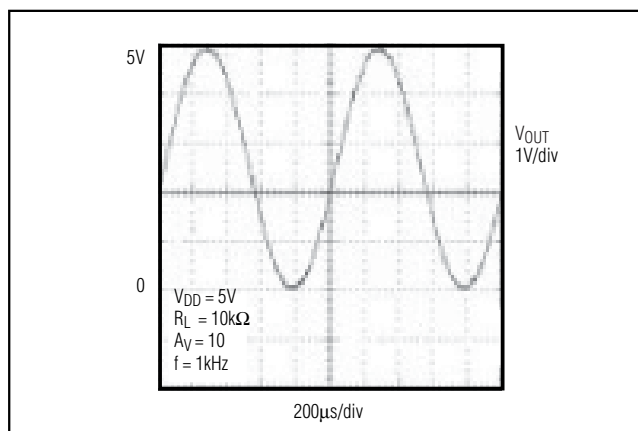


Figure 5. Capacitive-Load Driving Circuit

### Using a Feed-Forward Compensation Capacitor, $C_z$

The amplifier's input capacitance is 11pF. If the resistance seen by the inverting input is large (feedback network), this can introduce a pole within the amplifier's bandwidth, resulting in reduced phase margin. Compensate the reduced phase margin by introducing a feed-forward capacitor ( $C_z$ ) between the inverting input and the output (Figure 1). This effectively cancels the pole from the inverting input of the amplifier. Choose the value of  $C_z$  as follows:

$$C_z = 11 \times (R_F / R_G) \text{ [pF]}$$

In the unity-gain stable MAX4250–MAX4254, the use of a proper  $C_z$  is most important for  $A_V = 2V/V$ , and  $A_V = -1V/V$ . In the decompensated MAX4249/MAX4255 /MAX4256/MAX4257,  $C_z$  is most important for  $A_V = 10V/V$ . Figures 2a and 2b show transient response both with and without  $C_z$ .

Using a slightly smaller  $C_z$  than suggested by the formula above achieves a higher bandwidth at the expense of reduced phase and gain margin. As a general guideline, consider using  $C_z$  for cases where  $R_G || R_F$  is greater than 20k $\Omega$  (MAX4250–MAX4254) or greater than 5k $\Omega$  (MAX4249/MAX4255/MAX4256/MAX4257).

### Applications Information

The MAX4249–MAX4257 combine good driving capability with ground-sensing input and rail-to-rail output operation. With their low distortion, low noise and low-power consumption, these devices are ideal for use in portable instrumentation systems and other low-power, noise-sensitive applications.

#### Ground-Sensing and Rail-to-Rail Outputs

The common-mode input range of these devices extends below ground, and offers excellent common-mode rejection. These devices are guaranteed not to undergo phase reversal when the input is overdriven (Figure 3).

Figure 4 showcases the true rail-to-rail output operation of the amplifier, configured with  $A_V = 10V/V$ . The output swings to within 8mV of the supplies with a 10k $\Omega$  load, making the devices ideal in low-supply-voltage applications.

#### Output Loading and Stability

Even with their low quiescent current of 400 $\mu$ A, these amplifiers can drive 1k $\Omega$  loads while maintaining excellent DC accuracy. Stability while driving heavy capacitive loads is another key feature.

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

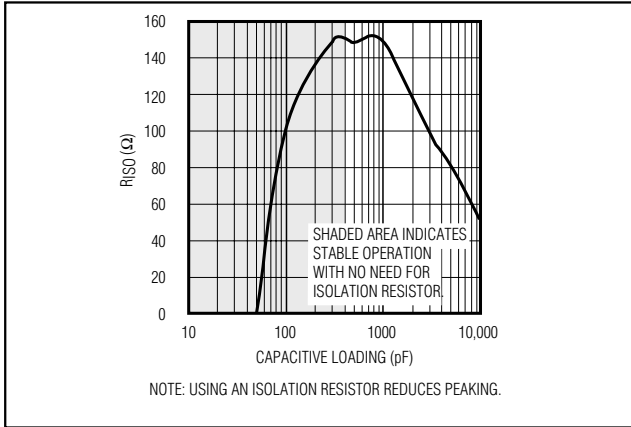


Figure 6. Isolation Resistance vs. Capacitive Loading to Minimize Peaking (<2dB)

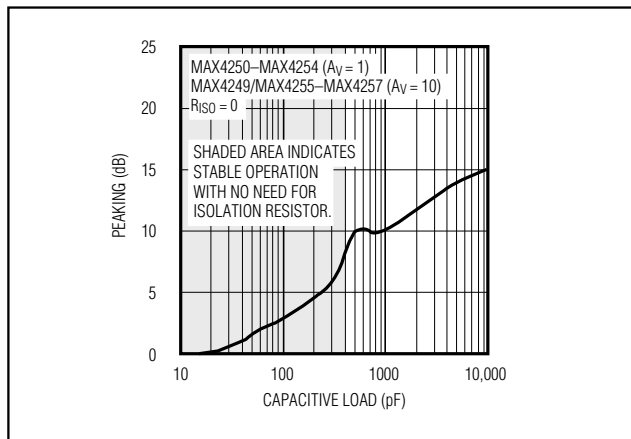


Figure 7. Peaking vs. Capacitive Load

These devices maintain stability while driving loads up to 400pF. To drive higher capacitive loads, place a small isolation resistor in series between the output of the amplifier and the capacitive load (Figure 5). This resistor improves the amplifier's phase margin by isolating the capacitor from the op amp's output. Reference Figure 6 to select a resistance value that will ensure a load capacitance that limits peaking to <2dB (25%). For example, if the capacitive load is 1000pF, the corresponding isolation resistor is 150Ω. Figure 7 shows that peaking occurs without the isolation resistor. Figure 8 shows the unity-gain bandwidth vs. capacitive load for the MAX4250-MAX4254.

## Power Supplies and Layout

The MAX4249-MAX4257 operate from a single 2.4V to 5.5V power supply or from dual supplies of ±1.20V to ±2.75V. For single-supply operation, bypass the power

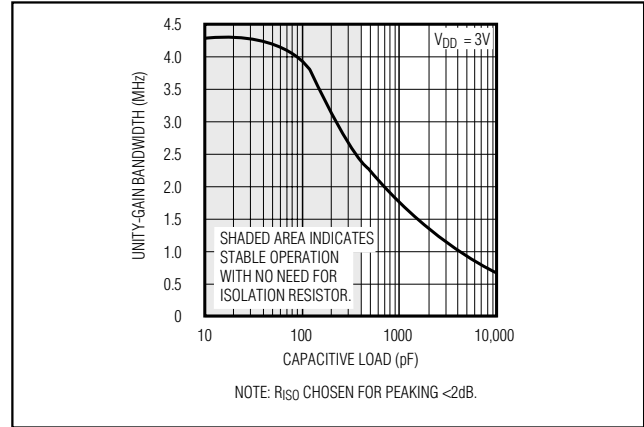


Figure 8. MAX4250-4254 Unity-Gain Bandwidth vs. Capacitive Load

supply with a 0.1μF ceramic capacitor placed close to the VDD pin. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and output. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amp's pins.

## UCSP Package Consideration

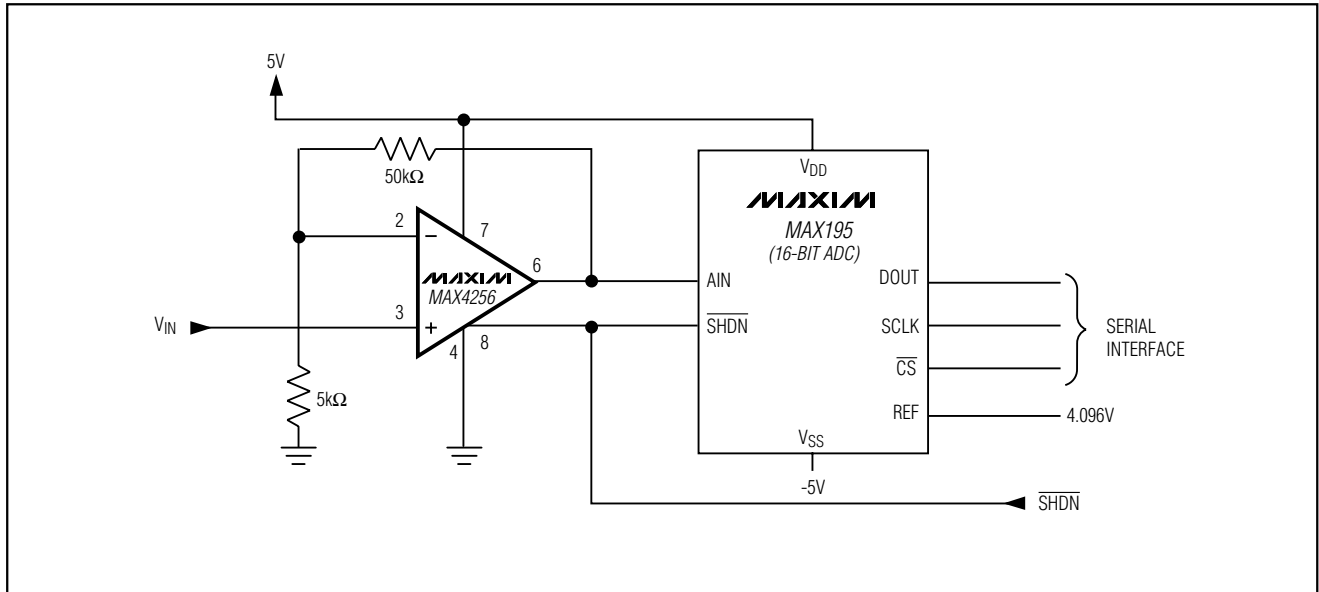
For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Ultra-Chip-Board-Scale-Package).

## UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP. Performance through operating life test and moisture resistance remains uncompromised as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder-joint contact integrity must be considered. Table 1 shows the testing done to characterize the UCSP reliability performance. In conclusion, the UCSP is capable of performing reliably through environmental stresses as indicated by the results in the table. Additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Typical Operating Circuit



MAX4249-MAX4257

Table 1. Reliability Test Data

TEST	CONDITIONS	DURATION	NO. OF FAILURES PER SAMPLE SIZE
Temperature Cycle	-35°C to +85°C, -40°C to +100°C	150 cycles, 900 cycles	0/10, 0/200
Operating Life	$T_A = +70^\circ\text{C}$	240h	0/10
Moisture Resistance	-20°C to +60°C, 90% RH	240h	0/10
Low-Temperature Storage	-20°C	240h	0/10
Low-Temperature Operational	-10°C	24h	0/10
Solderability	8h steam age	—	0/15
ESD	$\pm 2000V$ , Human Body Model	—	0/5
High-Temperature Operating Life	$T_J = +150^\circ\text{C}$	168h	0/45

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Selector Guide

PART	GAIN BANDWIDTH (MHz)	MINIMUM STABLE GAIN (V/V)	NO. OF AMPLIFIERS PER PACKAGE	SHUTDOWN MODE	PIN-PACKAGE
MAX4249	22	10	2	Yes	10-pin $\mu$ MAX, 14-pin SO
MAX4250	3	1	1	—	5-pin SOT23
MAX4251	3	1	1	Yes	8-pin $\mu$ MAX/SO
MAX4252	3	1	2	—	8-pin $\mu$ MAX/SO, 8-pin UCSP
MAX4253	3	1	2	Yes	10-pin $\mu$ MAX, 14-pin SO, 10-pin UCSP
MAX4254	3	1	4	—	14-pin SO
MAX4255	22	10	1	—	5-pin SOT23
MAX4256	22	10	1	Yes	8-pin $\mu$ MAX/SO
MAX4257	22	10	2	—	8-pin $\mu$ MAX/SO

## Ordering Information (continued)

PART	TEMP RANGE	PIN- PACKAGE	TOP MARK
<b>MAX4251</b> ESA	-40°C to +85°C	8 SO	—
MAX4251EUA	-40°C to +85°C	8 $\mu$ MAX	—
<b>MAX4252</b> EBL-T*	-40°C to +85°C	8 UCSP-8	AAO
MAX4252ESA	-40°C to +85°C	8 SO	—
MAX4252EUA	-40°C to +85°C	8 $\mu$ MAX	—
<b>MAX4253</b> EBC-T*	-40°C to +85°C	10 UCSP-10	AAK
MAX4253EUB	-40°C to +85°C	10 $\mu$ MAX	—
MAX4253ESD	-40°C to +85°C	14 SO	—
<b>MAX4254</b> ESD	-40°C to +85°C	14 SO	—
<b>MAX4255</b> EUK-T	-40°C to +85°C	5 SOT23-5	ACCJ
<b>MAX4256</b> ESA	-40°C to +85°C	8 SO	—
MAX4256EUA	-40°C to +85°C	8 $\mu$ MAX	—
<b>MAX4257</b> ESA	-40°C to +85°C	8 SO	—
MAX4257EUA	-40°C to +85°C	8 $\mu$ MAX	—

\*UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.

## Chip Information

MAX4250/MAX4251/MAX4255/MAX4256 TRANSISTOR COUNT: 170

MAX4249/MAX4252/MAX4253/MAX4257 TRANSISTOR COUNT: 340

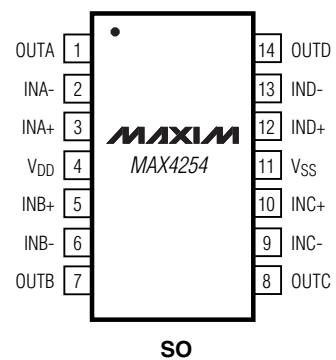
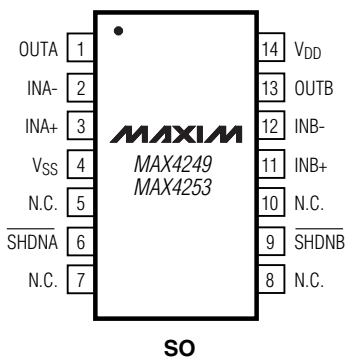
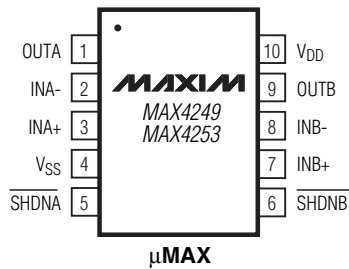
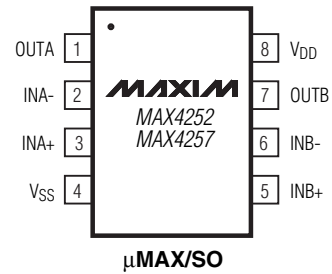
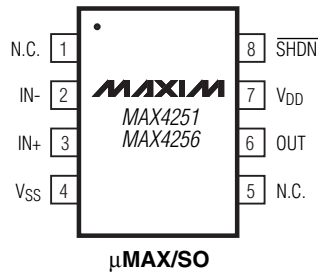
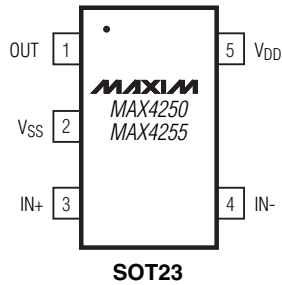
MAX4254 TRANSISTOR COUNT: 680

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Pin Configurations (continued)

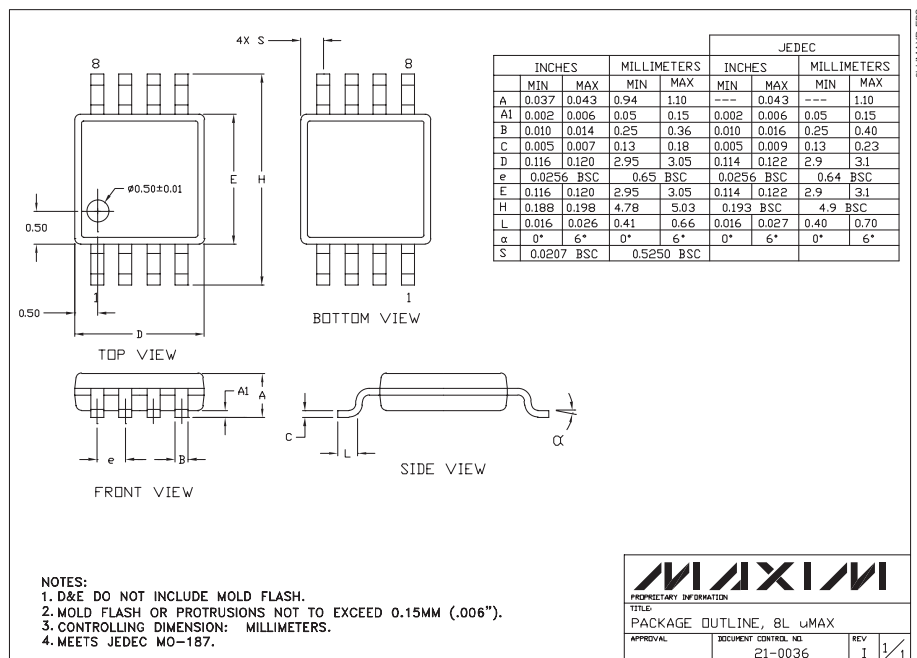
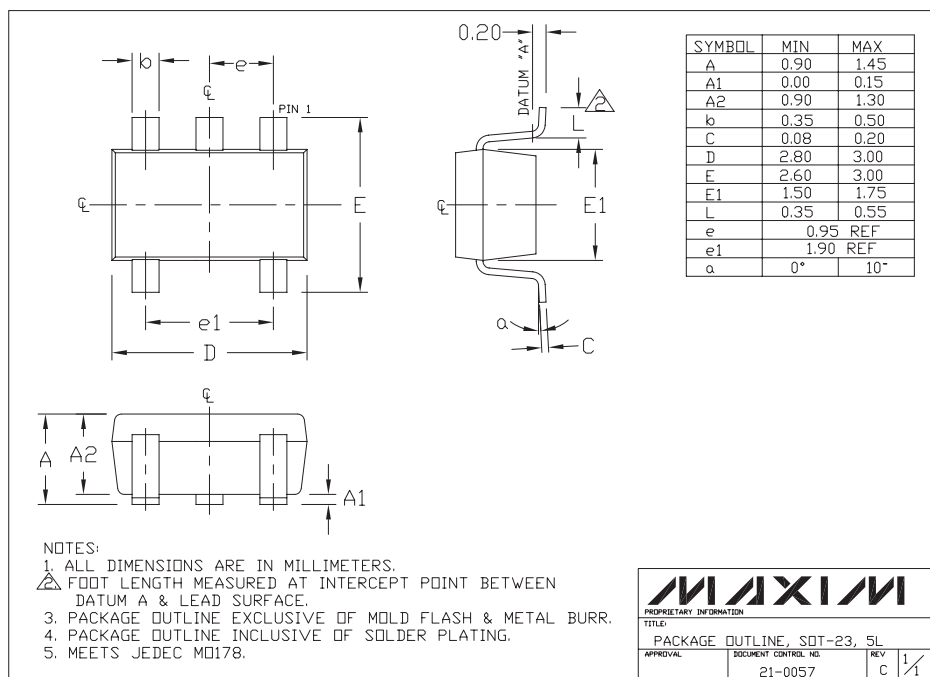
**MAX4249-MAX4257**

TOP VIEW



# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Package Information

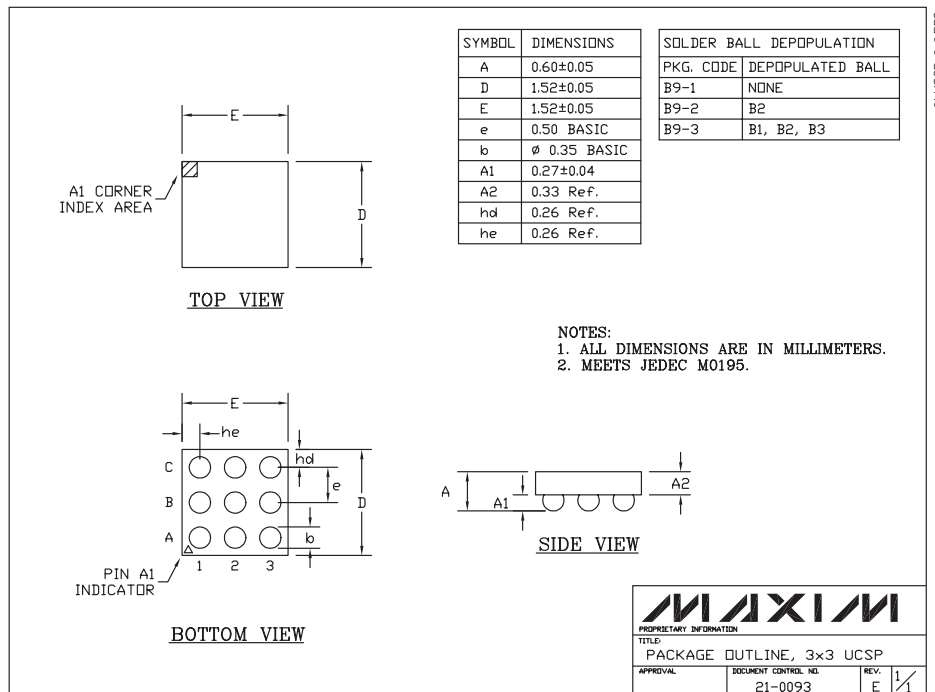
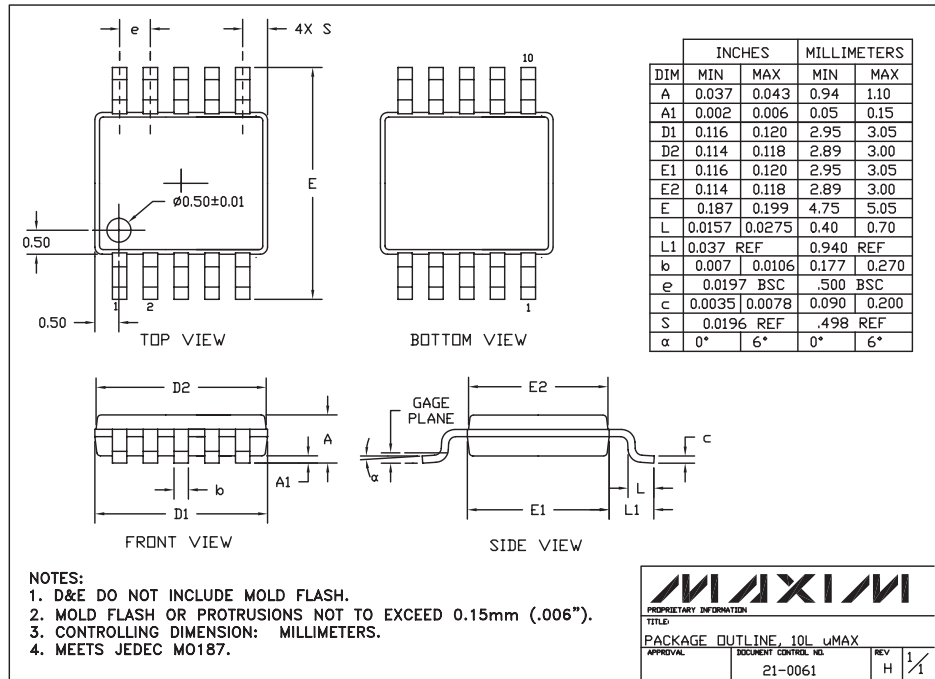




# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

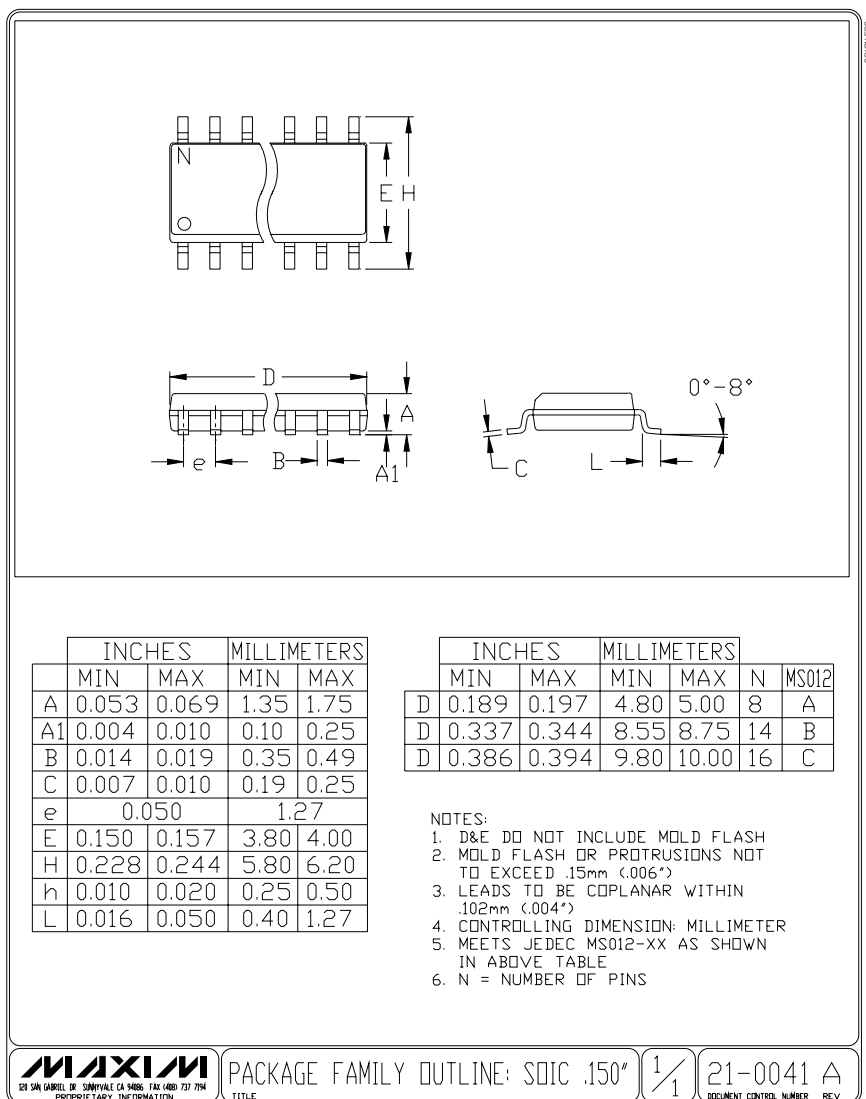
## Package Information (continued)

MAX4249-MAX4257



# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

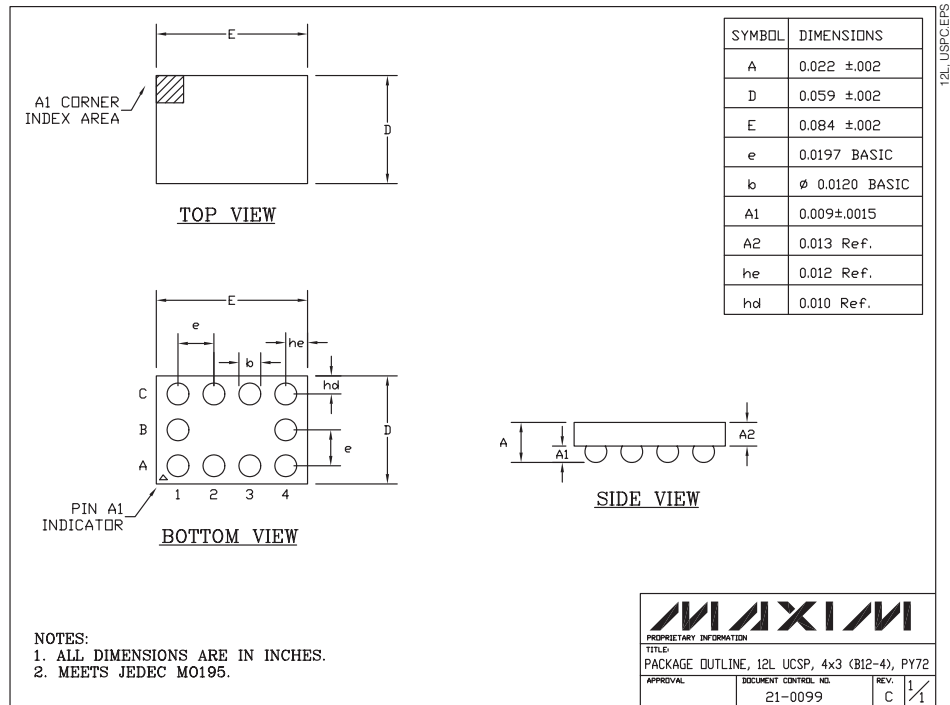
## Package Information (continued)



# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Package Information (continued)

MAX4249-MAX4257



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