

**MICROCHIP****24AA512/24LC512/24FC512****512K I²C™ CMOS Serial EEPROM****Device Selection Table**

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
24AA512	1.8-5.5V	400 kHz ⁽¹⁾	I
24LC512	2.5-5.5V	400 kHz	I, E
24FC512	2.5-5.5V	1 MHz	I

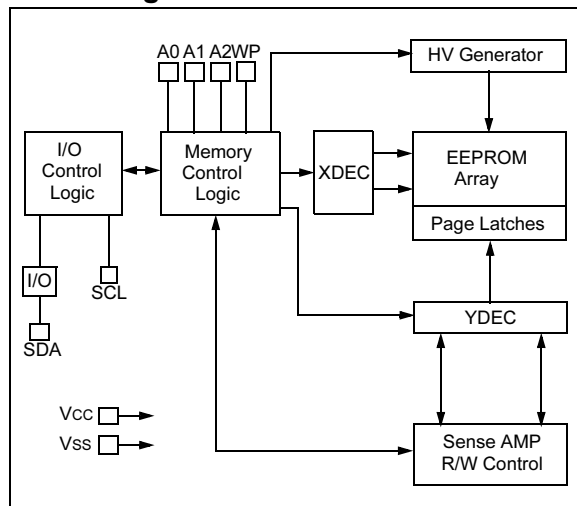
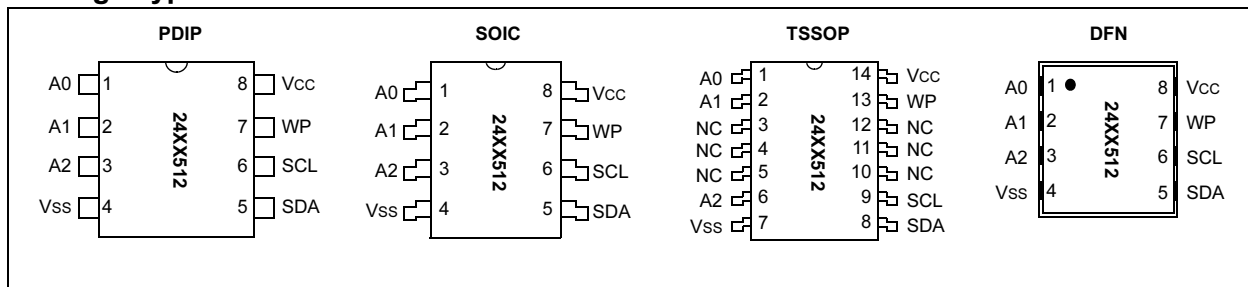
Note 1: 100 kHz for Vcc < 2.5V

Features

- Low-power CMOS technology
 - Maximum write current 5 mA at 5.5V
 - Maximum read current 400 µA at 5.5V
 - Standby current 100 nA typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- Cascadable for up to eight devices
- Self-timed ERASE/WRITE cycle
- 128-byte Page Write mode available
- 5 ms max. write cycle time
- Hardware write-protect for entire array
- Schmitt Trigger inputs for noise suppression
- 1,000,000 erase/write cycles
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP, SOIC (208 mil), and DFN packages
- 14-lead TSSOP package
- Standard and Pb-free finishes available
- Temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

Description

The Microchip Technology Inc. 24AA512/24LC512/24FC512 (24XX512*) is a 64K x 8 (512 Kbit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low-power applications such as personal communications and data acquisition. This device also has a page write capability of up to 128 bytes of data. This device is capable of both random and sequential reads up to the 512K boundary. Functional address lines allow up to eight devices on the same bus, for up to 4 Mbit address space. This device is available in the standard 8-pin plastic DIP, SOIC, DFN and 14-lead TSSOP packages.

Block Diagram**Package Type**

* 24XX512 is used in this document as a generic part number for the 24AA512/24LC512/24FC512 devices.

24AA512/24LC512/24FC512

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ^(†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature	-65°C to +150°C
Ambient temperature with power applied	-65°C to +125°C
ESD protection on all pins	≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics:			
			Industrial (I): V _{CC} = +1.8V to 5.5V		T _{AMB} = -40°C to +85°C	
			Automotive (E): V _{CC} = +2.5V to 5.5V		T _{AMB} = -40°C to +125°C	
Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
D1	—	A0, A1, A2, SCL, SDA and WP pins:	—	—	—	—
D2	V _{IH}	High-level input voltage	0.7 V _{CC}	—	V	—
D3	V _{IL}	Low-level input voltage	—	0.3 V _{CC} 0.2 V _{CC}	V V	V _{CC} ≥ 2.5V V _{CC} < 2.5V
D4	V _{HYS}	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 V _{CC}	—	V	V _{CC} ≥ 2.5V (Note)
D5	V _{OL}	Low-level output voltage	—	0.40	V	I _{OL} = 3.0 ma @ V _{CC} = 4.5V I _{OL} = 2.1 ma @ V _{CC} = 2.5V
D6	I _{LI}	Input leakage current	—	±10	μA	V _{IN} = V _{SS} or V _{CC} , WP = V _{SS} V _{IN} = V _{SS} or V _{CC} , WP = V _{CC}
D7	I _{LO}	Output leakage current	—	±10	μA	V _{OUT} = V _{SS} or V _{CC}
D8	C _{IN} , C _{OUT}	Pin capacitance (all inputs/outputs)	—	10	pF	V _{CC} = 5.0V (Note) T _{AMB} = 25°C, f _c = 1 MHz
D9	I _{CC} Read	Operating current	—	400	μA	V _{CC} = 5.5V, SCL = 400 kHz
	I _{CC} Write		—	5	mA	V _{CC} = 5.5V
D10	I _{CCS}	Standby current	—	1	μA	T _{AMB} = -40°C to +85°C SCL = SDA = V _{CC} = 5.5V A0, A1, A2, WP = V _{SS}
			—	5	μA	T _{AMB} = -40°C to +125°C SCL = SDA = V _{CC} = 5.5V A0, A1, A2, WP = V _{SS}

Note: This parameter is periodically sampled and not 100% tested.

24AA512/24LC512/24FC512

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics:			
			Industrial (I):	VCC = +1.8V to 5.5V	TAMB = -40°C to +85°C	
			Automotive (E):	VCC = +2.5V to 5.5V	TAMB = -40°C to +125°C	
Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
1	FCLK	Clock frequency	— — —	100 400 1000	kHz	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
2	THIGH	Clock high time	4000 600 500	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
3	TLOW	Clock low time	4700 1300 500	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
4	TR	SDA and SCL rise time (Note 1)	— — —	1000 300 300	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
5	TF	SDA and SCL fall time (Note 1)	— —	300 100	ns	All except, 24FC512 2.5V ≤ VCC ≤ 5.5V 24FC512
6	THD:STA	Start condition hold time	4000 600 250	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
7	TSU:STA	Start condition setup time	4700 600 250	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
8	THD:DAT	Data input hold time	0	—	ns	(Note 2)
9	TSU:DAT	Data input setup time	250 100 100	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
10	TSU:STO	Stop condition setup time	4000 600 250	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
11	TSU:WP	WP setup time	4000 600 600	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
12	THD:WP	WP hold time	4700 1300 1300	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
13	TAA	Output valid from clock (Note 2)	— — —	3500 900 400	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
14	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700 1300 500	— — —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 2.5V ≤ VCC ≤ 5.5V 24FC512
16	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except, 24FC512 (Notes 1 and 3)
17	TWC	Write cycle time (byte or page)	—	5	ms	—
18	—	Endurance	1,000,000	—	cycles	25°C (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

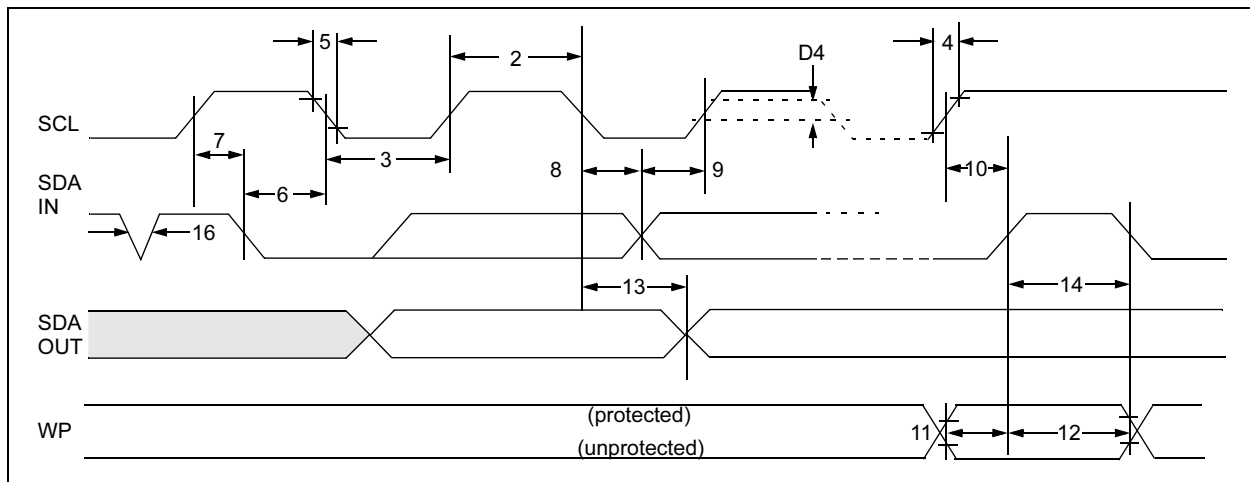
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

24AA512/24LC512/24FC512

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	14-lead TSSOP	DFN	Function
A0	1	1	1	1	User Configured Chip Select
A1	2	2	2	2	User Configured Chip Select
(NC)	—	—	3, 4, 5	—	Not Connected
A2	3	3	6	3	User Configured Chip Select
Vss	4	4	7	4	Ground
SDA	5	5	8	5	Serial Data
SCL	6	6	9	6	Serial Clock
(NC)	—	—	10, 11, 12	—	Not Connected
WP	7	7	13	7	Write-Protect Input
Vcc	8	8	14	8	+1.8V to 5.5V (24AA512) +2.5V to 5.5V (24LC512) +2.5V to 5.5V (24FC512)

2.1 A0, A1, A2 Chip Address Inputs

The A0, A1, A2 inputs are used by the 24XX512 for multiple device operations. The logic levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. If these pins are left unconnected, the inputs will be pulled down internally to Vss. If they are tied to Vcc or driven high, the internal pull-down circuitry is disabled.

In most applications, the chip address inputs A0, A1, and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable logic device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 k Ω for 100 kHz, 2 k Ω for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.4 Write-Protect (WP)

This pin can be connected to either Vss or Vcc. Internal pull-down circuitry on this pin will keep the device in the unprotected state if left floating, however, floating this pin is not recommended for most applications. If tied to Vss, normal memory operation is enabled (read/write the entire memory 0000-FFFF).

If tied to Vcc, write operations are inhibited. Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX512 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the Start and Stop conditions, while the 24XX512 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line, while the clock line is high, will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit. See Figure 4-2 for acknowledge timing.

Note: The 24XX512 does not generate any Acknowledge bits if an internal programming cycle is in progress.
--

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX512) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

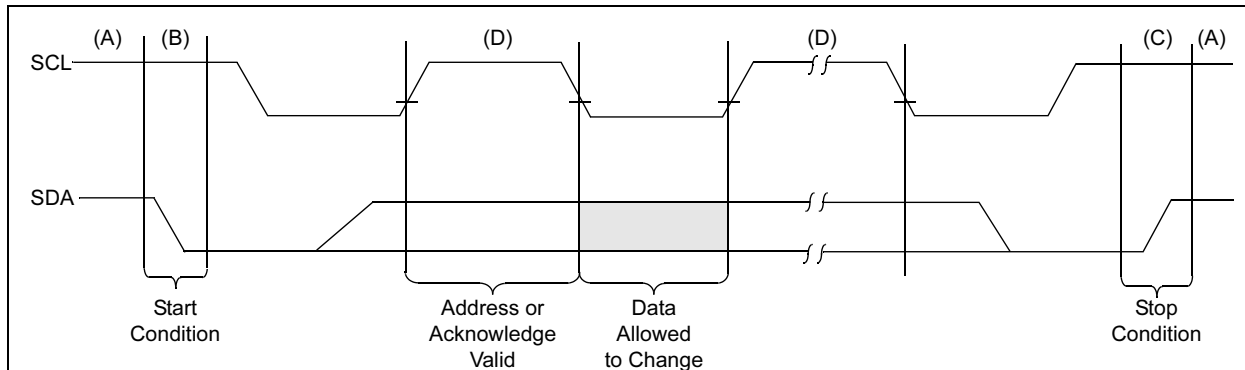
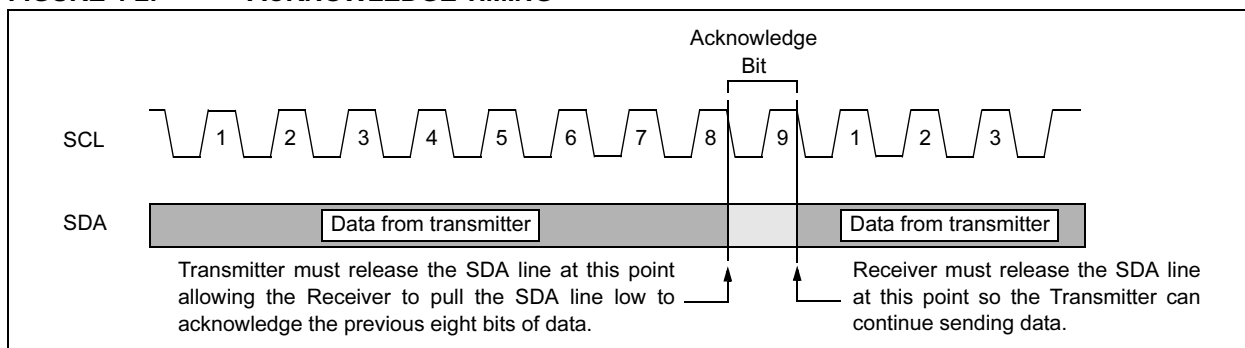


FIGURE 4-2: ACKNOWLEDGE TIMING



24AA512/24LC512/24FC512

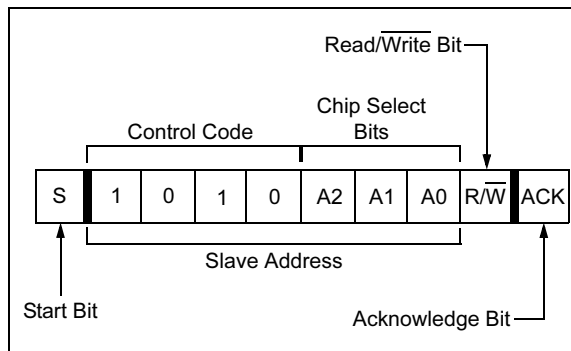
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a 4-bit control code; for the 24XX512 this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX512 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because all A15...A0 are used, there are no upper address bits that are don't care. The upper address bits are transferred first, followed by the less significant bits.

Following the Start condition, the 24XX512 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24XX512 will select a read or write operation.

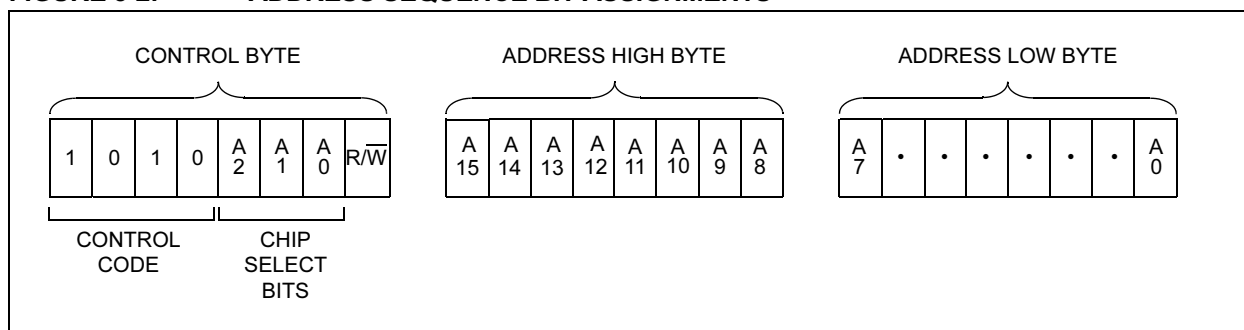
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1, A0 can be used to expand the contiguous address space for up to 4 Mbit by adding up to eight 24XX512s on the same bus. In this case, software can use A0 of the **control byte** as address bit A16; A1, as address bit A17; and A2, as address bit A18. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the master, the control code (four bits), the Chip Select (three bits), and the R/W bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24XX512. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX512, the master device will transmit the data word to be written into the addressed memory location. The 24XX512 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and, during this time, the 24XX512 will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24XX512 in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 127 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a Stop condition. After receipt of each word, the six lower address pointer bits are internally incremented by one. If the master should transmit more than 128 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-FFFF) when the pin is tied to Vcc. If tied to Vss or left floating, the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 1-1) Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

24AA512/24LC512/24FC512

FIGURE 6-1: BYTE WRITE

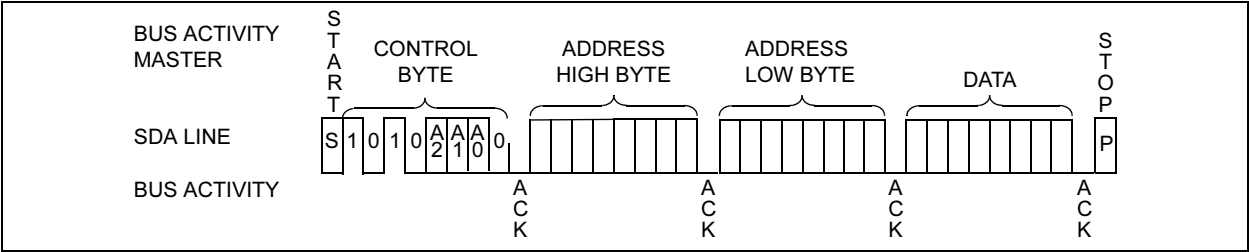
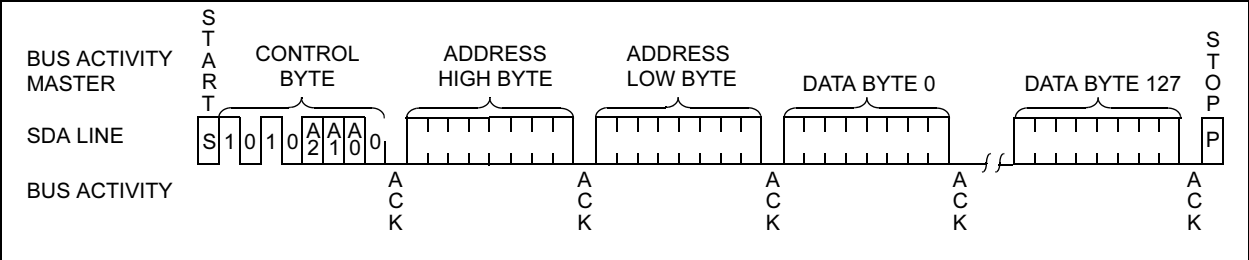


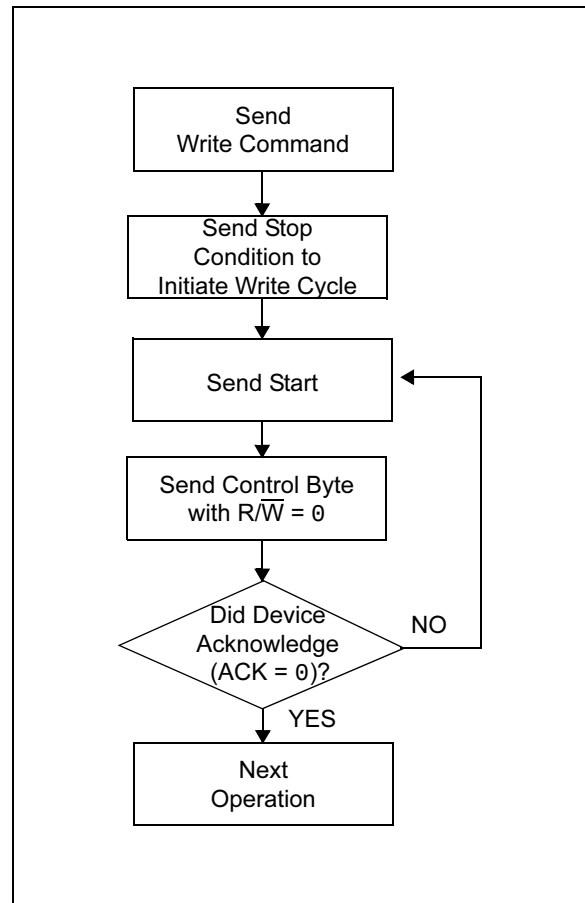
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



24AA512/24LC512/24FC512

8.0 READ OPERATION

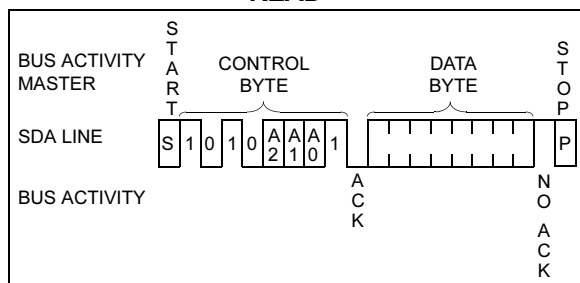
Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX512 contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with $R/\overline{W}$ bit set to '1', the 24XX512 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24XX512 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX512 as part of a write operation ($R/\overline{W}$ bit set to '0'). After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then, the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24XX512 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition which causes the 24XX512 to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX512 transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX512 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a Stop condition. To provide sequential reads, the 24XX512 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address FFFF to address 0000 if the master acknowledges the byte received from the array address FFFF.

FIGURE 8-2: RANDOM READ

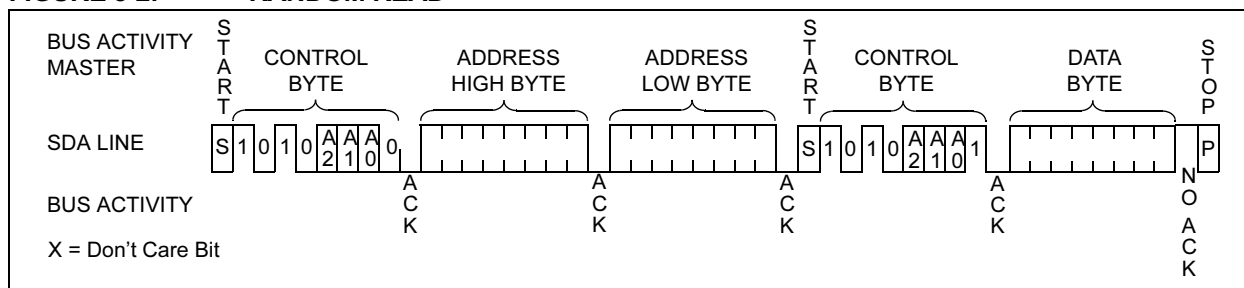
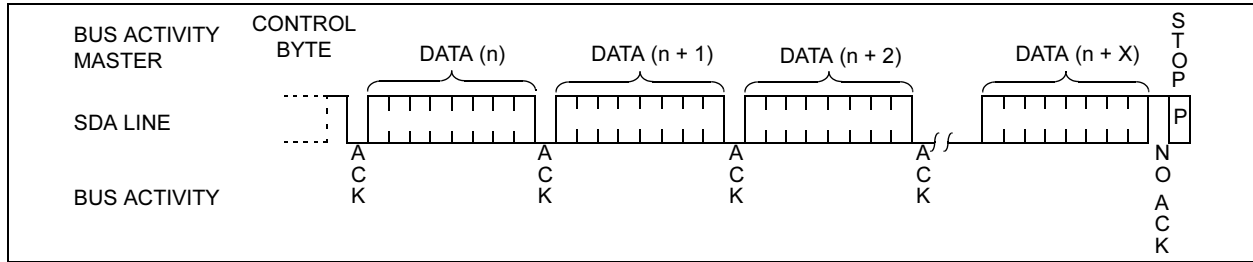


FIGURE 8-3: SEQUENTIAL READ

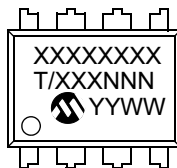


24AA512/24LC512/24FC512

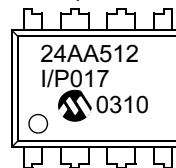
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

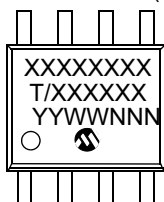
8-Lead PDIP (300 mil)



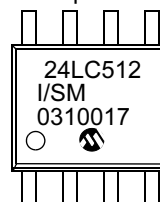
Example:



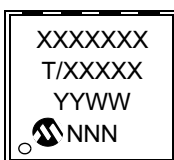
8-Lead SOIC (208 mil)



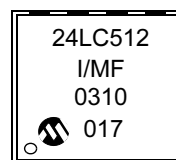
Example:



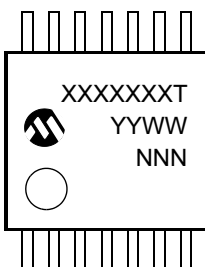
8-Lead DFN-S



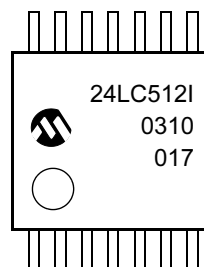
Example:



14-Lead TSSOP



Example:

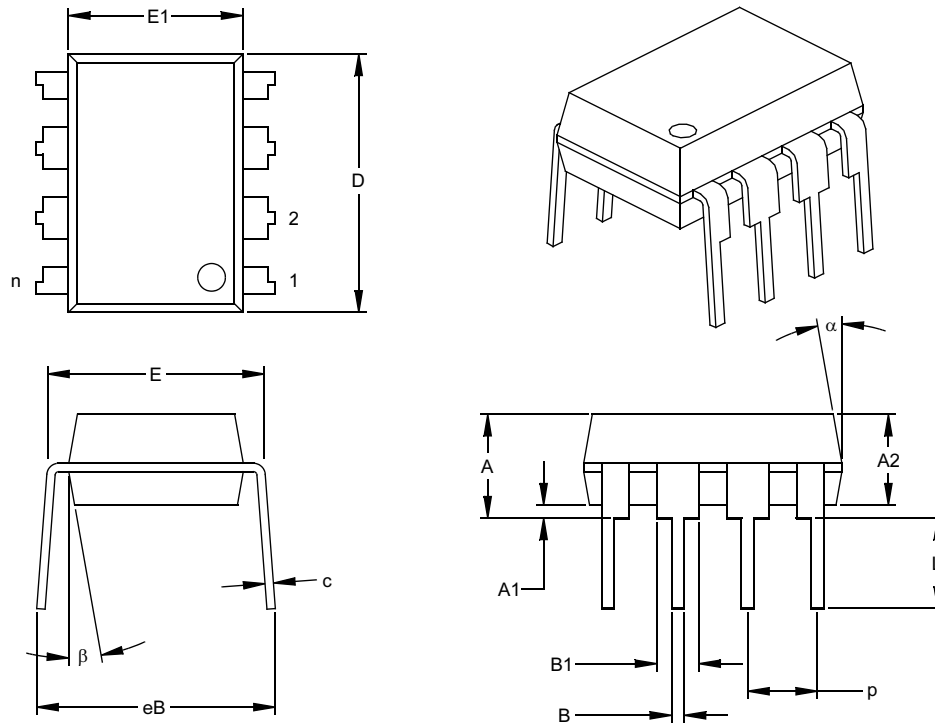


Legend:	XX...X	Customer specific information*
	T	Temperature grade (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.		

*Standard device marking consists of Microchip part number, year code, week code, and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

24AA512/24LC512/24FC512

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

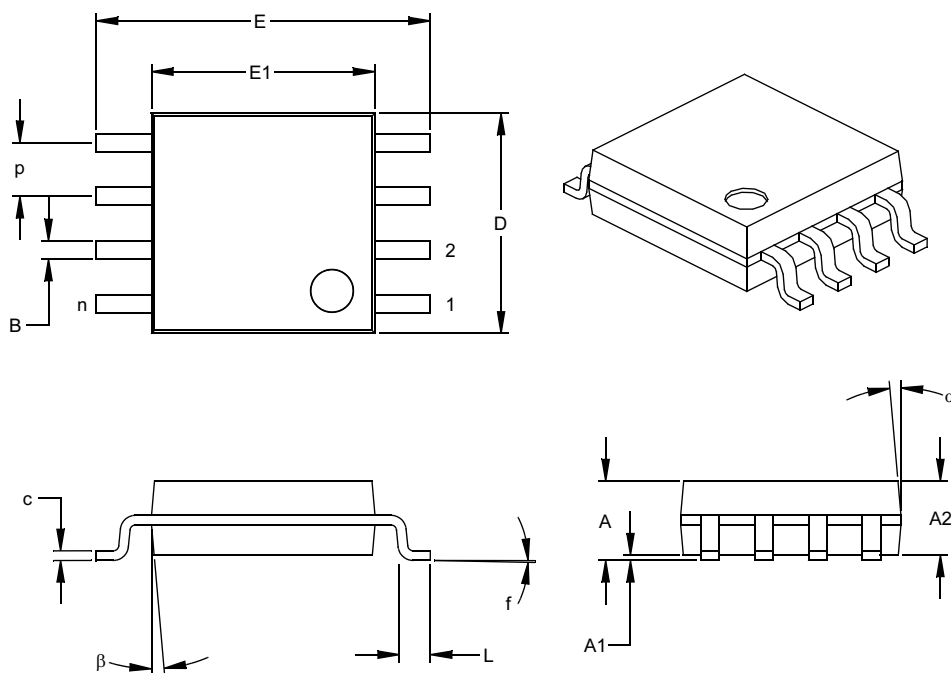
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

24AA512/24LC512/24FC512

8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff §	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

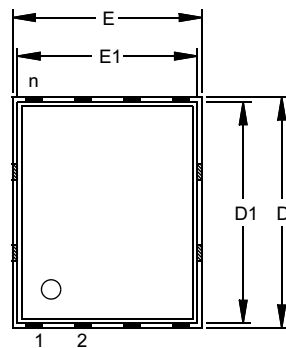
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

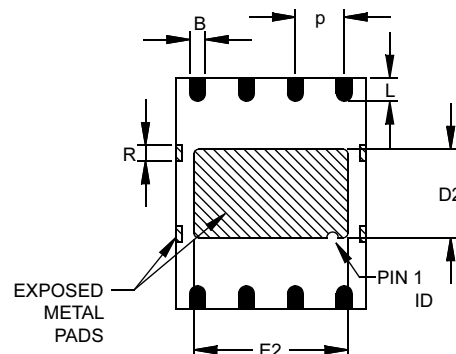
Drawing No. C04-056

24AA512/24LC512/24FC512

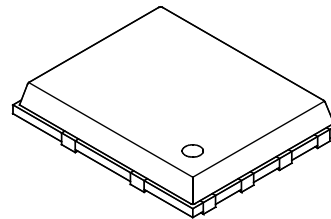
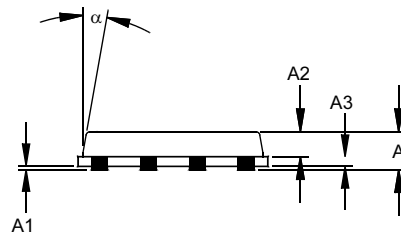
8-Lead Micro Lead Frame Package (MF) 6x5 mm Body (DFN-S) (Formerly MLF-S)



TOP VIEW



BOTTOM VIEW



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	P	.050 BSC			1.27 BSC		
Overall Height	A		.033	.039		0.85	1.00
Molded Package Thickness	A2		.026	.031		0.65	0.80
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.008 REF.			0.20 REF.		
Overall Length	E	.194 BSC			4.92 BSC		
Molded Package Length	E1	.184 BSC			4.67 BSC		
Exposed Pad Length	E2	.152	.158	.163	3.85	4.00	4.15
Overall Width	D	.236 BSC			5.99 BSC		
Molded Package Width	D1	.226 BSC			5.74 BSC		
Exposed Pad Width	D2	.085	.091	.097	2.16	2.31	2.46
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.020	.024	.030	0.50	0.60	0.75
Tie Bar Width	R		.014			.356	
Mold Draft Angle Top	α			12°			12°

*Controlling Parameter

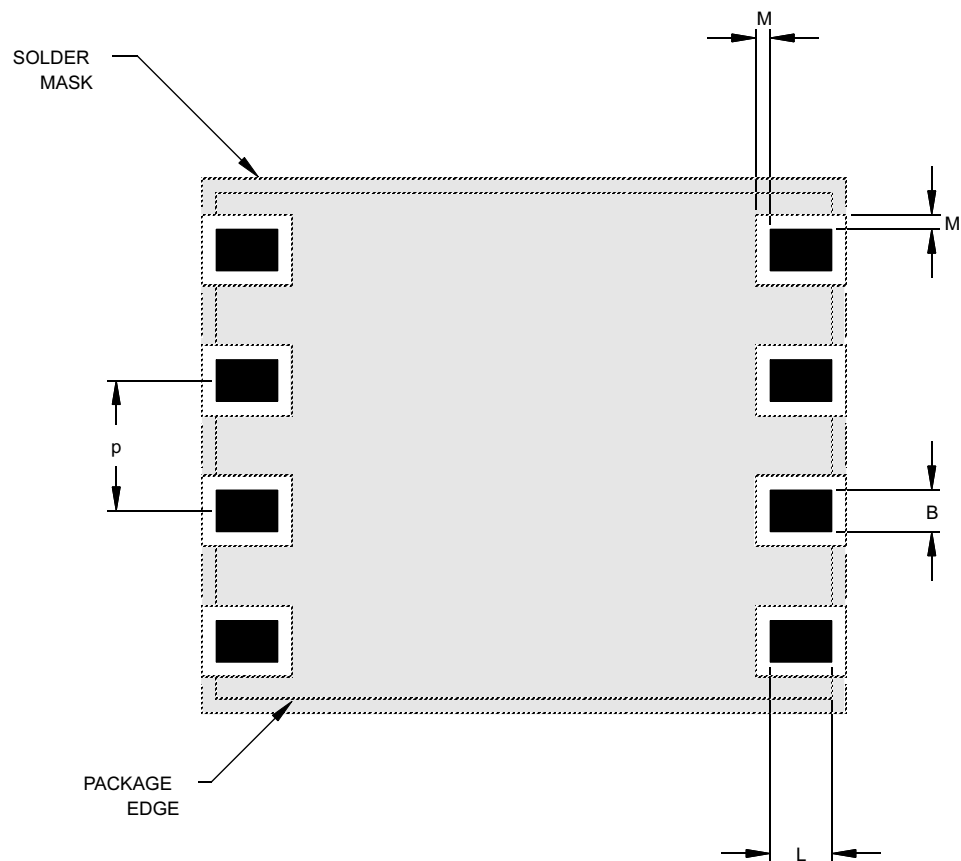
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC equivalent: pending

Drawing No. C04-113

24AA512/24LC512/24FC512

8-Lead Micro Leadframe Package (MF) 6x5 mm Body (DFN) (Continued)



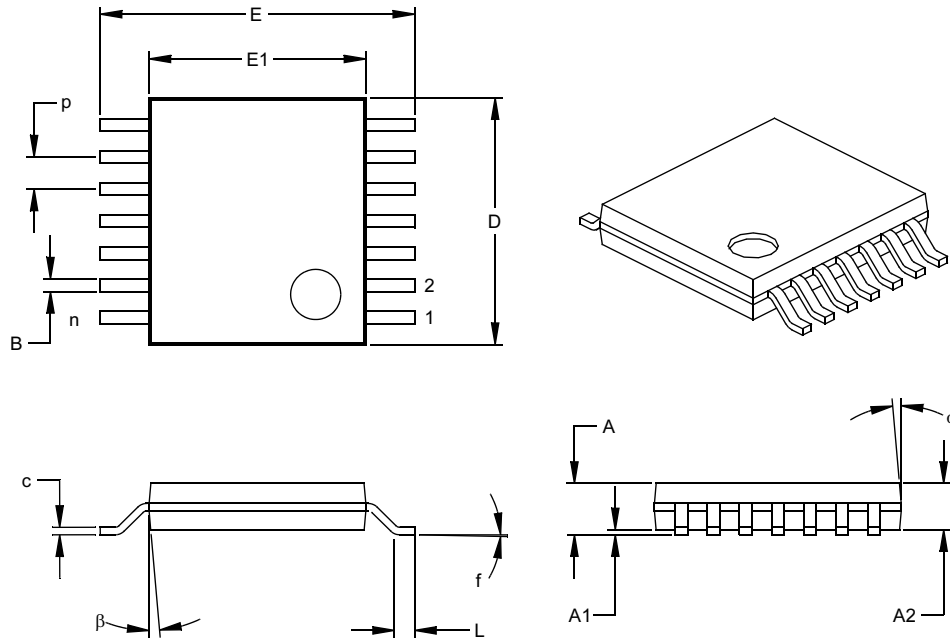
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	P	.050 BSC			1.27 BSC		
Pad Width	B	.014	.016	.019	0.35	0.40	0.47
Pad Length	L	.020	.024	.030	0.50	0.60	0.75
Pad to Solder Mask	M	.005		.006	0.13		0.15

*Controlling Parameter

Drawing No. C04-2113

24AA512/24LC512/24FC512

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

24AA512/24LC512/24FC512

NOTES:

24AA512/24LC512/24FC512

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>X</u>
Device	Temperature Range	Package	Lead Finish
Device:	24AA512:	512 Kbit 1.8V I ² C Serial EEPROM	
	24AA512T:	512 Kbit 1.8V I ² C Serial EEPROM (Tape and Reel)	
	24LC512:	512 Kbit 2.5V I ² C Serial EEPROM	
	24LC512T:	512 Kbit 2.5V I ² C Serial EEPROM (Tape and Reel)	
	24FC512:	512 Kbit 1 MHz I ² C Serial EEPROM	
	24FC512T:	512 Kbit 1 MHz I ² C Serial EEPROM (Tape and Reel)	
Temperature Range:	I = -40°C to +85°C		
	E = -40°C to +125°C		
Package:	P = Plastic DIP (300 mil body), 8-lead		
	SM = Plastic SOIC (208 mil body), 8-lead		
	ST14 = Plastic TSSOP (4.4 mm), 14-lead		
	MF = Micro Lead Frame (6x5 mm body), 8-lead		
Lead Finish	Blank = Standard 63%/37% Sn/Pb		
	G = Pb-free (Pure Matte Sn)		

Examples:

- a) 24AA512-I/P: Industrial Temp., 1.8V, PDIP package.
- b) 24AA512T-I/SM: Tape and Reel, Industrial Temp., 1.8V, SOIC package.
- c) 24AA512-I/ST14: Industrial Temp., 1.8V, 14-lead, TSSOP package.
- d) 24AA512-I/MF: Industrial Temp., 1.8V, DFN package.
- e) 24LC512-E/P: Extended Temp., 2.5V, PDIP package.
- f) 24LC512-I/SM: Industrial Temp., 2.5V, SOIC package.
- g) 24LC512T-I/SM: Tape and Reel, Industrial Temp., 2.5V, SOIC package.
- h) 24LC512-I/MF: Industrial Temp., 2.5V, DFN package.
- i) 24FC512-I/P: Industrial Temp., 2.5V, High Speed, PDIP package.
- j) 24FC512-I/SM: Industrial Temp., 2.5V, High Speed, SOIC package.
- k) 24FC512T-I/SM: Tape and Reel, Industrial Temp., 2.5V, High Speed, SOIC package
- l) 24LC512T-I/SM: Industrial Temp., 2.5V, SOIC package, Tape & Reel, Pb-free
- m) 24LC512-I/PG: Industrial Temp., 2.5V, PDIP package, Pb-free

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

24AA512/24LC512/24FC512

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELoQ, MPLAB, PIC, PICmicro, PICSTART, PRO MATE and PowerSmart are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AmpLab, FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

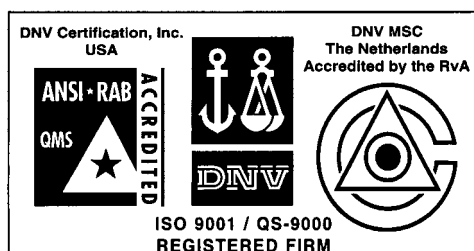
Application Maestro, dsPICDEM, dsPICDEM.net, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICKit, PICDEM, PICDEM.net, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rPIC, Select Mode, SmartSensor, SmartShunt, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2003, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

Phoenix

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966
Fax: 480-792-4338

San Jose

2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950
Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai

Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building
No. 2 Fengxiangnan Road, Ronggui Town
Shunde City, Guangdong 528303, China
Tel: 86-765-8395507 Fax: 86-765-8395571

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore

200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan

Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France

Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany

Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

07/28/03