

M62463AFP

Dolby Pro Logic Surround Decoder

REJ03F0275-0200

Rev.2.00

Jun 16, 2008

Description

The M62463AFP is a single chip Dolby Pro Logic surround decoder. This LSI has all of required functions for Dolby Pro Logic surround.

Note: Dolby and the double-D symbol are trademarks of Dolby laboratories licensing corporation. San Francisco, CA94103-4813, USA.

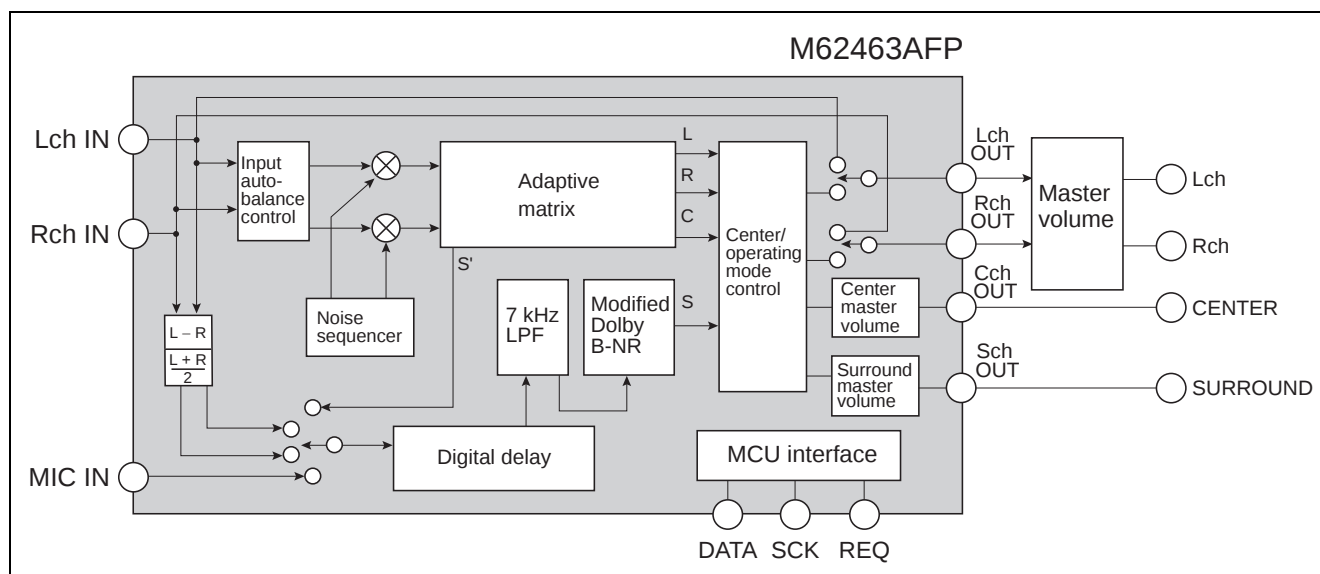
This device available only to licensees of Dolby Lab.

Licensing and application information may be obtained from Dolby Lab.

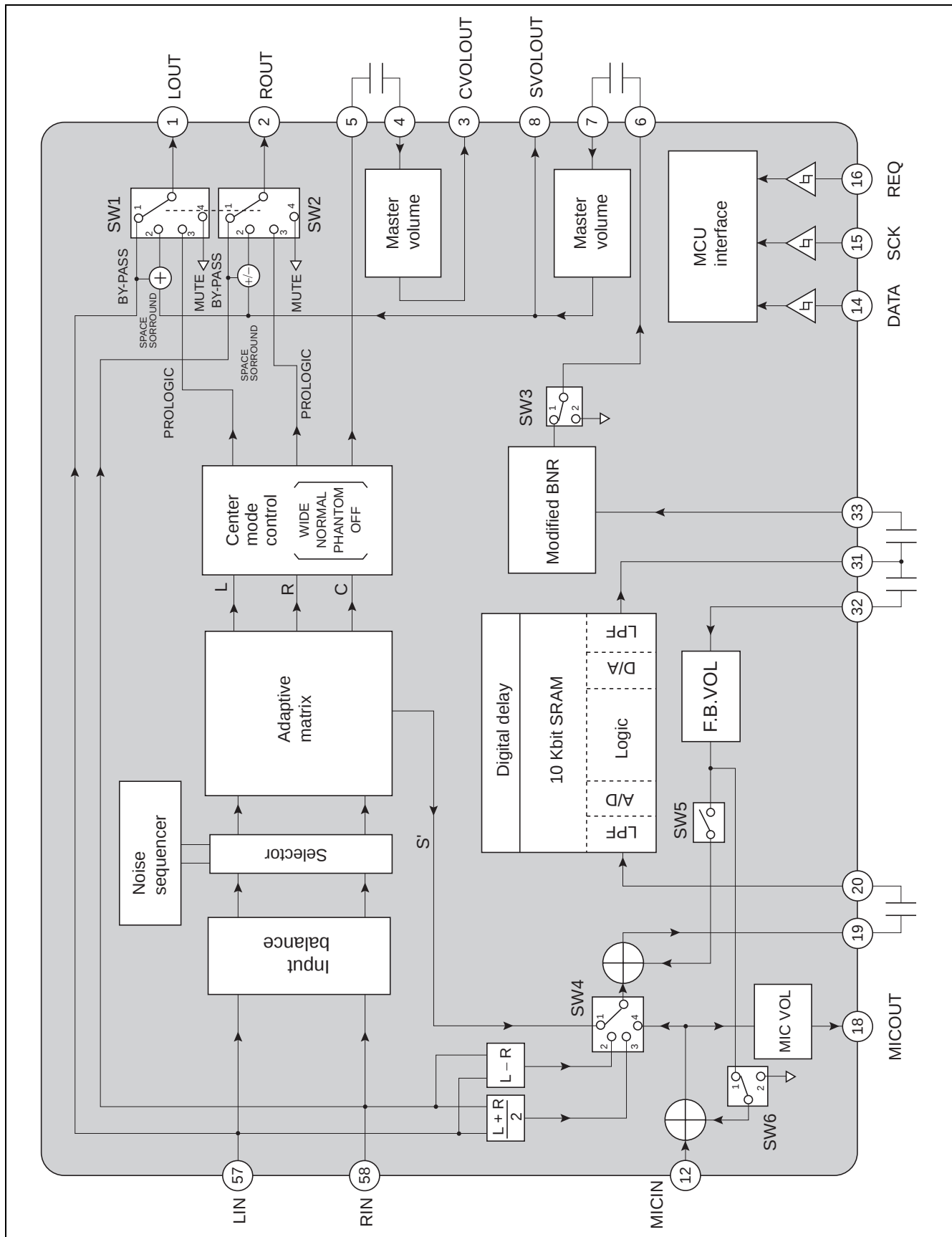
Features

- Includes all functions necessary for Dolby Pro Logic surround
 - Adaptive matrix
 - Input auto-balance
 - Noise sequencer
 - Center mode control ON/OFF, WIDE/NORMAL/PHANTOM
 - Modified Dolby B type noise reduction
 - 4 channel (Lch/Rch/Cch/Sch) / 3 channel (Lch/Rch/Cch)
 - Digital delay Delay time: 15.4 to 51.2 ms
- Cch/Sch master volume: 0 to -87 dB / 1 dB step, $-\infty$
- 3-lines MCU control
- Space surround such as Disco, Hall and Live
- Digital echo for Karaoke function Delay time: 123,184 ms
- Current control oscillation circuit for system clock

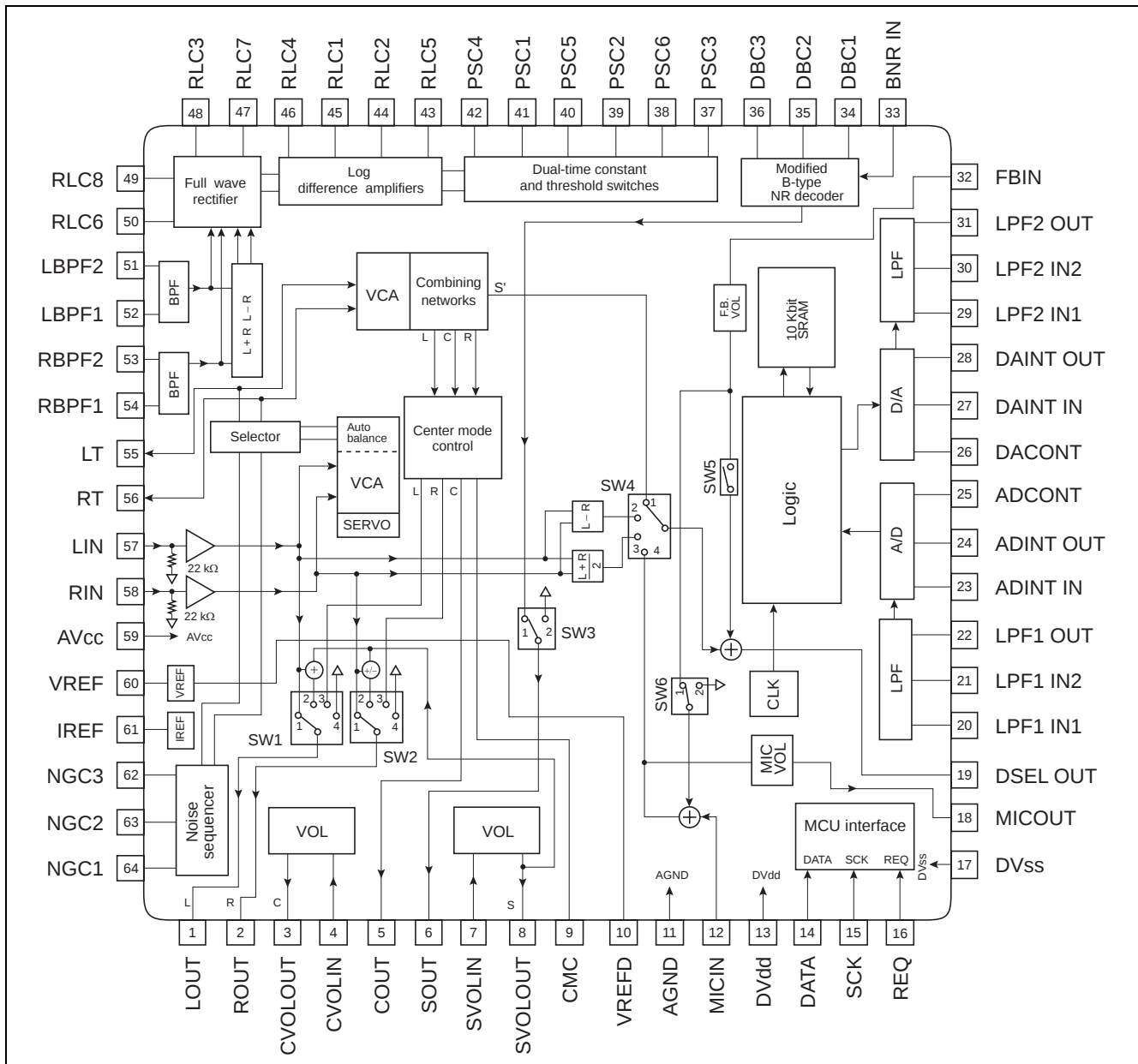
System Configuration



Block Diagram



Pin Arrangement



Functional Description

Function		Description
1	Fundamental function for Dolby Pro Logic surround decoder	Adaptive matrix Input auto-balance Noise sequencer Center mode control ON/OFF WIDE/NORMAL/PHANTOM Modified Dolby B type noise reduction 4 ch (L, R, C, S), 3 ch (L, R, C) mode switch
2	RAM for digital delay	10-Kbit RAM
3	Surround delay time	15.4, 20.5, 25.6, 29.2 ms (for Dolby Pro Logic surround) 51.2 ms (for space surround)
4	Circuit for space surround	Digital delay circuit can be used for space surround such as a Disco, Hall or Live, and Karaoke echo
5	Echo delay time	123,184 ms
6	Feedback volume	Delay signal feedback volume −3 to −21 dB / 3 dB step, and $-\infty$
7	Microphone volume	Internal microphone volume 0 to −18 dB / 3 dB step, and $-\infty$
8	Cch/Sch master volume	0 to −87 dB / 1 dB step, and $-\infty$
9	Bypass switch	Bypass the decode circuit
10	Output mute	Mute the Lch and Rch output
11	MCU interface	Controlled by 3-lines serial data from MCU Including the chip address (2-bit)
12	Current control oscillation circuit	Including the oscillation circuit without external parts

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	10.5	V
	Vdd	6.5	V
Power dissipation	Pd	1	W
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Condition

Item	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage	Vcc	8	9	10	V	
	Vdd	4.5	5	5.5	V	
Input voltage (L)	V _{IL}	0	—	0.8	V	14, 15, 16 pin
Input voltage (H)	V _{IH}	Vdd – 1	—	Vdd	V	14, 15, 16 pin

Electrical Characteristics

(Ta = 25°C, Vcc = 9 V, Vdd = 5 V, Cch volume = 0 dB, at C-OUT 0 dBd = 300 mVrms, f = 1 kHz, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Total						
Circuit current	I _{CC}	—	25	40	mA	No signal
Circuit current	I _{DD}	—	13	25	mA	No signal
Auto-Balance						
Capture range	CPR	—	5	—	dB	
Error correction	CER	—	4	—	dB	
Adaptive Matrix						
Output level accuracy relative to Cch	ΔVoL	−0.5	0	0.5	dB	L, R, Sch output
Matrix rejection	MR	25	40	—	dB	L, R, C, Sch output
Head room	HRAM	15	17	—	dB	L, R, C, Sch output
Total harmonic distortion	THDAM	—	0.05	0.2	%	L, R, Cch output, 30 kHzLPF
S/N ratio	SNAM	70	80	—	dB	Rg = 0 Ω, weighted CCIR/ARM, 4 ch mode
Noise Sequencer						
Output noise level	Vno	−15	−12.5	−10	dB	L, R, C, Sch output
Noise level accuracy relative to Cch	ΔVno	−0.5	0	0.5	dB	L, R, Sch output
Modified B Noise Reduction (Sch volume = 0 dB, 0 dB reference is 300 mVrms/100 Hz at S-Out)						
Gain between input and output	VGNR	—	5.1	—	dB	Vin = 0 dBd, f = 100 Hz
Decode character 1	DEC1	−1.6	−0.1	1.4	dB	Vin = 0 dBd, f = 1.0 kHz
Decode character 2	DEC2	−3.0	−1.5	0		Vin = −15 dBd, f = 1.4 kHz
Decode character 3	DEC3	−4.9	−3.4	−1.9		Vin = −20 dBd, f = 1.4 kHz
Decode character 4	DEC4	−6.8	−5.3	−3.8		Vin = −40 dBd, f = 5.0 kHz
Total harmonic distortion	THDNR	—	0.07	0.3	%	Vin = 0 dBd, f = 1 kHz, 30 kHzLPF
Head room	HRNR	15	17	—	dB	THD = 1%
S/N ratio	SNNR	68	78	—	dB	Rg = 0 Ω, weighted CCIR/ARM
Cch/Sch Master Volume						
Maximum attenuator	ATTmax	—	−95	−87	dB	ATT = −∞, Vi = 2 Vrms
Minimum attenuator	ATTmin	−3.0	0	3.0	dB	ATT = 0 dB
Volume step	VOLS1	0.5	1.0	1.5	dB	ATT = 0 to −40 dB
	VOLS2	0.2	1.0	1.8	dB	ATT = −40 to −87 dB
Volume cross-talk	CTVOL	68	83	—	dB	R input/CVOL, SVOL output
Output noise voltage	VnoVOL	—	2.6	5.2	μVrms	ATT = −∞
Line (Bypass mode)						
Total harmonic distortion	THDLN	—	0.002	0.05	%	L, Rch output, 30 kHzLPF
S/N ratio	SNLN	95	100	—	dB	L, Rch output
Line cross-talk	CTLN	70	80	—	dB	L input/R output, R input/L output
Input impedance	Zi	11	22	44	kΩ	

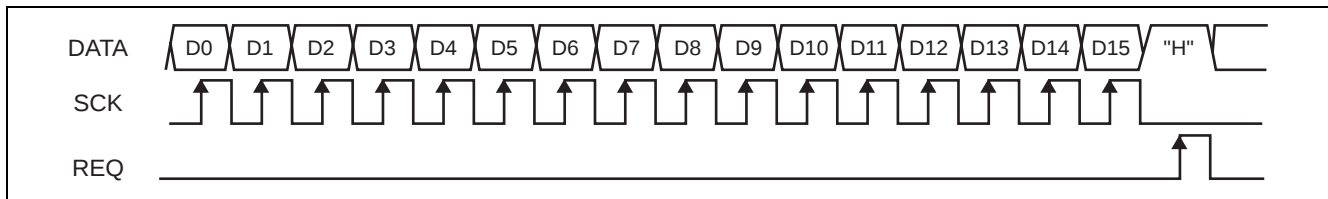
(Ta = 25°C, Vcc = 9 V, Vdd = 5 V, Vin = 200 mVrms, f = 1 kHz, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Digital Delay							
Input/output voltage gain	GvD	-8.1	-5.1	-2.1	dB	LIN-LPF2OUT, surround L – R	
Delay time	Td	17.4	20.5	23.6	ms	Td = 20.5 ms	
Total harmonic distortion	THDD	—	0.5	0.9	%	30 kHz LPF	Td = 20.5 ms
		—	1.2	2.2			Td = 51.2 ms
		—	3.0	5.6			Td = 184 ms
Output noise voltage	NoD	—	-92	-80	dBV	Vin = 0 Vrms JIS-A	Td = 20.5 ms
		—	-84	-70			Td = 51.2 ms
		—	-80	-65			Td = 184 ms
Maximum output voltage	Vomax	0.7	1.0	—	Vrms	THD = 10%	
LPF cut-off frequency	LPFfc	6.0	7.0	8.0	kHz	Td = 15.4 to 51.2 ms Gv = -3 dB (Dolby Pro Logic mode)	
		—	3.0	—	kHz	Td = 123,184 ms (Echo mode) Gv = -3 dB	
Feedback Volume							
Maximum attenuation	FBATTmax	—	-70	-60	dB	ATT = -∞	
Minimum attenuation	FBATTmin	-6.0	-3.0	0	dB	ATT = -3 dB	
Volume step	FBVOLS	—	3.0	—	dB		
Microphone Volume							
Maximum attenuation	MICATTmax	—	-70	-60	dB	ATT = -∞	
Minimum attenuation	MICATTmin	-3.0	0	3.0	dB	ATT = 0 dB	
Volume step	MICVOLS	—	3.0	—	dB		
Output noise voltage	VnoMIC	—	2.0	4.0	μVrms	ATT = -∞	

Serial Data Control Format

(1) Data input format

DATA is read at the rising edge of SCK, and loaded last 16 bits at the rising edge of REQ.



D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
L	L	Mode set		Pro Logic mode	Center mode		Sch volume							L	H
	H	Delay time			Auto- balance	set to "L"	Cch volume								
H	L	Noise sequencer			Surround/echo mode										
	H	Test mode (user inhibit)													

(2) Control condition

No.	Control Mode	Contents
1	Mode set	Normal stereo/Dolby Pro Logic/space surround or echo/mute
2	Pro Logic mode	4 ch Pro Logic/3 ch stereo
3	Center mode	Wide/Normal/Phantom/OFF
4	Delay time	15.4, 20.5, 25.6, 29.2, 51.2 ms (for surround) 123,184 ms (for echo)
5	Auto-balance	Input auto-balance ON/OFF
6	Noise sequencer	ON/OFF Lch/Rch/Cch/Sch
7	Surround/echo mode	Delay input $L - R / (L + R) / 2$ / MICin Feedback volume, microphone volume, delay output mixing
8	Cch/Sch volume	0 to -87 dB / 1 dB step, and $-\infty$
9	Chip address	Input data effect or not

(3) Set conditions

Mode Setting (D0 = "L", D1 = "L")

D2	D3	Condition
L	L	Normal stereo (bypass)
L	H	Dolby Pro Logic surround
H	L	Space surround/echo
H	H	Output mute

Pro Logic Mode Setting (D0 = "L", D1 = "L")

D4	Condition
L	4 ch Pro Logic
H	3 ch stereo

Center Mode Setting (D0 = "L", D1 = "L")

D5	D6	Condition
L	L	Wide
L	H	Normal
H	L	Phantom
H	H	OFF

Delay Time Setting (D0 = "L", D1 = "H")

D2	D3	D4	Delay Time	Sampling Frequency	LPF Cutoff Frequency
L	L	L	15.4 ms	500 kHz	7 kHz
L	L	H	20.5 ms	500 kHz	
L	H	L	25.6 ms	400 kHz	
L	H	H	29.2 ms	333 kHz	
H	L	L	51.2 ms	200 kHz	
H	L	H	123 ms	83.3 kHz	3 kHz
H	H	L	184 ms	55.6 kHz	

Auto-Balance Setting (D0 = "L", D1 = "H")

D5	Condition
L	Auto-balance OFF
H	Auto-balance ON

Noise Sequencer (D0 = "H", D1 = "L")

D2	D3	D4	Condition	
L	—	—	Noise sequencer OFF	
H	L	L	Noise sequencer ON	Lch
	L	H		Rch
	H	L		Cch
	H	H		Sch

Surround/Echo Mode (D0 = "H", D1 = "L")**Surround/Echo Mode Switch**

D5	Condition
L	Surround
H	Echo

Delay Input

D6	Delay Input
L	L – R
H	(L + R) / 2

Delay Mixing Polarity

D7	Mixing Polarity
L	L+ delay signal/R+ delay signal
H	L+ delay signal/R– delay signal

Feedback Volume

D8	D9	D10	Volume
L	L	L	–3 dB
L	L	H	–6 dB
L	H	L	–9 dB
L	H	H	–12 dB
H	L	L	–15 dB
H	L	H	–18 dB
H	H	L	–21 dB
H	H	H	–∞

Microphone Volume

D11	D12	D13	Volume
L	L	L	0 dB
L	L	H	–3 dB
L	H	L	–6 dB
L	H	H	–9 dB
H	L	L	–12 dB
H	L	H	–15 dB
H	H	L	–18 dB
H	H	H	–∞

Relation Between Mode Setting and Switch Condition

Mode Setting	Pro Logic Mode (D0 = L, D1 = L)	Surround/Echo Mode (D0 = H, D1 = L)		Switch Condition					
	D4	D5	D6	SW1	SW2	SW3	SW4	SW5	SW6
Normal stereo (bypass)	X	X	X	1	1	2	4	OFF	2
Dolby Pro Logic surround	L	X	X	3	3	1	1	OFF	2
	H					2			
Space surround/echo	X	L	L	2	2	1	2	ON	2
		(Surround)	H	Delay mixing ON			3		
	X	H	X	1	1	2	4	OFF	1
		(Echo)		Delay mixing OFF					
Mute	X	X	X	4	4	2	4	OFF	2

Note: X: L or H

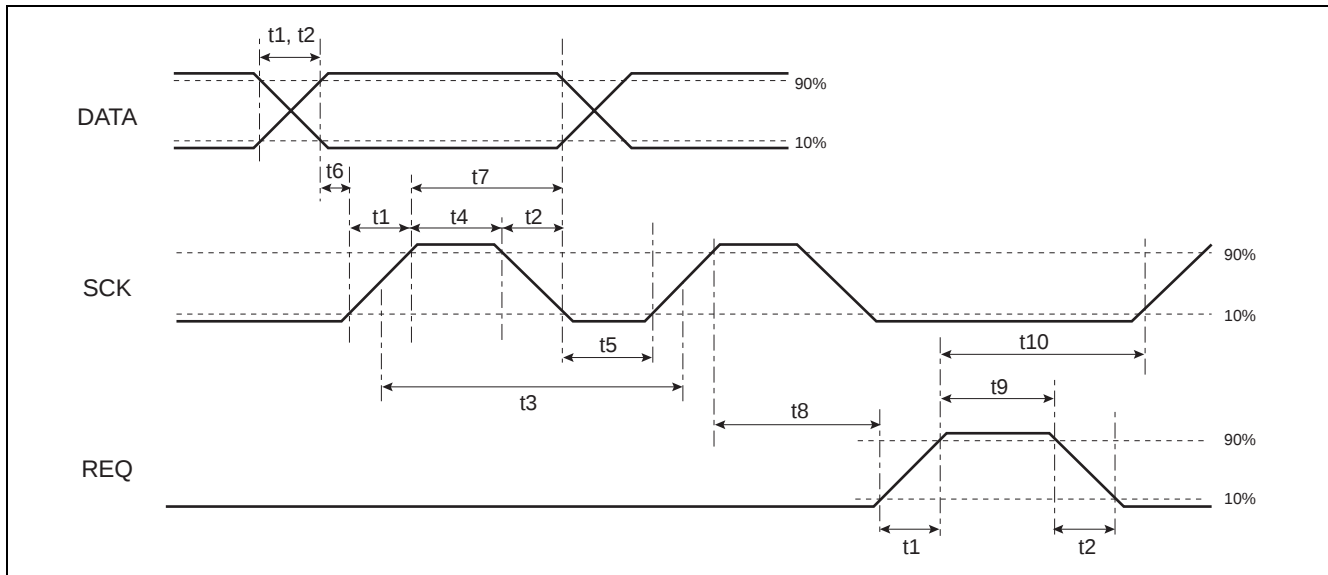
Sch Volume Setting (D0 = "L", D1 = "L"), Cch Volume Setting (D0 = "L", D1 = "H")

Volume Level	D7	D8	D9	D10	D11	Volume Level	D12	D13
0 dB	L	L	L	L	L	0 dB	L	L
-2 dB	L	L	L	L	H	-1 dB	L	H
-4 dB	L	L	L	H	L	-2 dB	H	L
-6 dB	L	L	L	H	H	-3 dB	H	H
-8 dB	L	L	H	L	L			
-10 dB	L	L	H	L	H			
-12 dB	L	L	H	H	L			
-14 dB	L	L	H	H	H			
-16 dB	L	H	L	L	L			
-18 dB	L	H	L	L	H			
-20 dB	L	H	L	H	L			
-22 dB	L	H	L	H	H			
-24 dB	L	H	H	L	L			
-26 dB	L	H	H	L	H			
-28 dB	L	H	H	H	L			
-30 dB	L	H	H	H	H			
-32 dB	H	L	L	L	L			
-34 dB	H	L	L	L	H			
-36 dB	H	L	L	H	L			
-40 dB	H	L	L	H	H			
-44 dB	H	L	H	L	L			
-48 dB	H	L	H	L	H			
-52 dB	H	L	H	H	L			
-56 dB	H	L	H	H	H			
-60 dB	H	H	L	L	L			
-64 dB	H	H	L	L	H			
-68 dB	H	H	L	H	L			
-72 dB	H	H	L	H	H			
-76 dB	H	H	H	L	L			
-80 dB	H	H	H	L	H			
-84 dB	H	H	H	H	L			
-∞	H	H	H	H	H			

Chip Address

D14	D15	Data Read
L	H	Enable
Others		Unable

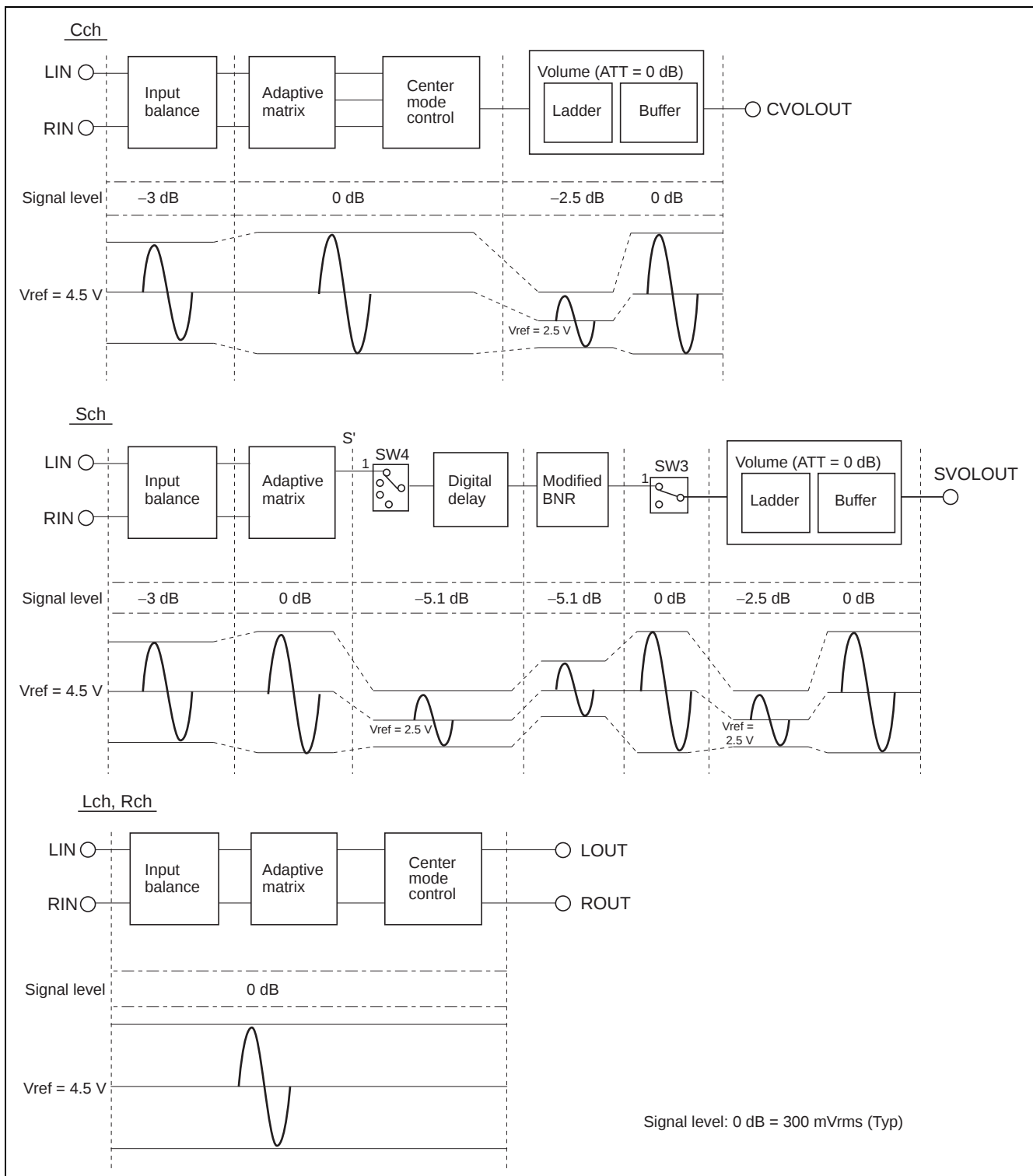
(4) Data timing



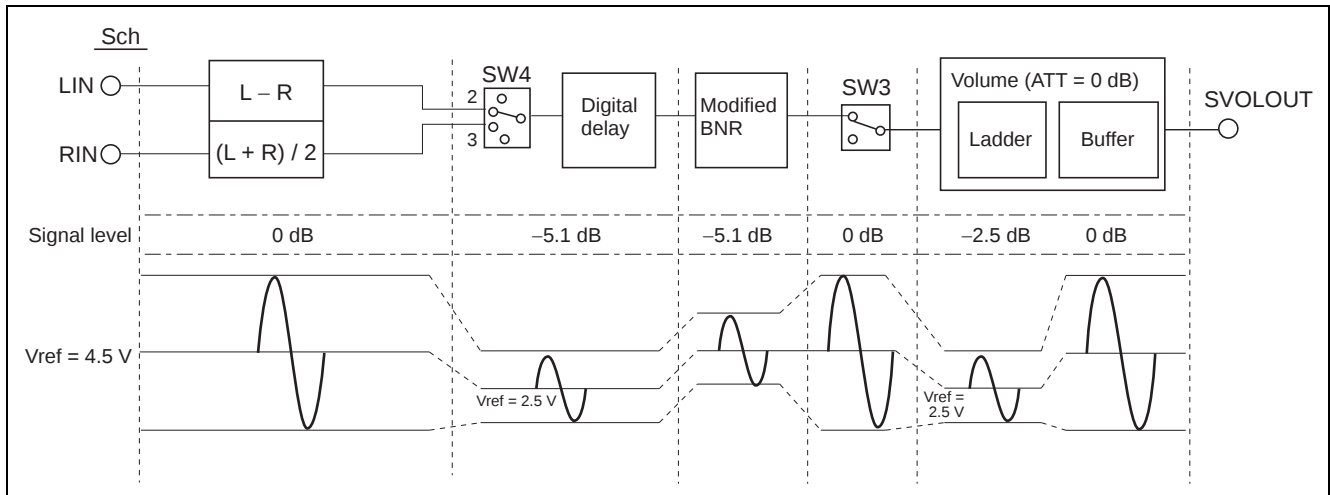
Symbol	Name	Min	Typ	Max	Unit
t1	Signal rise time	—	—	0.5	μ S
t2	Signal fall time	—	—	0.5	μ S
t3	SCK clock width	2	—	—	μ S
t4	SCK "H" pulse width	0.8	—	—	μ S
t5	SCK "L" pulse width	0.8	—	—	μ S
t6	DATA setup time	0.8	—	—	μ S
t7	DATA hold time	0.8	—	—	μ S
t8	REQ rise hold time	1.6	—	—	μ S
t9	REQ "H" pulse width	0.8	—	—	μ S
t10	SCK setup time	1.6	—	—	μ S

Level Diagram

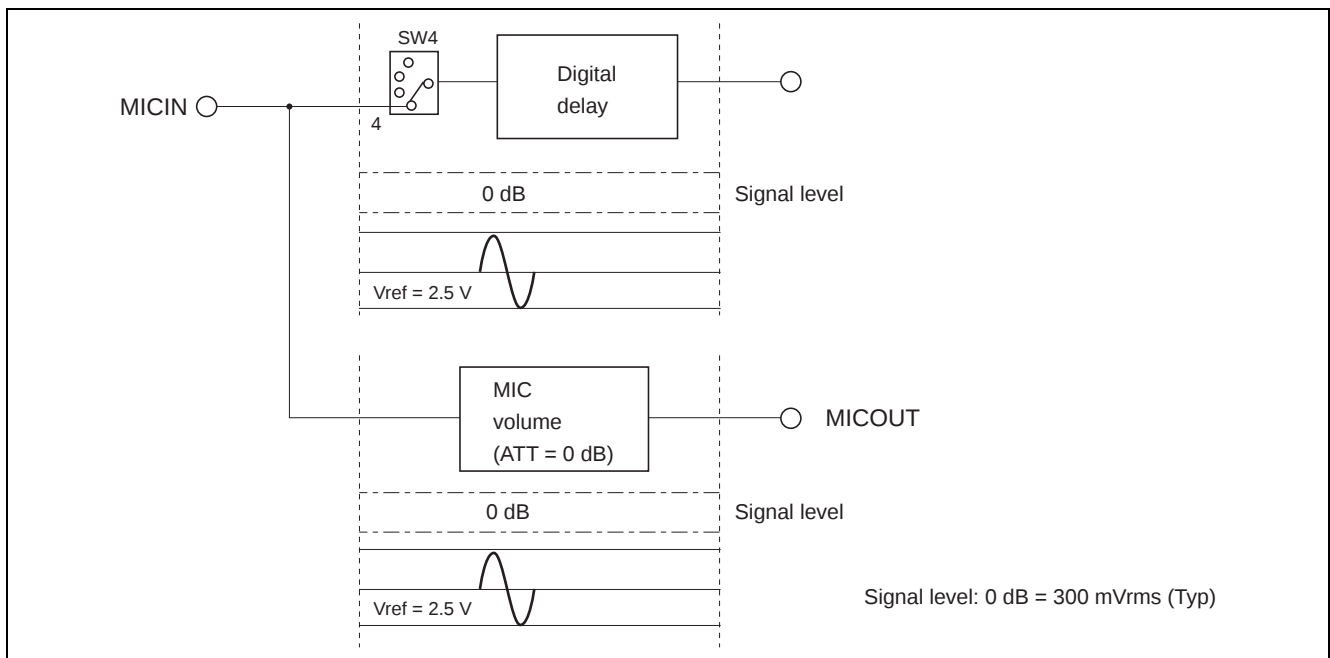
(1) Dolby Pro Logic surround mode



(2) Space surround mode



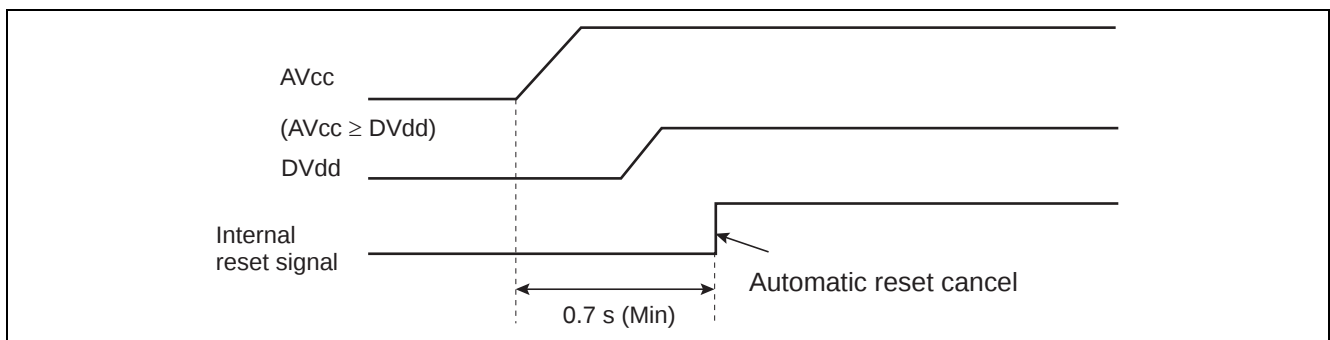
(3) Echo mode



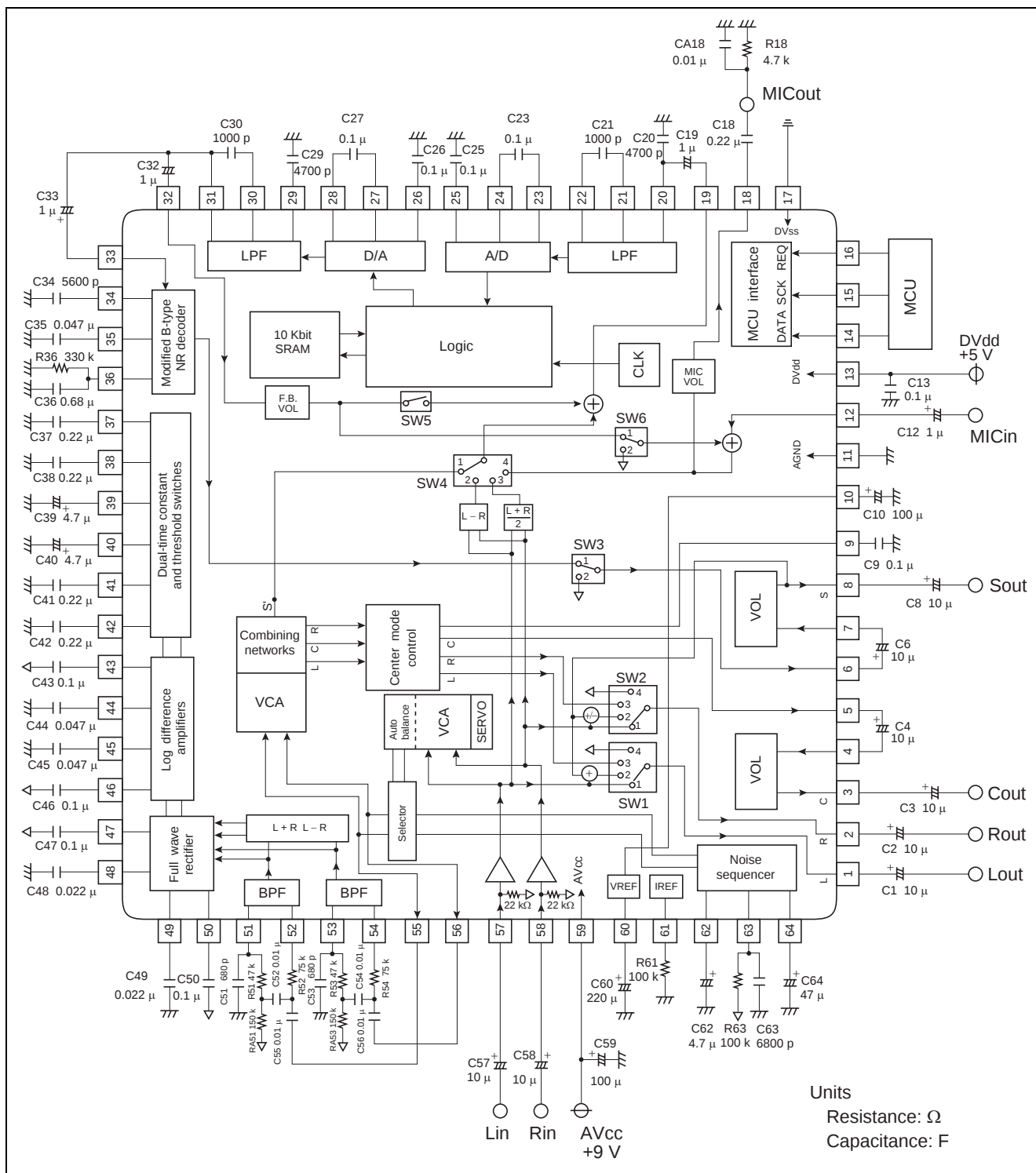
Notice

Relation AVcc and DVdd at power supply

Digital Vdd must be supplied less than 0.7 seconds from analog Vcc supply.



Application Example

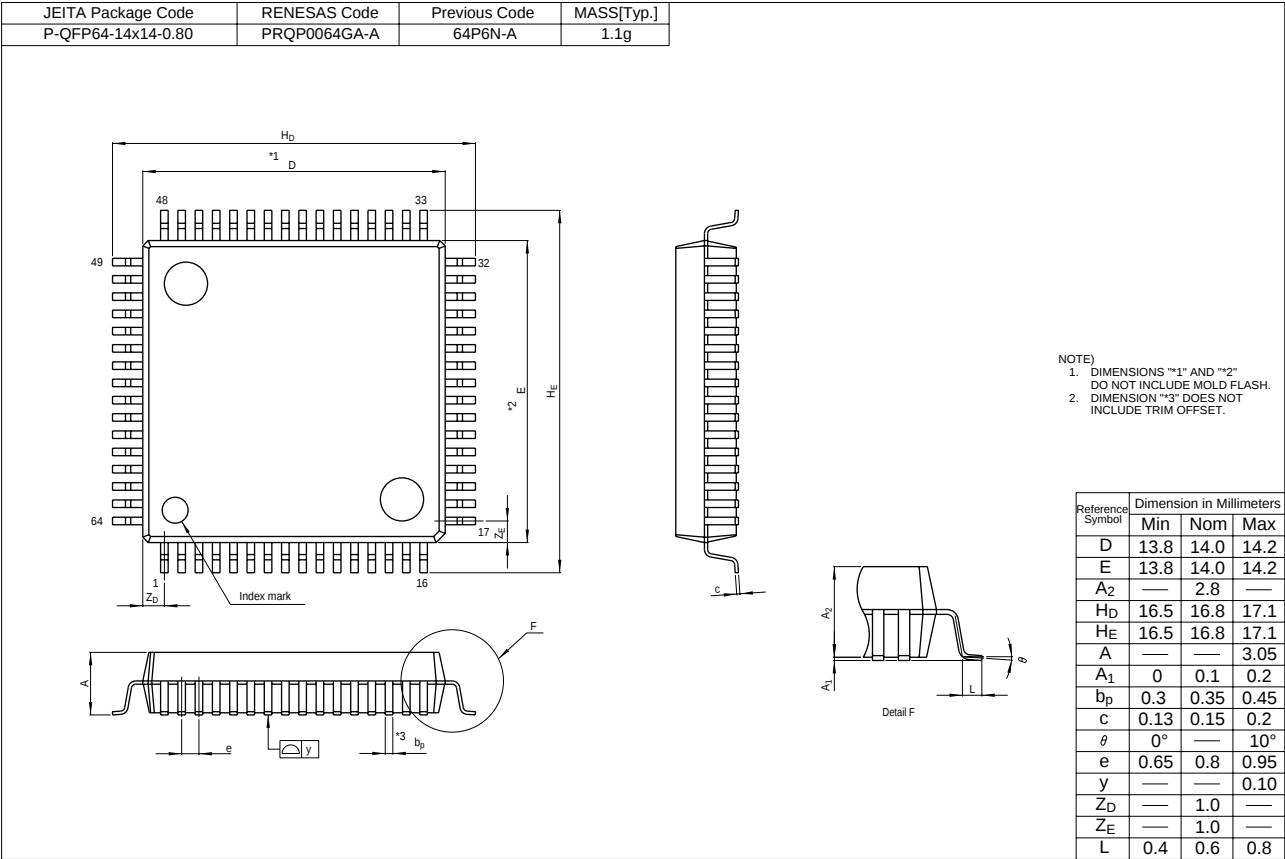


External Parts List

Parts No.	Values	Unit	Tol.
C1	10	μF	
C2	10	μF	
C3	10	μF	
C4	10	μF	
C6	10	μF	
C8	10	μF	
C9	0.1	μF	10%
C10	100	μF	
C12	10	μF	
C13	0.1	μF	
C18	0.22	μF	
CA18	0.01	μF	
C19	1.0	μF	non-polar
C20	4700	pF	5%
C21	1000	pF	5%
C23	0.1	μF	5%
C25	0.1	μF	5%
C26	0.1	μF	5%
C27	0.1	μF	5%
C29	4700	μF	5%
C30	1000	pF	5%
C32	1.0	μF	
C33	1.0	μF	
C34	5600	pF	5%
C35	0.047	μF	5%
C36	0.68	μF	10%
C37	0.22	pF	10%
C38	0.22	pF	10%
C39	4.7	μF	20%
C40	4.7	μF	20%
C41	0.22	μF	10%
C42	0.22	μF	10%
C43	0.1	μF	20%
C44	0.047	μF	5%
C45	0.047	μF	5%
C46	0.1	μF	20%

Parts No.	Values	Unit	Tol.
C47	0.1	μF	20%
C48	0.022	μF	5%
C49	0.022	μF	5%
C50	0.1	μF	20%
C51	680	pF	5%
C52	0.01	μF	5%
C53	680	pF	5%
C54	0.01	μF	5%
C55	0.01	μF	5%
C56	0.01	μF	5%
C57	10	μF	
C58	10	μF	
C59	100	μF	
C60	220	μF	
C62	4.7	μF	10%
C63	6800	pF	5%
C64	47	μF	
R18	4.7	$\text{k}\Omega$	10%
R36	330	$\text{k}\Omega$	10%
R51	47	$\text{k}\Omega$	5%
RA51	150	$\text{k}\Omega$	5%
R52	75	$\text{k}\Omega$	5%
R53	47	$\text{k}\Omega$	5%
RA53	150	$\text{k}\Omega$	5%
R54	75	$\text{k}\Omega$	5%
R61	100	$\text{k}\Omega$	1%
R63	100	$\text{k}\Omega$	5%

Package Dimensions



Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510