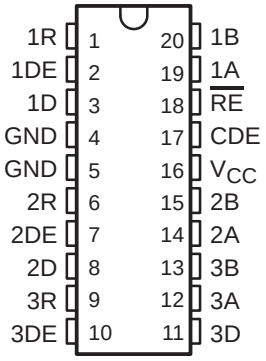
SLLS056D – AUGUST 1987 – REVISED SEPTEMBER 1995

- **Three Bidirectional Transceivers**
- **Driver Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **Two Skew Limits Available**
- **Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Pulse Skew . . . 5 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Features Independent Driver Enables and Combined Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±300 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

**DW OR J PACKAGE**
**(TOP VIEW)**




## description

The SN75ALS171 and the SN75ALS171A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines, and each driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the drivers and receivers meet ITU Recommendation V.11. The SN75ALS171A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

The SN75ALS171 and the SN75ALS171A operate from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC}$ is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS171 and the SN75ALS171A are characterized for operation from 0°C to 70°C.

## Function Tables

**EACH DRIVER**

| INPUT D | ENABLES | | OUTPUTS | |
|---|---|---|---|---|
| | DE | CDE | A | B |
| H | H | H | H | L |
| L | H | H | L | H |
| X | L | X | Z | Z |
| X | X | L | Z | Z |

**EACH RECEIVER**

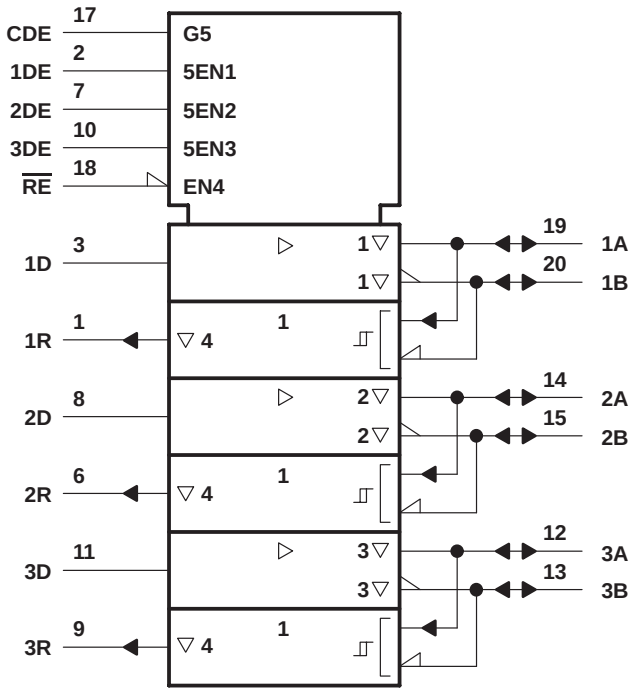
| DIFFERENTIAL INPUTS A – B | ENABLE $\overline{RE}$ | OUTPUT R |
|---|---|---|
| $V_{ID} \geq 0.3$ V | L | H |
| $-0.3$ V $< V_{ID} < 0.3$ V | L | ? |
| $V_{ID} \leq -0.3$ V | L | L |
| X | H | Z |
| Open | L | H |

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

**AVAILABLE OPTIONS**

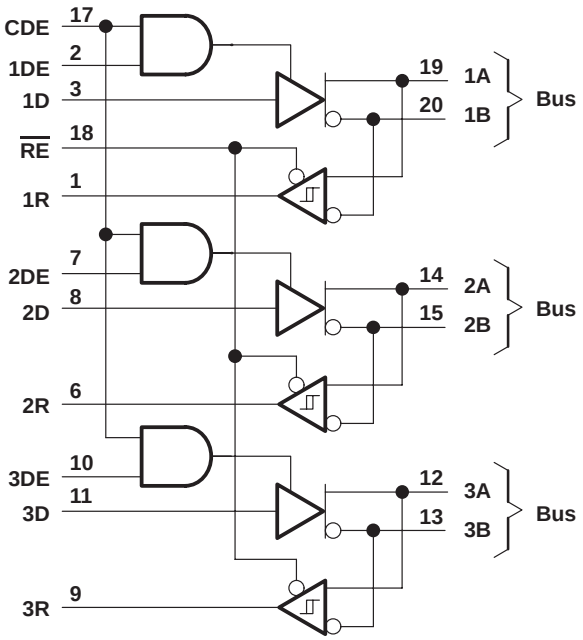
| SKEW LIMIT | PART NUMBER | |
|---|---|---|
| 10 ns | SN75ALS171DW | SN75ALS171J |
| 5 ns | SN75ALS171ADW | |

## logic symbol†

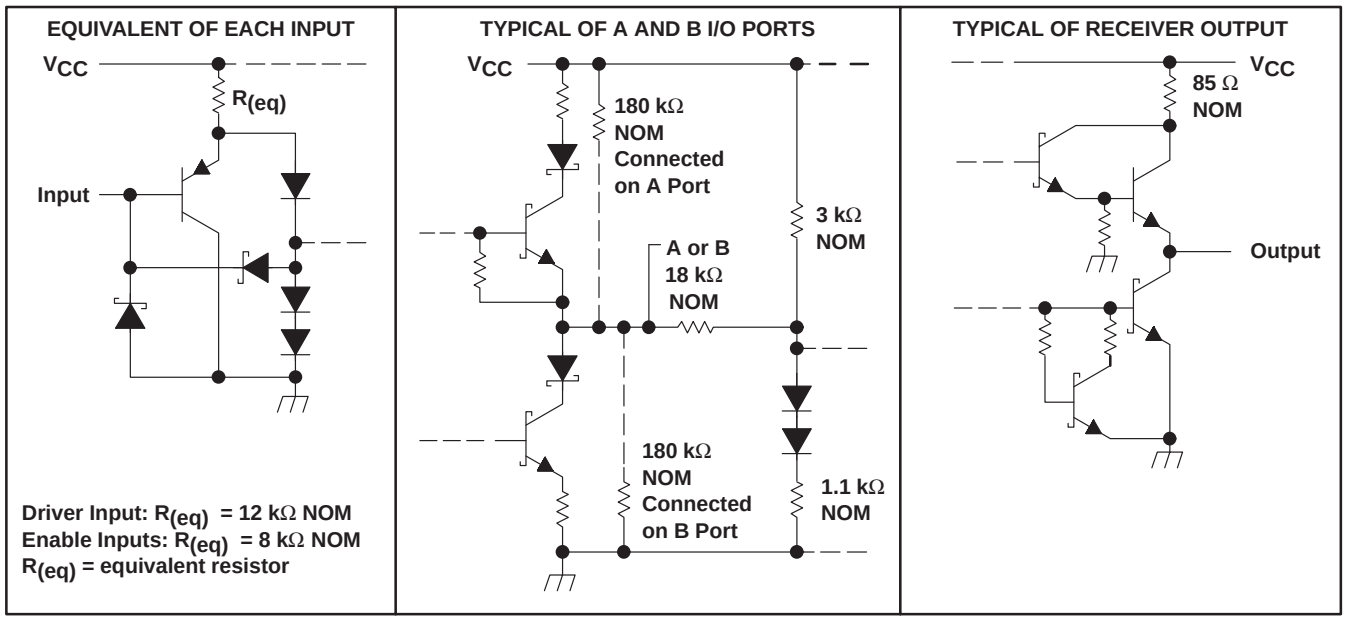



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . –7 V to 12 V
Enable input voltage, $V_I$ . . . . . 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$ | | –7 | | 12 | V |
| High-level input voltage, $V_{IH}$ | D, CDE, DE, and $\overline{RE}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | D, CDE, DE, and $\overline{RE}$ | | | 0.8 | V |
| Differential input voltage, $V_{ID}$ (see Note 2) | | | | ±12 | V |
| High-level output current, $I_{OH}$ | Driver | | | –60 | mA |
| | Receiver | | | –400 | µA |
| Low-level output current, $I_{OL}$ | Driver | | | 60 | mA |
| | Receiver | | | 8 | |
| Operating free-air temperature, $T_A$ | | 0 | | 70 | °C |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

## DRIVER SECTION

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I$ = –18 mA | | | | –1.5 | V |
| $V_O$ | Output voltage | $I_O$ = 0 | | 0 | | 6 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $I_{OH}$ = –55 mA | 2.7 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $I_{OL}$ = 55 mA | | | 1.7 | V |
| $\lvert V_{OD1}\rvert$ | Differential output voltage | $I_O$ = 0 | | 1.5 | | 6 | V |
| $\lvert V_{OD2}\rvert$ | Differential output voltage | $R_L$ = 100 Ω, | See Figure 1 | 1/2 $V_{OD1}$ or 2§ | 2.5 | 5 | V |
| | | $R_L$ = 54 Ω, | See Figure 1 | 1.5 | 2.5 | 5 | |
| $V_{OD3}$ | Differential output voltage | $V_{test}$ = –7 V to 12 V, | See Figure 2 | 1.5 | | 5 | V |
| $\Delta\lvert V_{OD}\rvert$ | Change in magnitude of differential output voltage¶ | $R_L$ = 54 Ω or 100 Ω, | See Figure 1 | | | ±0.2 | V |
| $V_{OC}$ | Common-mode output voltage | | | | | 3 | V |
| | | | | | | –1 | |
| $\Delta\lvert V_{OC}\rvert$ | Change in magnitude of common-mode output voltage¶ | | | | | ±0.2 | V |
| $I_O$ | Output current | Output disabled, See Note 3 | $V_O$ = 12 V | | | 1 | mA |
| | | | $V_O$ = –7 V | | | –0.8 | |
| $I_{IH}$ | High-level enable-input current | D and DE | $V_{IH}$ = 2.7 V | | | 20 | µA |
| | | CDE | | | | 60 | |
| $I_{IL}$ | Low-level enable-input current | D and DE | $V_{IL}$ = 0.4 V | | | –100 | |
| | | CDE | | | | –900 | |
| $I_{OS}$ | Short-circuit output current | $V_O$ = –6 V | | | | –250 | mA |
| | | $V_O$ = 0 | | | | –150 | |
| | | $V_O$ = $V_{CC}$ | | | | 250 | |
| | | $V_O$ = 8 V | | | | 250 | |
| $I_{CC}$ | Supply current | No load | Outputs enabled | | 69 | 90 | mA |
| | | | Outputs disabled | | 57 | 78 | |

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
§ The minimum $V_{OD2}$ with 100-W load is either 1/2 $V_{OD2}$ or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{d(OD)}$ | Differential output delay time | ALS171 | $R_L$ = 54 Ω, $C_L$ = 50 pF | See Figure 3, | 3 | | 13 | ns |
| | | ALS171A | | | 6 | | 11 | |
| | | ALS171 | $R_{L1} = R_{L3}$ = 165 Ω, $C_L$ = 60 pF, $R_{L2}$ = 75 Ω, | $V_{TERM}$ = 5 V, See Figure 6 | 3 | | 13 | |
| | | ALS171A | | | 6 | | 11 | |
| $t_{sk(p)}$ | Pulse skew‡ | | $R_L$ = 54 Ω, See Figure 3 | $C_L$ = 50 pF, | | 1 | 5 | ns |
| | | | $R_{L1} = R_{L3}$ = 165 Ω, $C_L$ = 60 pF, | $R_{L2}$ = 75 Ω, See Figure 6 | | 1 | 5 | ns |
| $t_{sk(lim)}$ | Skew limit§ | ALS171 | $R_L$ = 54 Ω, See Figure 3 | $C_L$ = 50 pF, | | | 10 | ns |
| | | ALS171A | | | | | 5 | |
| | | ALS171 | $R_{L1} = R_{L3}$ = 165 Ω, $C_L$ = 60 pF, | $R_{L2}$ = 75 Ω, See Figure 6 | | | 10 | |
| | | ALS171A | | | | | 5 | |
| $t_{t(OD)}$ | Differential-output transition time | | $R_L$ = 54 Ω, See Figure 3 | $C_L$ = 50 pF, | 3 | 8 | 13 | ns |
| | | | $R_{L1} = R_{L3}$ = 165 Ω, $C_L$ = 60 pF, See Figure 6 | $R_{L2}$ = 75 Ω, $V_{TERM}$ = 5 V, | 3 | 8 | 13 | |
| $t_{PZH}$ | Output enable time to high level | | $R_L$ = 110 Ω, | See Figure 4 | | 30 | 50 | ns |
| $t_{PZL}$ | Output enable time to low level | | $R_L$ = 110 Ω, | See Figure 5 | | 30 | 50 | ns |
| $t_{PHZ}$ | Output disable time from high level | | $R_L$ = 110 Ω, | See Figure 4 | 3 | 8 | 13 | ns |
| $t_{PLZ}$ | Output disable time from low level | | $R_L$ = 110 Ω, | See Figure 5 | 3 | 8 | 13 | ns |
| $t_{PDE}$ | Differential-output enable time | | $R_{L1} = R_{L3}$ = 165 Ω, $C_L$ = 60 pF, | $R_{L2}$ = 75 Ω, See Figure 7 | 8 | 30 | 45 | ns |
| $t_{PDZ}$ | Differential-output disable time | | | | 5 | 10 | 45 | ns |

† All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
‡ Pulse skew is defined as the $|t_{d(ODH)} - t_{d(ODL)}|$ of each channel.
§ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one $V_{CC}$ and operating temperature within the recommended operating conditions.

**SYMBOL EQUIVALENTS**

| DATA-SHEET PARAMETER | EIA/TIA-422-B | RS-485 |
|---|---|---|
| $V_O$ | $V_{oa}$, $V_{ob}$ | $V_{oa}$, $V_{ob}$ |
| $\|V_{OD1}\|$ | $V_o$ | $V_o$ |
| $\|V_{OD2}\|$ | $V_t$ ($R_L$ = 100 Ω) | $V_t$ ($R_L$ = 54 Ω) |
| $\|V_{OD3}\|$ | | $V_t$ (Test Termination Measurement 2) |
| $V_{test}$ | | $V_{tst}$ |
| $\Delta\|V_{OD}\|$ | $\|\|V_t\|-\|\overline{V}_t\|\|$ | $\|\|V_t\|-\|\overline{V}_t\|\|$ |
| $V_{OC}$ | $\|V_{os}\|$ | $\|V_{os}\|$ |
| $\Delta\|V_{OC}\|$ | $\|V_{os} - \overline{V}_{os}\|$ | $\|V_{os} - \overline{V}_{os}\|$ |
| $I_{OS}$ | $\|I_{sa}\|$, $\|I_{sb}\|$ | |
| $I_O$ | $\|I_{xa}\|$, $\|I_{xb}\|$ | $I_{ia}$, $I_{ib}$ |

## RECEIVER SECTION

### electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $V_O$ = 2.7 V, | $I_O$ = –0.4 mA | | | 0.3 | V |
| $V_{IT-}$ | Negative-going input threshold voltage | $V_O$ = 0.5 V, | $I_O$ = 8 mA | –0.3‡ | | | V |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | | 60 | | mV |
| $V_{IK}$ | Enable-input clamp voltage | $I_I$ = –18 mA | | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 300 mV, See Figure 8 | $I_{OH}$ = –400 μA, | 2.7 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –300 mV, See Figure 8 | $I_{OL}$ = 8 mA, | | | 0.45 | V |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0.4 V to 2.4 V | | | | ±20 | μA |
| $I_I$ | Line input current | Other input = 0 V, See Note 4 | $V_I$ = 12 V | | | 1 | mA |
| | | | $V_I$ = –7 V | | | –0.8 | |
| $I_{IH}$ | High-level enable-input current | $V_{IH}$ = 2.7 V | | | | 60 | μA |
| $I_{IL}$ | Low-level enable-input current | $V_{IL}$ = 0.4 V | | | | –300 | μA |
| $r_i$ | Input resistance | | | 12 | | | kΩ |
| $I_{OS}$ | Short-circuit output current | $V_{ID}$ = 300 mV, | $V_O$ = 0 | –15 | | –85 | mA |
| $I_{CC}$ | Supply current | No load | Outputs enabled | | 69 | 90 | mA |
| | | | Outputs disabled | | 57 | 78 | |

† All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | ALS171 | $V_{ID}$ = –1.5 V to 1.5 V, $C_L$ = 15 pF, $T_A$ = 25°C, See Figure 9 | 9 | | 19 | ns |
| | | ALS171A | | 11 | | 16 | |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | ALS171 | | 9 | | 19 | ns |
| | | ALS171A | | 11 | | 16 | |
| $t_{sk(p)}$ | Pulse skew§ | | $V_{ID}$ = –1.5 V to 1.5 V, $C_L$ = 15 pF, See Figure 9 | | 2 | 5 | ns |
| $t_{sk(lim)}$ | Skew limit¶ | ALS171 | | | | 10 | ns |
| | | ALS171A | | | | 5 | |
| $t_{PZH}$ | Output enable time to high level | | $C_L$ = 15 pF, See Figure 10 | | 7 | 14 | ns |
| $t_{PZL}$ | Output enable time to low level | | | | 7 | 14 | ns |
| $t_{PHZ}$ | Output disable time from high level | | $C_L$ = 15 pF, See Figure 10 | | 20 | 35 | ns |
| $t_{PLZ}$ | Output disable time from low level | | | | 8 | 17 | ns |

† All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one $V_{CC}$ and operating temperature within the recommended operating conditions.

## PARAMETER MEASUREMENT INFORMATION

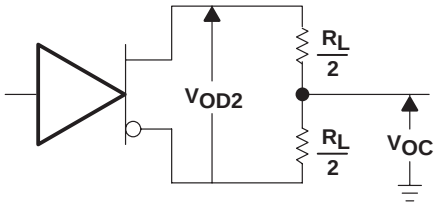



**Figure 1. Driver $V_{OD}$ and $V_{OC}$**

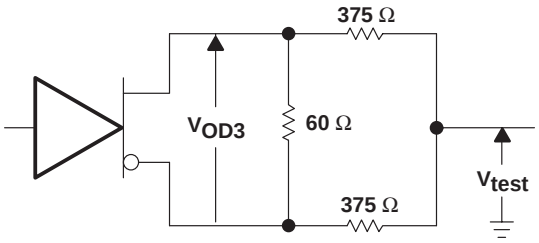
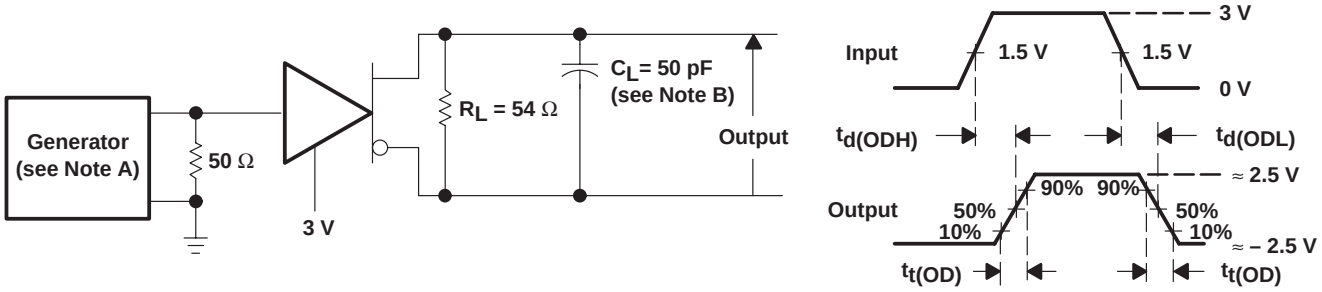



**Figure 2. Driver $V_{OD3}$**

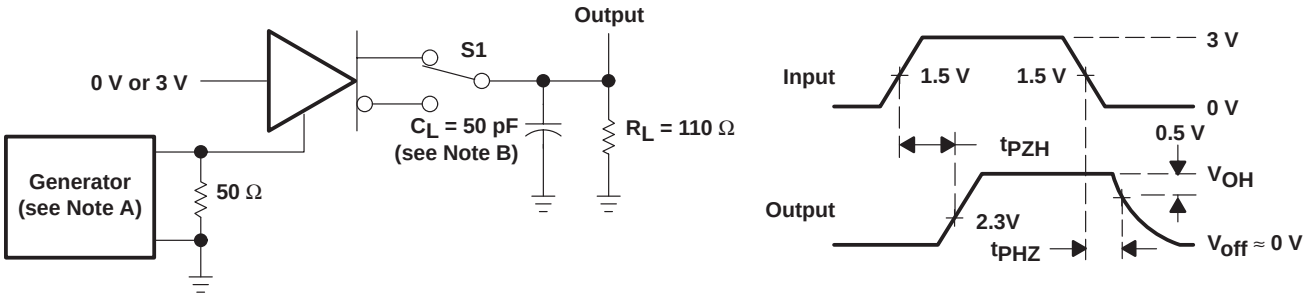



**TEST CIRCUIT** **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

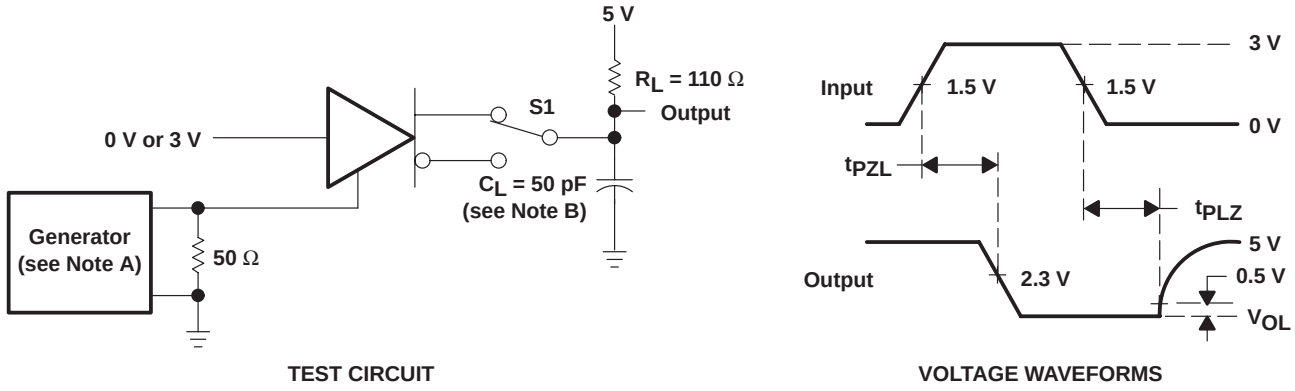
**Figure 3. Driver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

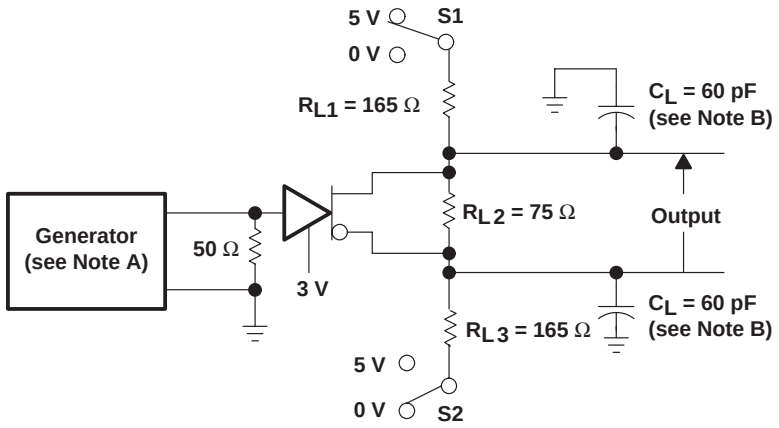
**Figure 4. Driver Test Circuit and Voltage Waveforms**



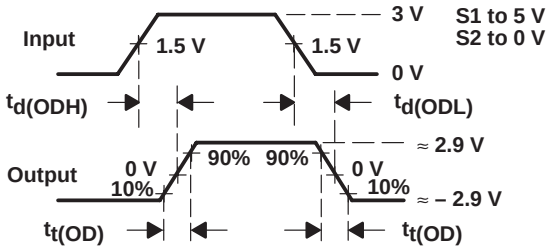

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 5. Driver Test Circuit and Voltage Waveforms**

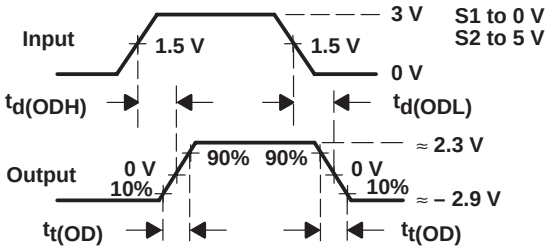
## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

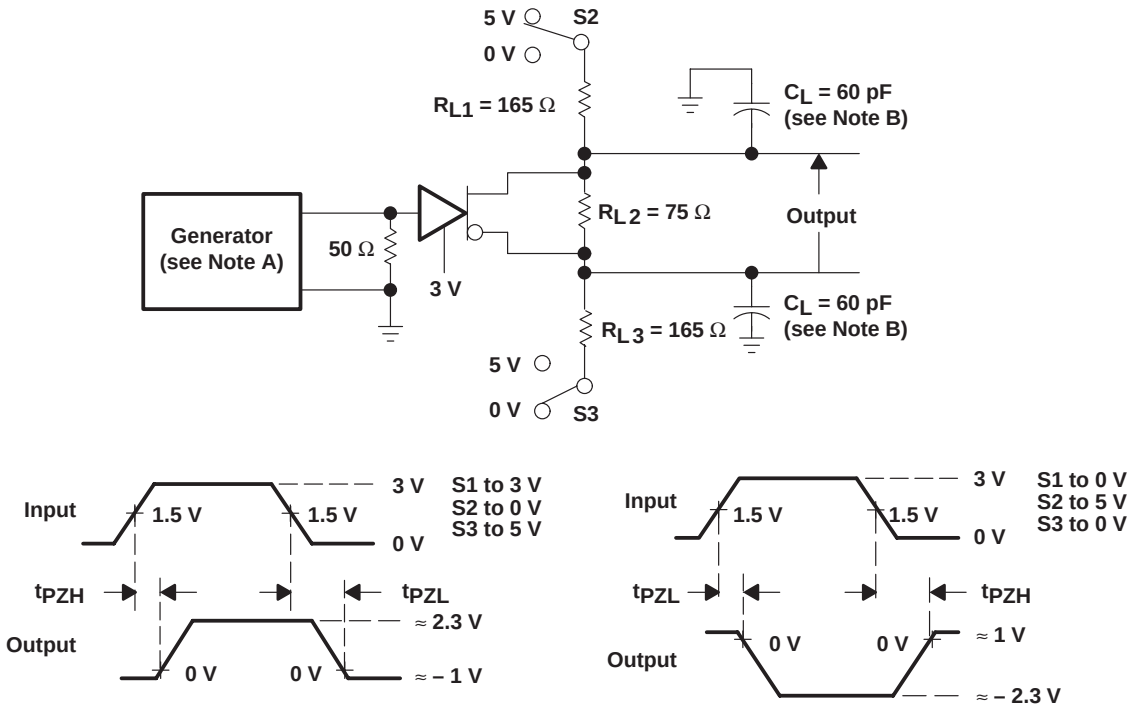



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 6. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 7. Driver Differential-Enable and Disable Times With a Double-SCSI Termination**

## PARAMETER MEASUREMENT INFORMATION

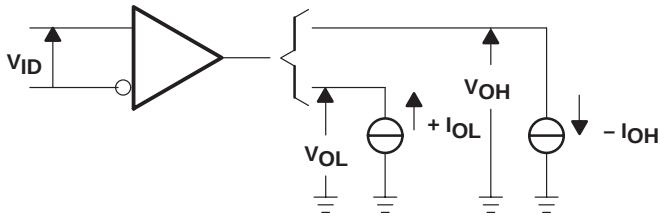
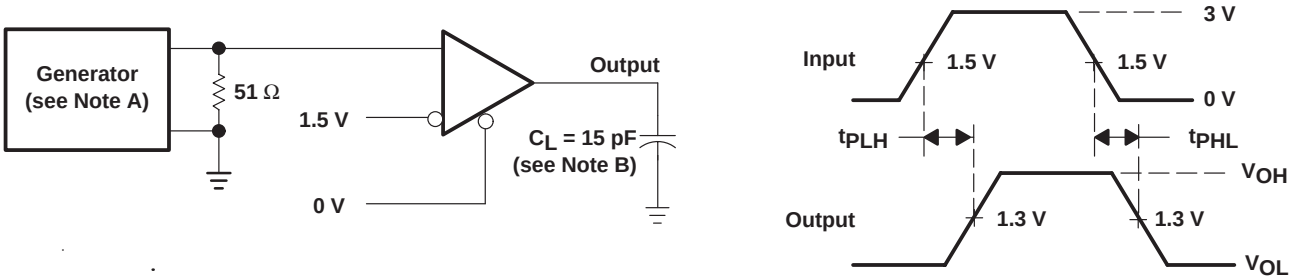



**Figure 8. Receiver $V_{OH}$ and $V_{OL}$**

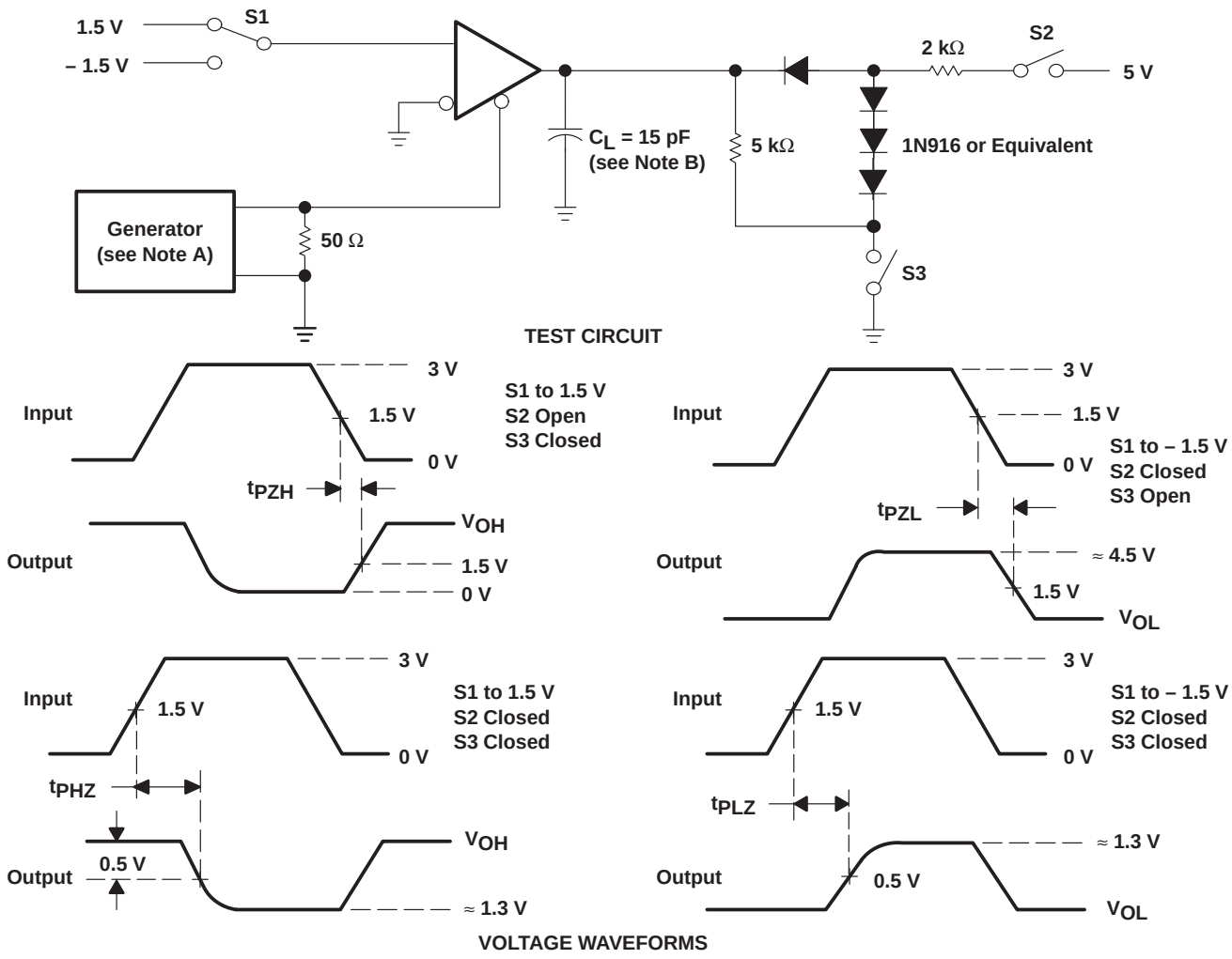



**TEST CIRCUIT** **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 9. Receiver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 10. Receiver Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

**DRIVER**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

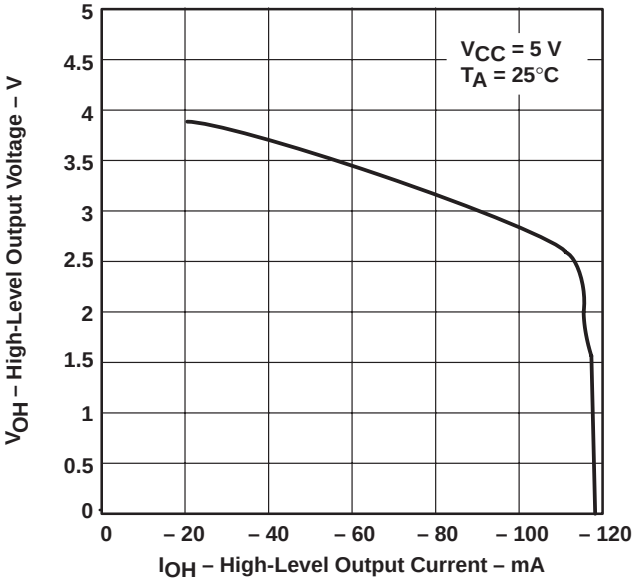



Figure 11

**DRIVER**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

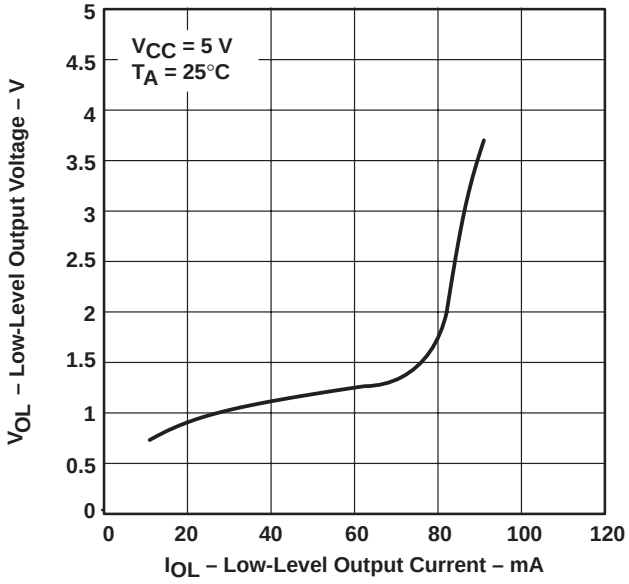



Figure 12

**DRIVER**
**DIFFERENTIAL OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

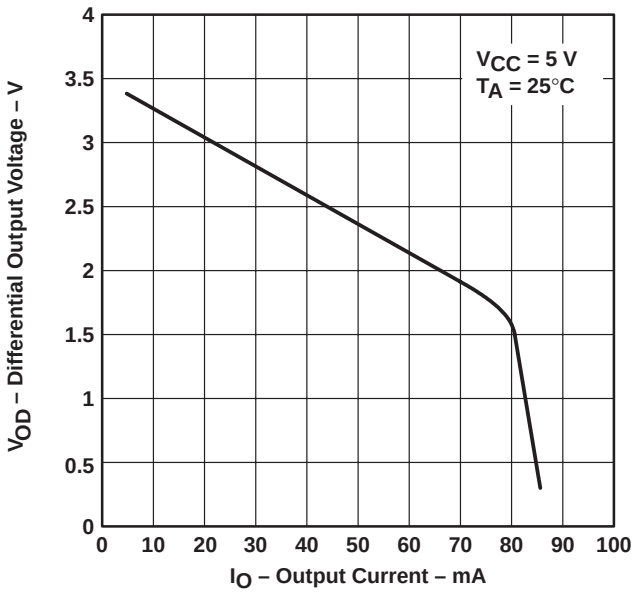



Figure 13

## TYPICAL CHARACTERISTICS

**RECEIVER**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

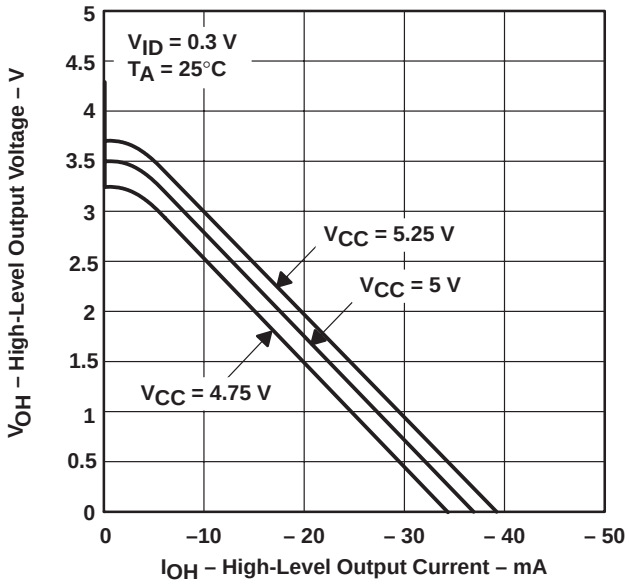



**Figure 14**

**RECEIVER**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**

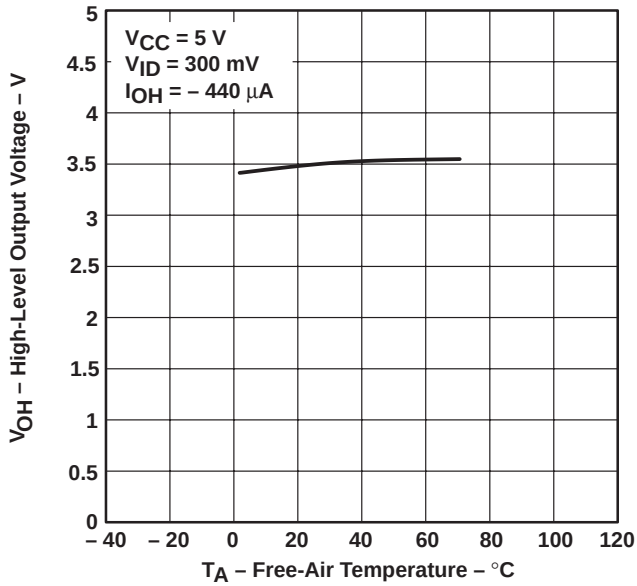



**Figure 15**

**RECEIVER**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

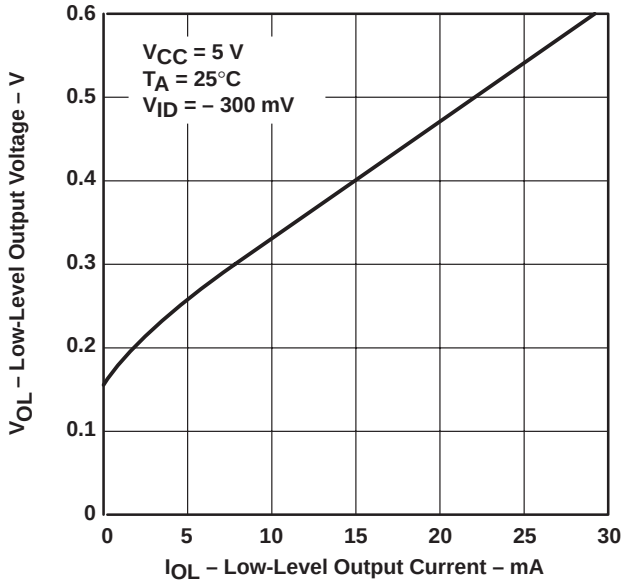



**Figure 16**

**RECEIVER**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**

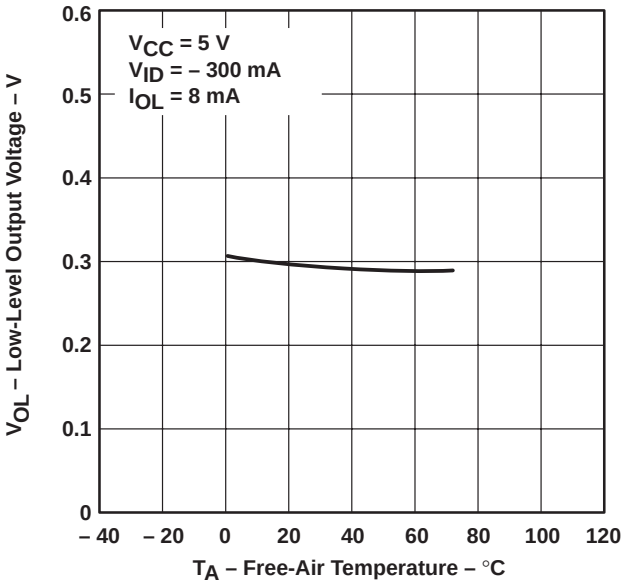



**Figure 17**

## TYPICAL CHARACTERISTICS

**RECEIVER OUTPUT VOLTAGE vs ENABLE VOLTAGE**

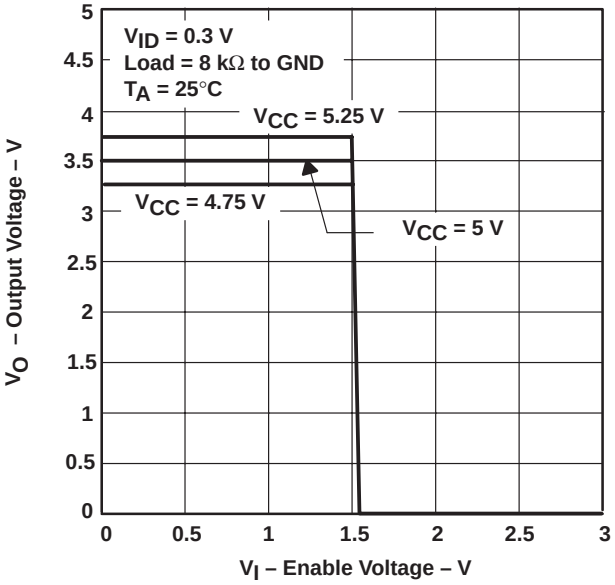



Figure 18

**RECEIVER OUTPUT VOLTAGE vs ENABLE VOLTAGE**

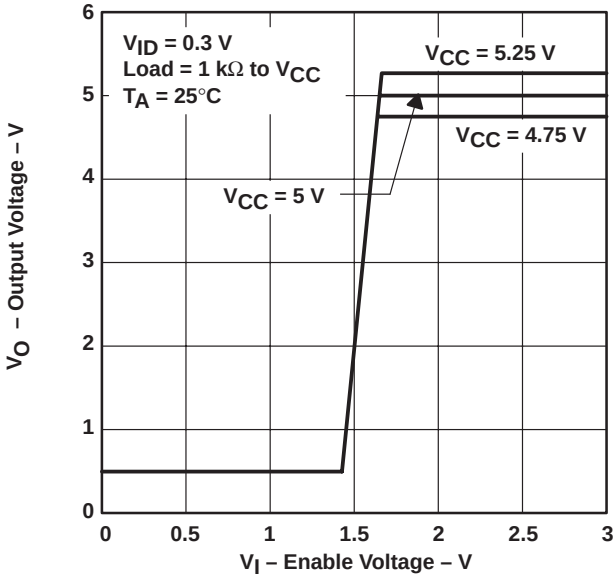
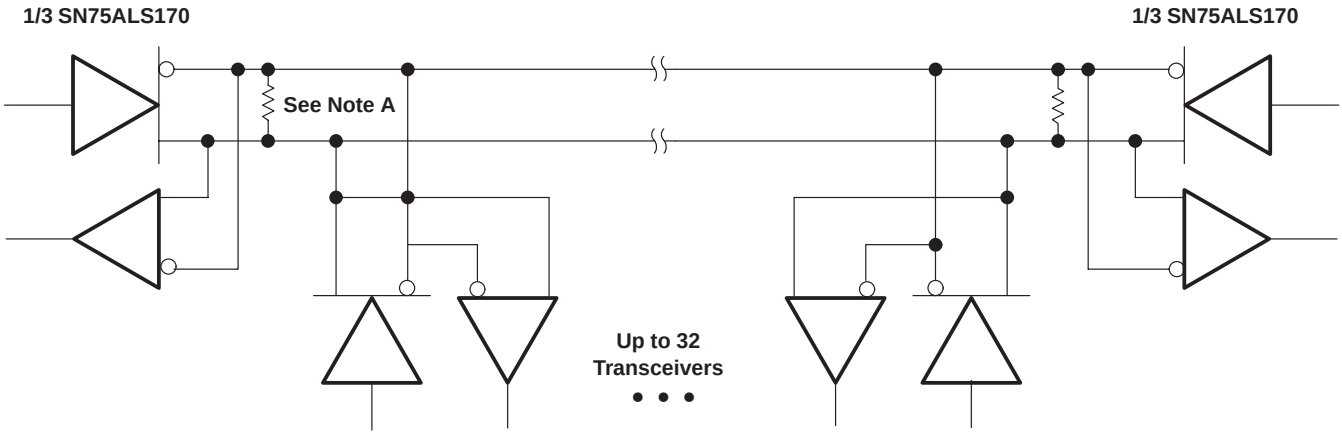



Figure 19

## APPLICATION INFORMATION




NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

**Figure 20. Typical Application Circuit**

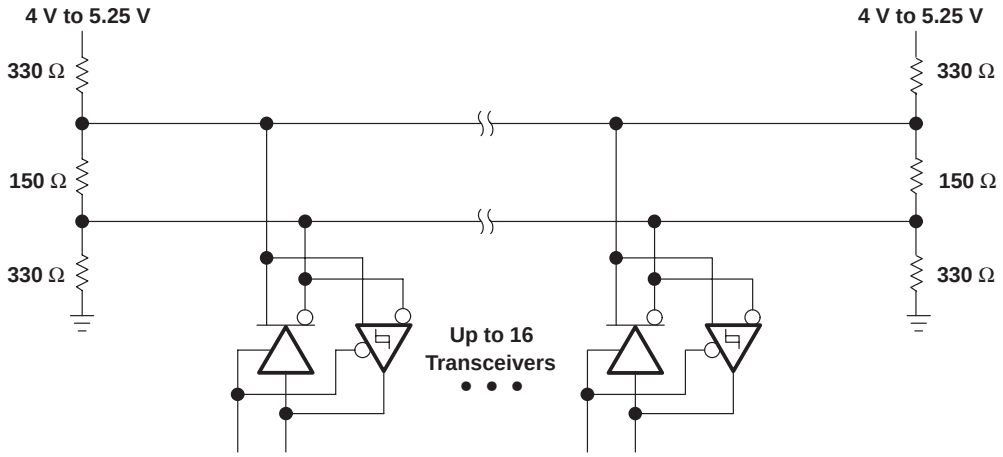



**Figure 21. Typical Differential SCSI Application CIrcuit**

## APPLICATION INFORMATION

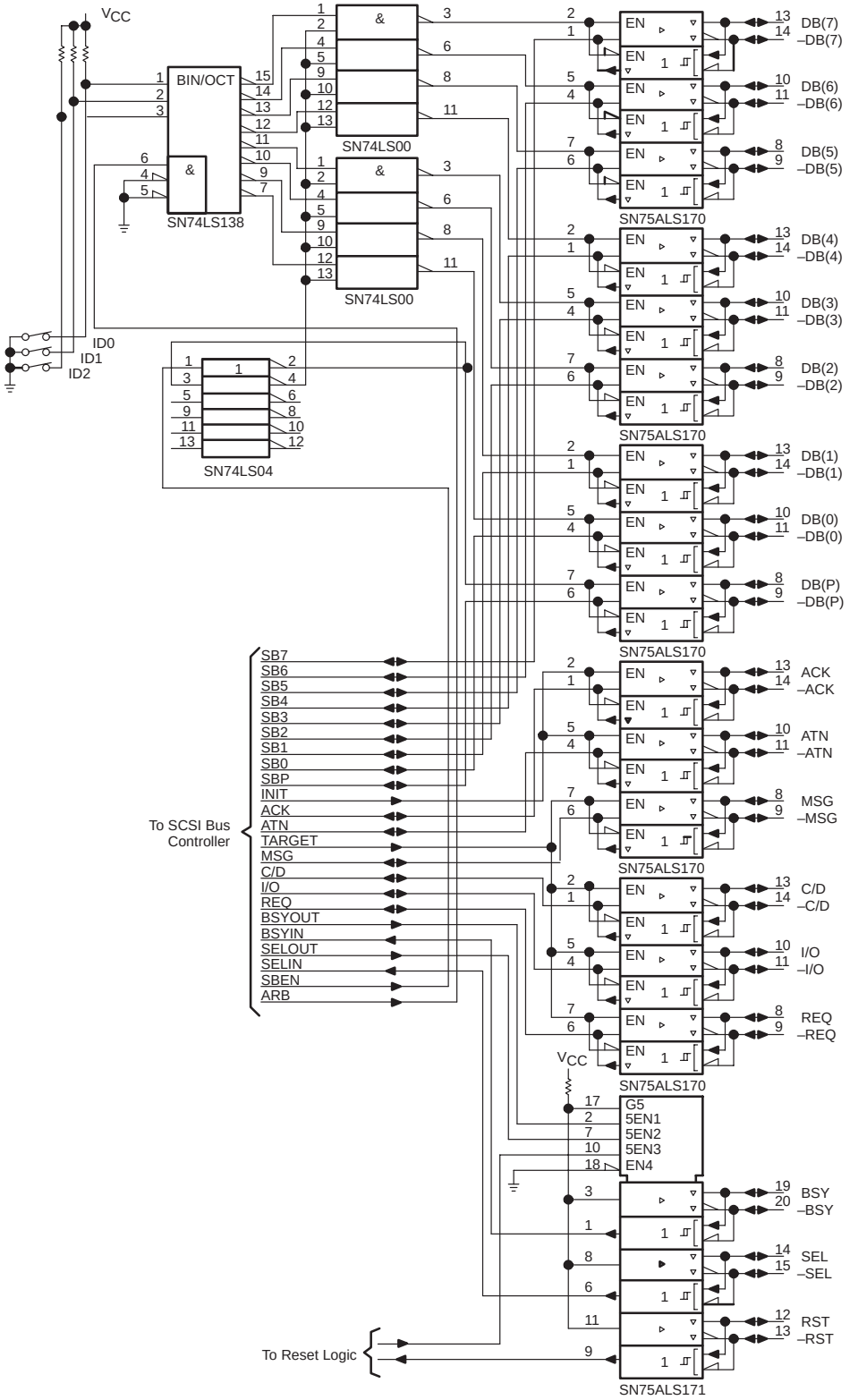



**Figure 22. Typical Differential SCSI Bus Interface Implementation**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN75ALS171ADW | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS171A |
| SN75ALS171ADW.A | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS171A |
| SN75ALS171DW | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS171 |
| SN75ALS171DW.A | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS171 |
| SN75ALS171DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS171 |
| SN75ALS171DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS171 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

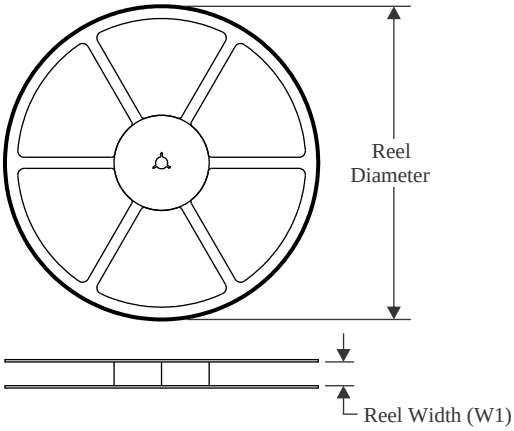
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

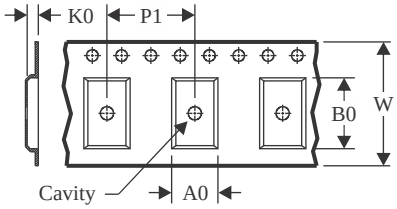
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

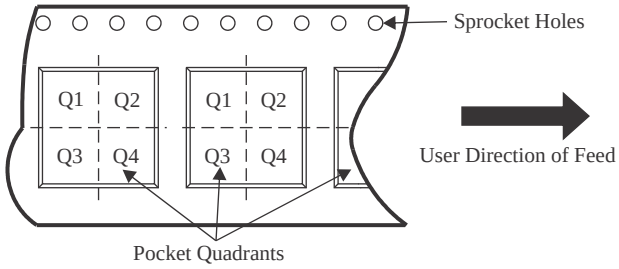



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

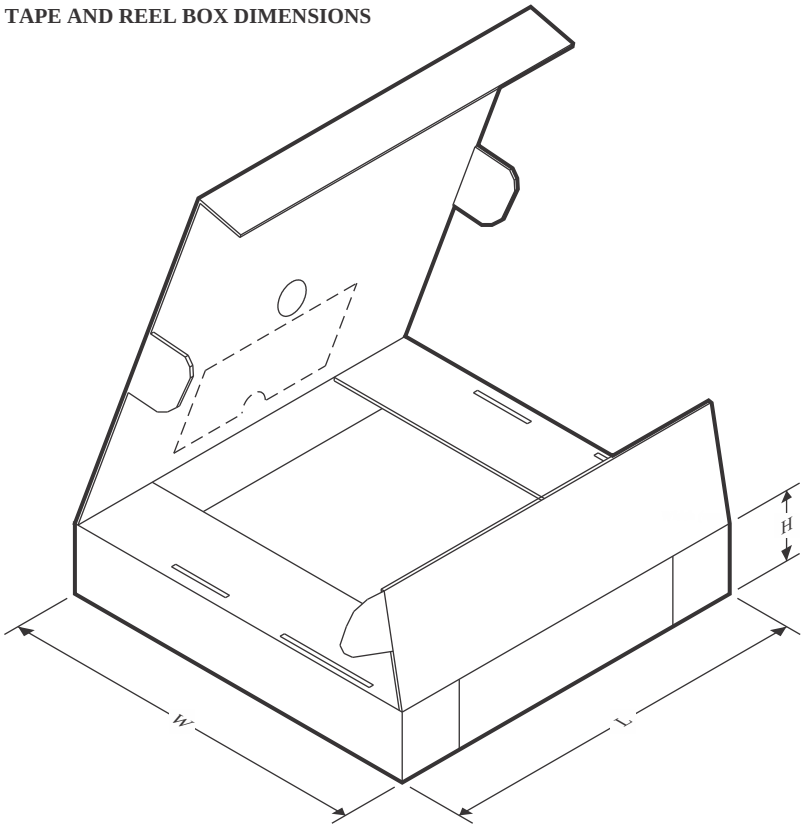
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75ALS171DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

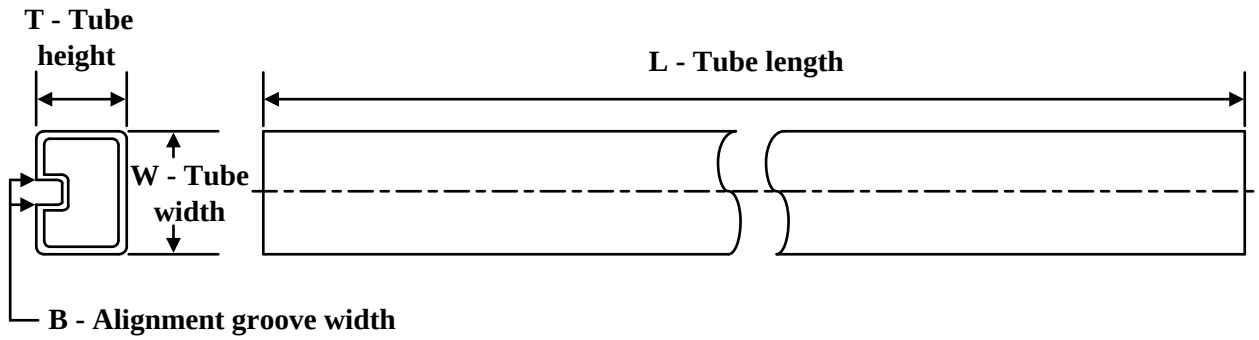
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

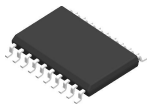
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75ALS171DWR | SOIC | DW | 20 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN75ALS171ADW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75ALS171ADW.A | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75ALS171DW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75ALS171DW.A | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |

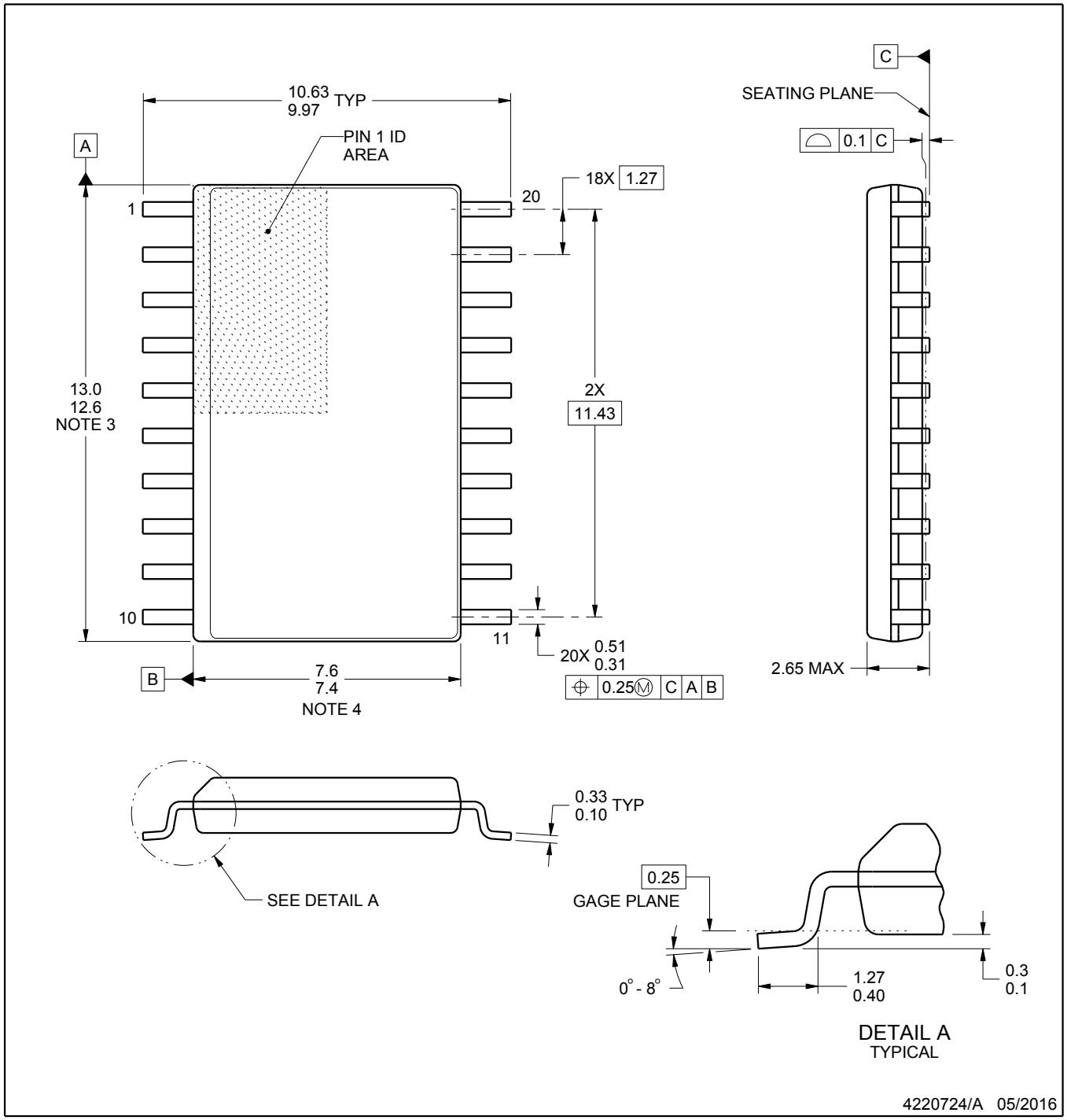


# PACKAGE OUTLINE

## DW0020A

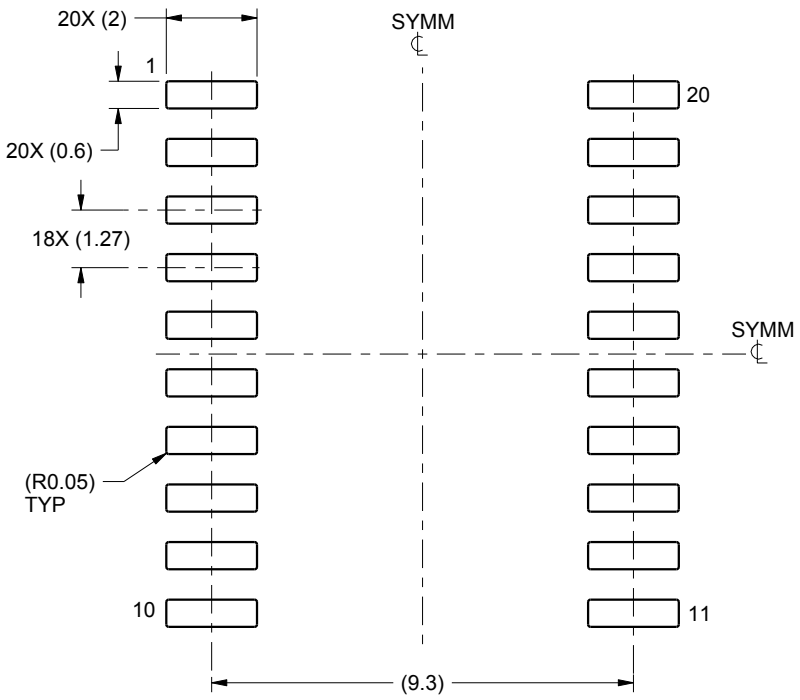
## SOIC - 2.65 mm max height

SOIC

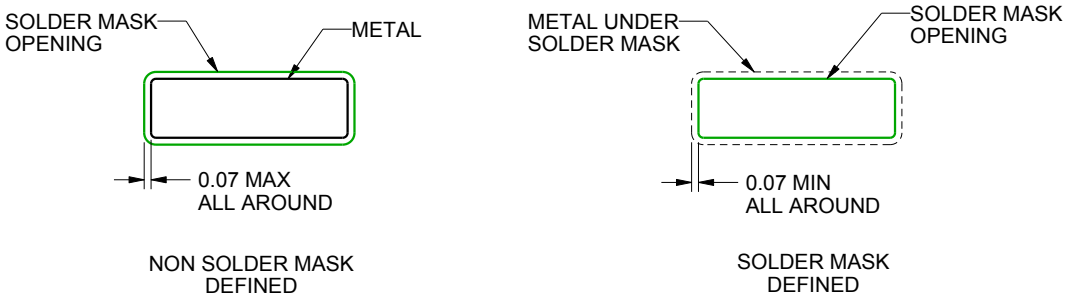



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

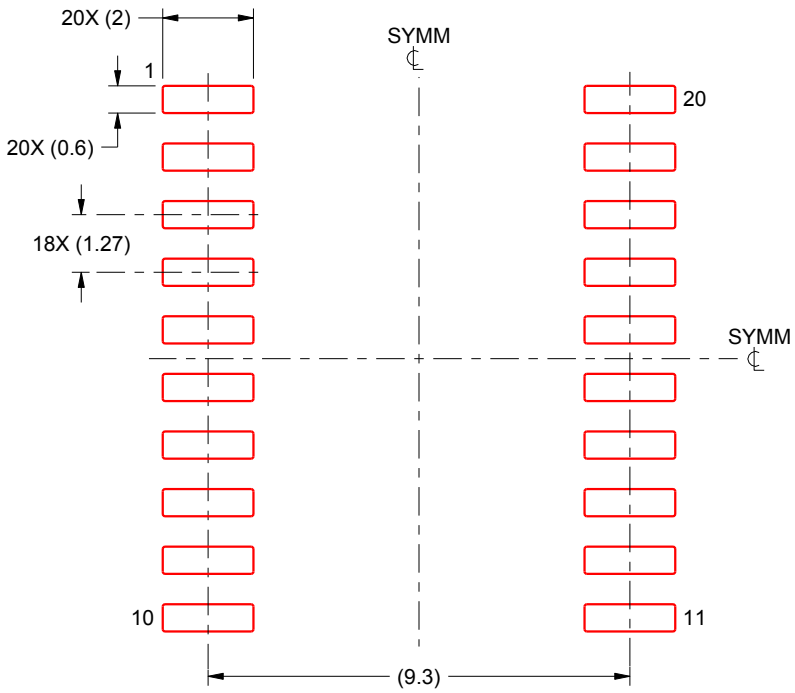



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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