National Semiconductor

May 2000

CLC5801
High Speed Low Noise Voltage Feedback Amplifier

General Description

The CLC5801 is a low-cost, wideband voltage feedback amplifier excellent for low noise applications. It combines a wide bandwidth of 420MHz with very low noise ($2nV/\sqrt{Hz}$, $1.8pA/\sqrt{Hz}$) and low DC errors (100µV V_{OS}) making it an excellent precision high speed op amp offering closed-loop gains of ≥ 10.

The CLC5801 employs a traditional voltage-feedback topology and provides all the benefits of balanced inputs, such as low offsets and drifts, as well as 96dB open-loop gain, 95dB CMRR and a 90dB PSRR. Providing a wide 420MHz bandwidth at a gain of A_V = 10, a fast 300V/µs slew rate, the CLC5801 is well suited for wide band active filters and low noise loop filters for PLLs.

The low noise, wide gain-bandwidth, high slew rate and low DC errors enable applications such as medical diagnostic ultrasound, magnetic tape and disk storage, communications and optoelectronics that require maximum high-frequency signal-to-noise ratios. Low noise and offset make the CLC5801 and ideal preamplifier for CD-ROMs and receivers.

The CLC5801 consumes 16mA of supply current and can be used in either dual 5V systems or single supply applications. It can easily drive a 100Ω load to within 1.6V of either rail.

The CLC5801 is available in both SOIC-8 and the tiny SOT23-5.

Features

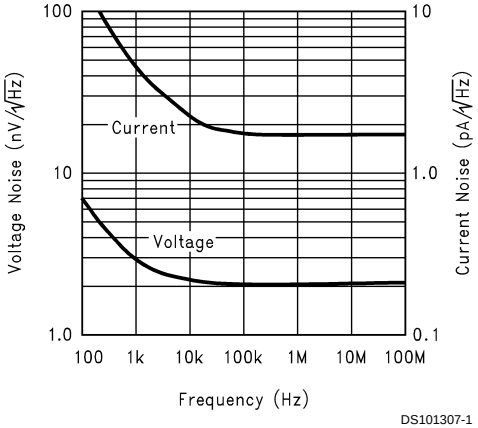
(T_A = 25°C, V_S = ±5V, R_L = 100Ω Typical unless specified).

- 420MHz, −3dB bandwidth (A_V = 10)
- $2nV/\sqrt{Hz}$ input voltage noise
- $1.8pA/\sqrt{Hz}$ input current noise
- 100µV input offset voltage
- 300V/µs slew rate
- 16mA supply current
- 18ns settling time

Applications

- Ultrasound preamplifier
- CD-ROM preamplifer
- Photo-diode transimpedance amplifier
- Low-noise loop filters for PLLs
- High-performance receivers
- ADC preamplifier

Equivalent Input Noise



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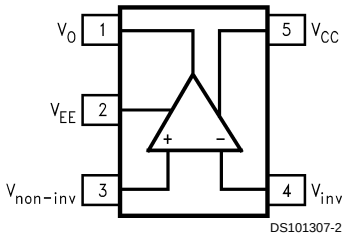
Connection Diagrams

5-Pin SOT23-5



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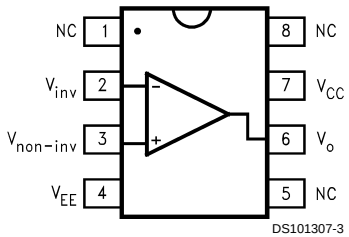
Top View

8-Pin SOIC



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Top View

Ordering Information

Package	Part Number	Packaging Marking	Transport Media	NSC Drawing
8-pin SOIC	CLC5801IM	CLC5801IM	Rails	M08A
	CLC5801IMX	CLC5801IM	2.5k Tape and Reel	
5-pin SOT23-5	CLC5801IM5	A50A	1k Units Tape and Reel	MF05A
	CLC5801IM5X	A50A	3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	±7V
I_{OUT} Short Circuit protected to ground. Maximum reliability is obtained if I_{OUT} does not exceed:	125mA
Common-Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+125˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C
ESD (human body model)	1000V

Operating Rating (Note 1)

Thermal Resistance (θ_{JC})	
SOIC	65˚C/W
SOT23-5	115˚C/W
Thermal Resistance (θ_{JA})	
SOIC	145˚C/W
SOT23-5	185˚C/W
Temperature Range	−40˚C to +85˚C
Recommended Gain Range	±10 to ±1000V/V

Electrical Characteristics

(T_A= 25˚C, V_{CC} = ±5V, R_g = 26.1Ω, R_f= 499Ω, R_L= 100Ω; unless specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
			+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
GBW	Gain Bandwidth Product	$V_O < 0.4V_{PP}$	1.8		1.3		GHz
SSBW	−3dB Bandwidth (A_V = +10)	$V_O < 0.4V_{PP}$	420				MHz
	−3dB Bandwidth (A_V = +20)	$V_O < 0.4V_{PP}$	90		70		
LSBW	−3dB Bandwidth	$V_O < 5.0V_{PP}$	35		30		
GFP	Gain Flatness Peaking	DC to 30MHz, $V_O < 0.4V_{PP}$	0.4		0.5		dB
GFR	Gain Flatness Rolloff	DC to 30MHz, $V_O < 0.4V_{PP}$	0.2		0.5		dB
LPD	Linear Phase Deviation	DC to 30MHz, $V_O < 0.4V_{PP}$	0.8		1.5		Deg
Time Domain Response							
TRS	Rise and Fall Time	0.4V step	4.0		4.7		ns
TSS	Settling Time to 0.2%	2V step	18		30		ns
OS	Overshoot	0.4V step	5		10		%
SR	Slew Rate	2V step	300		250		V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	$1V_{PP}$,10MHz	−53		−48		dBc
HD3	3rd Harmonic Distortion	$1V_{PP}$,10MHz	−78		−65		dBc
IMD	3rd Order Intermod. Intercept	10MHz	34				dBm
VN	Equivalent Input Noise Voltage	1MHz to 100MHz	2.0		2.7		nV/$\sqrt{Hz}$
ICN	Equivalent Input Noise Current	1MHz to 100MHz	1.8		2.5		pA/$\sqrt{Hz}$
Static, DC Performance							
AOL	Open-Loop Gain	DC	96	77	86	86	dB
VIO	Input Offset Voltage (Note 3)		±100	±1000	±800	±1000	µV
DVIO	Offset Voltage Average Drift		±2	8	–	4	µV/˚C
IB	Input Bias Current (Note 3)		12	40	20	20	µA
DIB	Bias Current Average Drift		−100	−250	–	−120	µA/˚C
IIO	Input Offset Current		±0.2	3.4	2.0	2.0	µA
DIIO	Offset Current Average Drift		±3	±50	–	±25	nA/˚C
PSRR	Power Supply Rejection Ratio	DC	90	80	85	84	dB
CMRR	Common Mode Rejection Ratio	DC	95	84	88	86	dB
ICC	Supply Current (Note 3)	R_L = ∞	16	18	17	17	mA

Electrical Characteristics (Continued)

(T_A= 25˚C, V_{CC} = ±5V, R_g = 26.1Ω, R_f= 499Ω, R_L= 100Ω; unless specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
			+25˚C	−40˚C	+25˚C	+85˚C	
Miscellaneous Performance							
RINC	Input Resistance	Common-Mode	2	0.6	1.6	1.6	MΩ
RIND		Differential-Mode	6	1	3	3	kΩ
CINC	Input Capacitance	Common-Mode	1.5	3	3	3	pF
CIND		Differential-Mode	1.9	3	3	3	pF
ROUT	Output Resistance	Closed Loop	5	50	10	10	mΩ
VO	Output Voltage Range	R_L = ∞	±3.8	±3.5	±3.7	±3.7	V
VOL		R_L = 100Ω	±3.4	±2.8	±3.2	±3.2	V
CMIR	Input Voltage Range	Common-Mode	±3.8	±3.4	±3.5	±3.5	V
IOP	Output Current	Source	80	60	65	65	mA
ION		Sink	80	40	55	55	

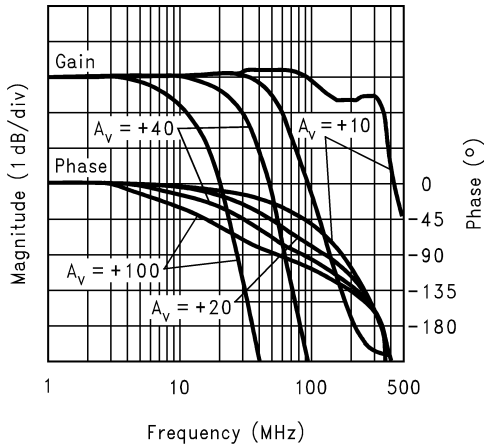
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed,

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: 100% tested at +25˚C.

Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).

Non-Inverting Frequency Response



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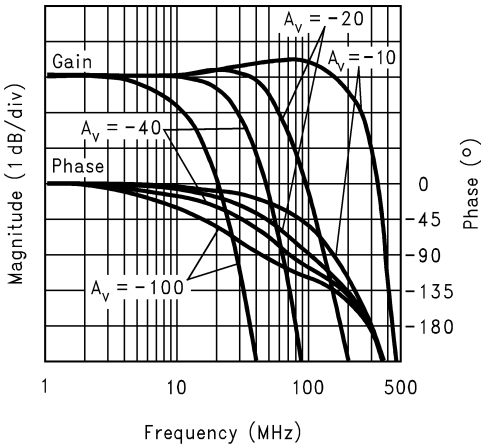
Inverting Frequency Response



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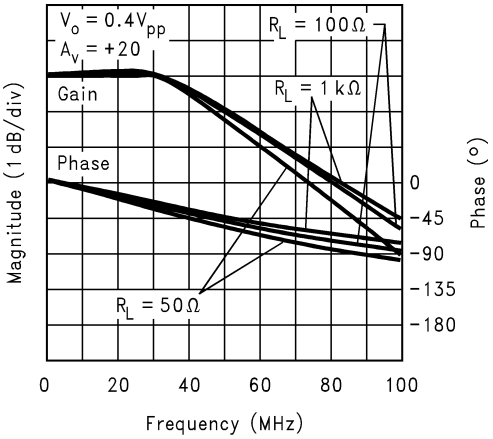
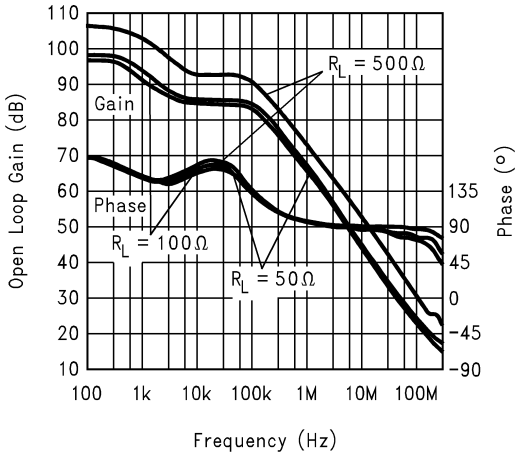
Frequency Response for Various R_Ls



DS101307-6

Open Loop Gain and Phase vs. R_L



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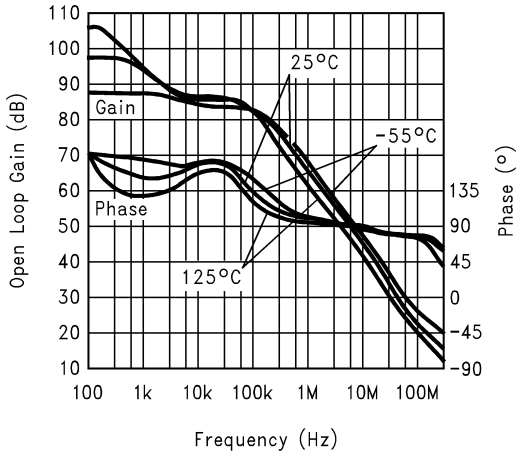
Open Loop Gain and Phase vs. Temp



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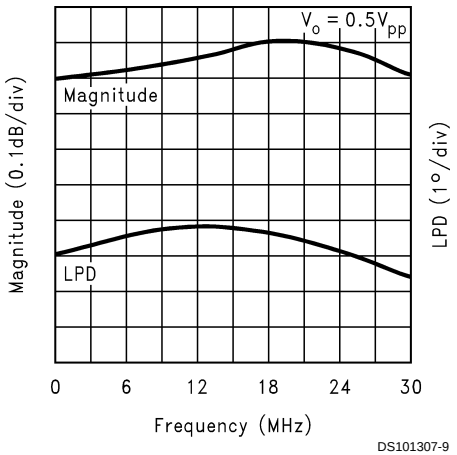
Gain Flatness & Linear Phase Deviation



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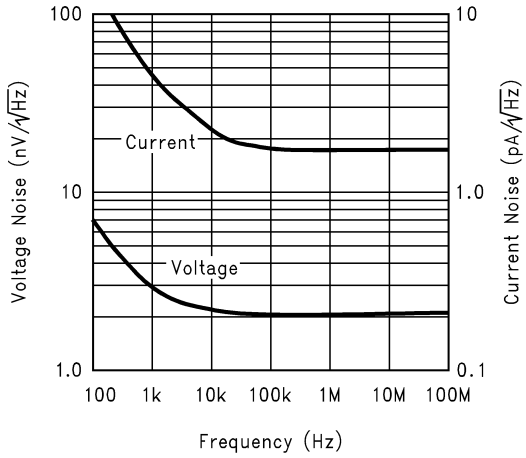
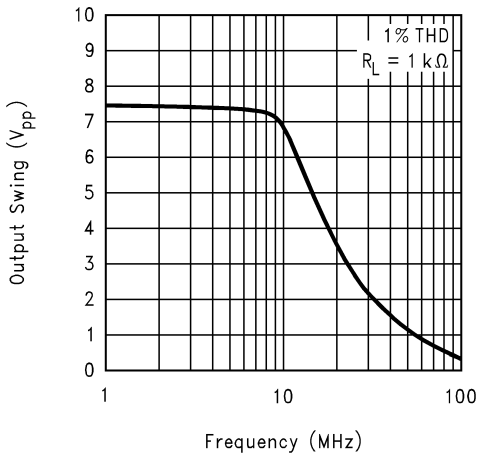
Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).. (Continued)

Equivalent Input Noise



DS101307-1

Maximum Output Swing vs. Frequency



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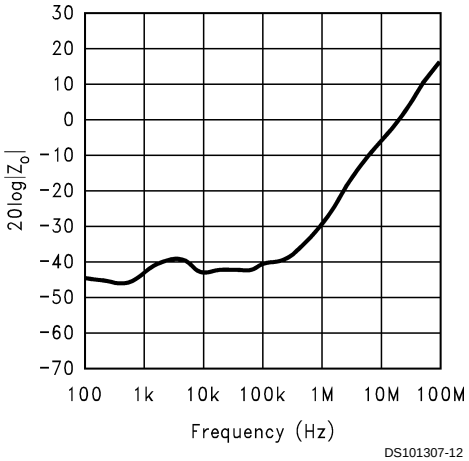
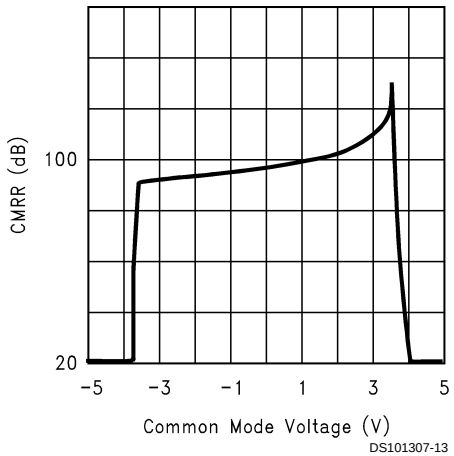
Closed-Loop Output Impedance



DS101307-12

CMRR vs. Common Mode Input Voltage



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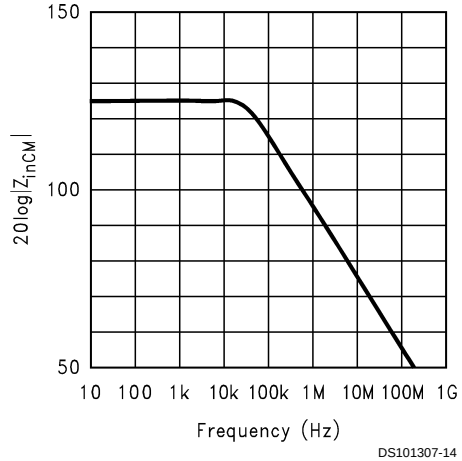
Common Mode Input Impedance



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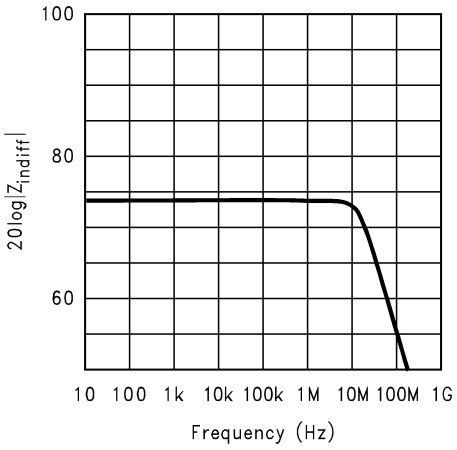
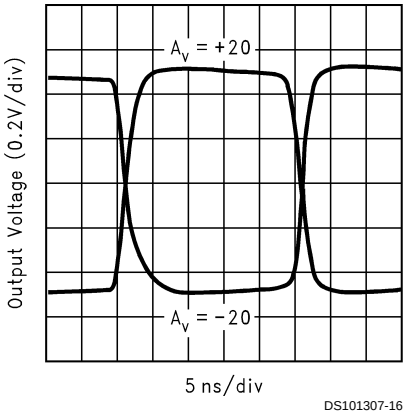
Differential Input Impedance



DS101307-15

Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).. (Continued)

Pulse Response (V_O = 1V_{PP})



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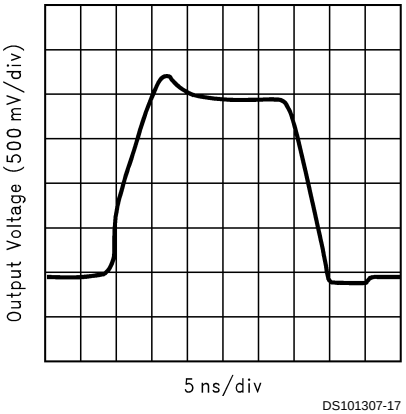
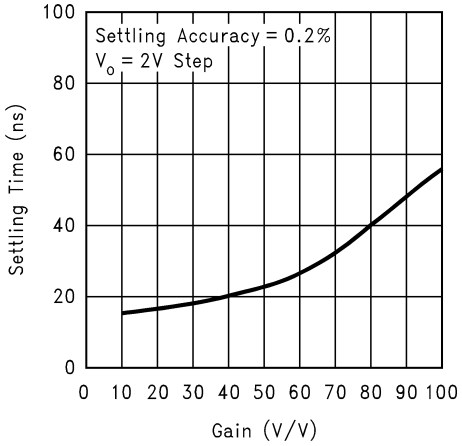
Large Signal Pulse Response (V_O = 2V_{PP})



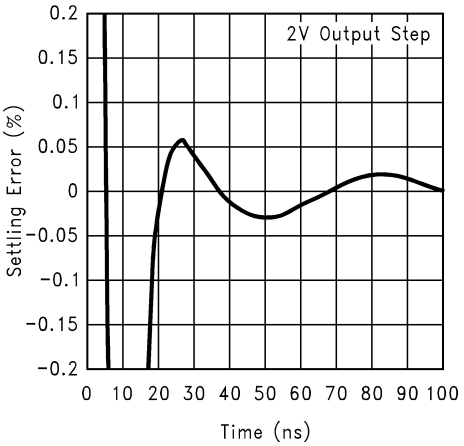
DS101307-17

Settling Time vs. Gain



DS101307-18

Short Term Settling Time



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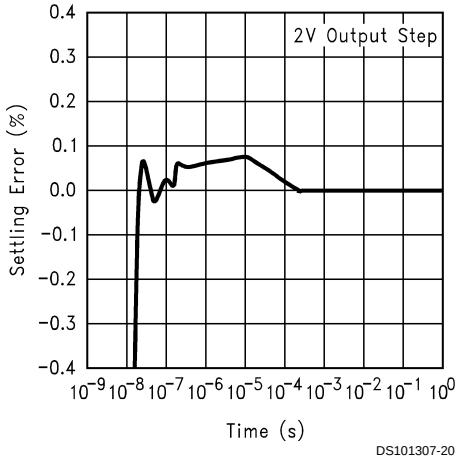
Long Term Settling Time



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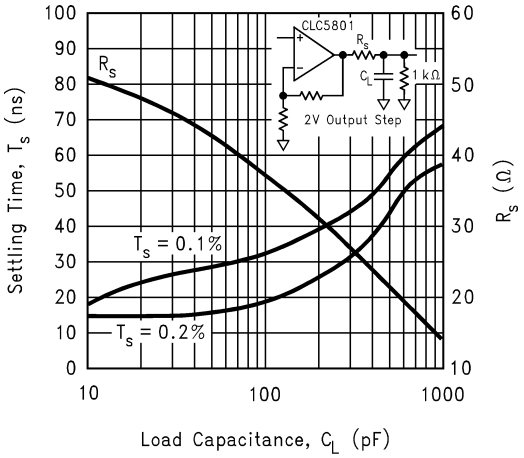
Settling Time vs. C_L and R_S



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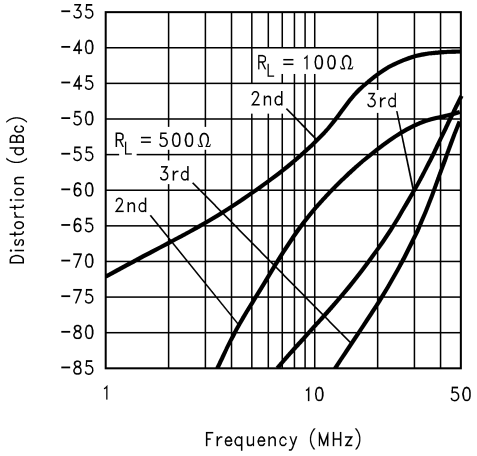
Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).. (Continued)

2nd & 3rd Harmonic Distortion (V_O = 1V_{PP})



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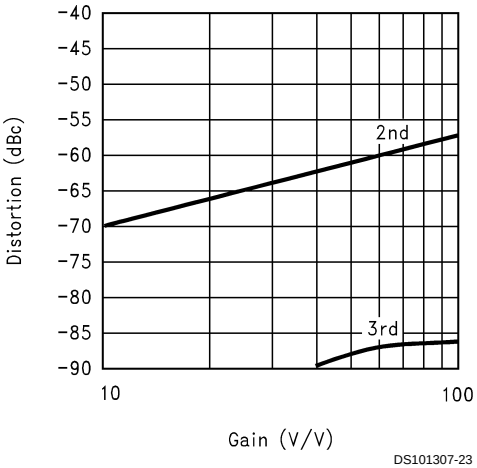
Distortion vs. Gain (V_O = 1V_{PP}, f_o = 3MHz)



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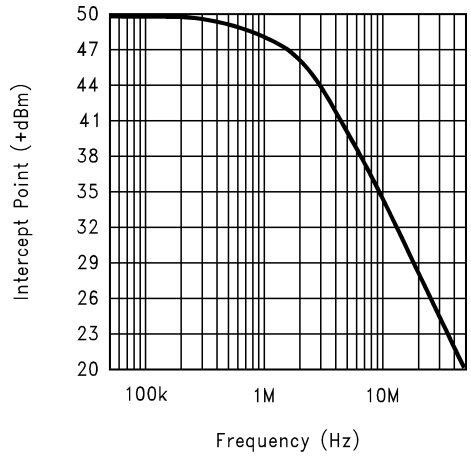
2-Tone, 3rd Order Intermod. Intercept.



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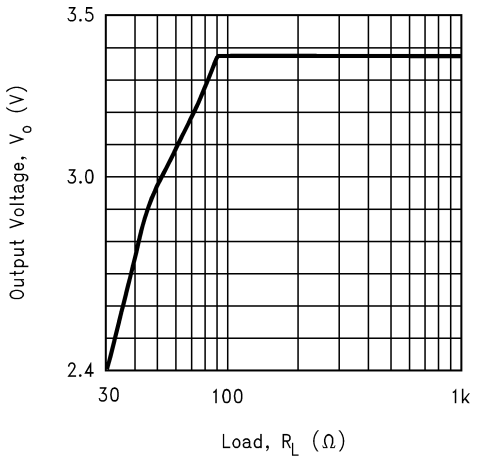
Output Voltage vs. Load



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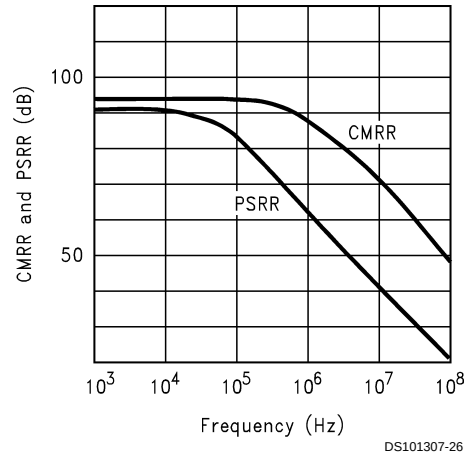
CMRR and PSRR



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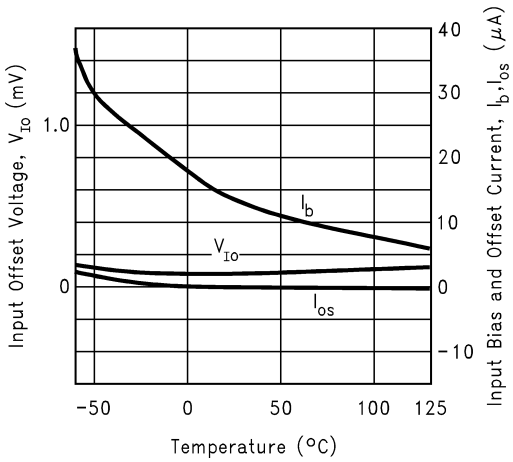
Typical DC Errors vs. Temperature



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Application Information

Introduction

The CLC5801 is a very wide gain-bandwidth, low noise voltage feedback operational amplifier which enables applications areas such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high-frequency signal-to-noise ratios. The following discussion will describe the proper selection of external components in order to achieve optimum device performance.

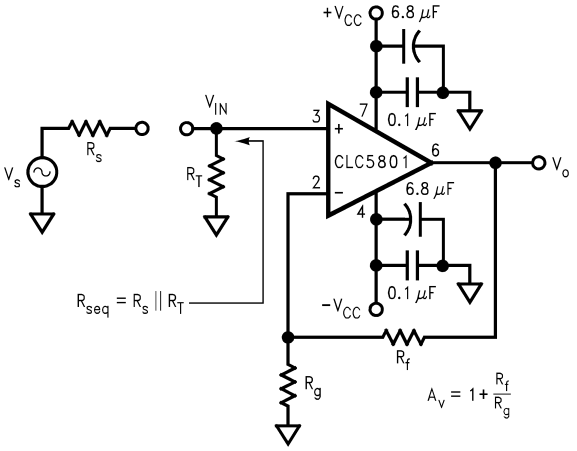


FIGURE 1. Non-Inverting Amplifier Configuration

Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain-setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in *Figure 1*. Combining this constraint with the non-inverting gain equation also seen in *Figure 1*, allows both R_f and R_g to be determined explicitly from the following equations: $R_f = A_V R_{seq}$ and $R_g = R_f/(A_V - 1)$. When driven from a 0Ω source, such as that from the output of an op amp, the non-inverting input of the CLC5801 should be isolated with at least a 25Ω series resistor.

As seen in *Figure 2*, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f \parallel (R_g + R_s)$). R_b is recommended to be no less than 25Ω for best CLC5801 performance. The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

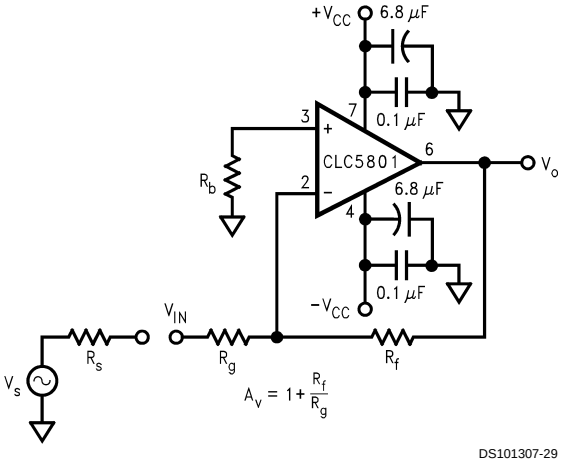


FIGURE 2. Inverting Amplifier Configuration

Total Input Noise vs. Source Resistance

In order to determine maximum signal-to-noise ratios from the CLC5801, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 3 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) sources, there also exists thermal voltage noise ($e_t = \sqrt{4kTR}$) associated with each of the external resistors. *Equation (1)* provides the general form for total equivalent input voltage noise density (e_{ni}). *Equation (2)* is a simplification of *Equation (1)* that assumes $R_f \parallel R_g = R_{seq}$ for bias current cancellation. *Figure 4* illustrates the equivalent noise model using this assumption. *Figure 5* is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing noise sources of *Equation (2)* shown. This plot gives the expected e_{ni} for a given R_{seq} which assumes $R_f \parallel R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni} \times A_V$.

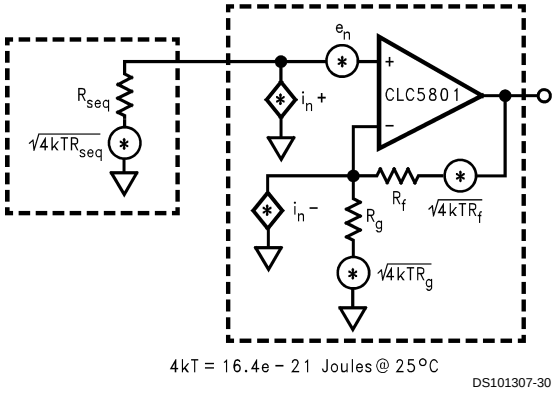


FIGURE 3. Non-Inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + (i_n R_{seq})^2 + 4kTR_{seq} + (i_n (R_f \parallel R_g))^2 + 4kT(R_f \parallel R_g)} \quad (1)$$

Application Information (Continued)

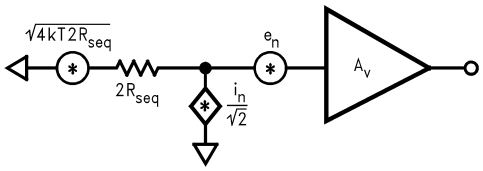


FIGURE 4. Noise Model with R_f || R_g = R_{seq}

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{seq})^2 + 4kT(2R_{seq})} \quad (2)$$

As seen in *Figure 5*, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistance below 121Ω. Between 121Ω and 5.11kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{4kT(2R_{seq})}$) of the external resistors. Above 5.11kΩ, e_{ni} is dominated by the amplifier's current noise ($e_n/\sqrt{2}\, i_n R_{seq}$). The point at which the CLC5801's voltage noise and current noise contribute equally occurs for R_{seq} = 786Ω ($e_n/\sqrt{2}\, i_n$). As an example, configured with a gain of +20V/V giving a −3dB of 90MHz and driven from an R_{seq} = 25Ω, the CLC5801 produces a total equivalent input noise voltage ($e_{ni} * \sqrt{1.57 * 90\,MHz}$) of 26μ$V_{rms}$.

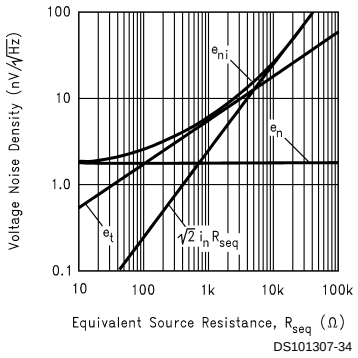


FIGURE 5. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then R_f || R_g does not need to equal R_{seq}. In this case, according to *Equation (1)*, R_f || R_g should be as low as possible in order to minimize noise. Results similar to *Equation (1)* are obtained for the inverting configuration of *Figure 2* if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, *Equation (1)* will yield e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Inverting Gains Less Than 10V/V

The lag compensation of *Figure 6* will achieve stability for lower gains. Placing the network between the two input terminals does not affect the closed-loop nor noise gain, but is best used for the inverting configuration because of its affect on the non-inverting input impedance.

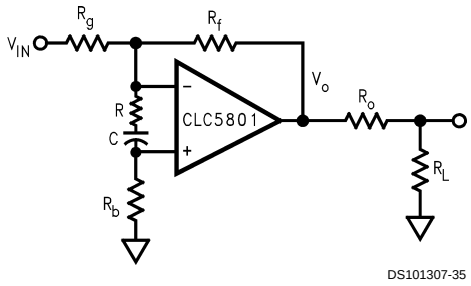


FIGURE 6. External Lag Compensation

Single-Supply Operation

The CLC5801 can be operated with single power supply as shown in *Figure 7*. Both the input and output are capacitively coupled to set the DC operating point.

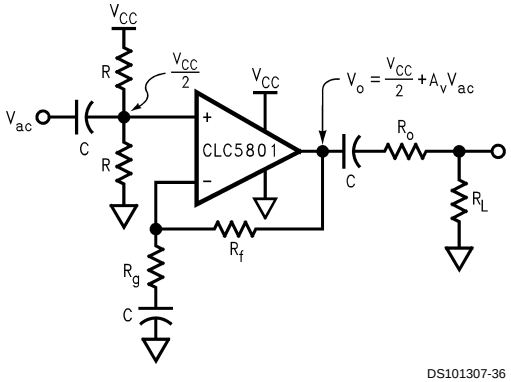


FIGURE 7. Single Supply Operation

Low Noise Transimpedance Amplifier

Figure 8 shows a transimpedance amplifier used to amplify the small signal from a Photodiode. Using a low noise amplifier such as the CLC5801 and proper design, ensures that the amplifier noise contribution is minimal. Here R_b can be used to compensate for the input bias current of the CLC5801. Generally, R_b is selected to be equal to R_f to cancel the effect of I_b flowing in each of the Op Amp input terminals.

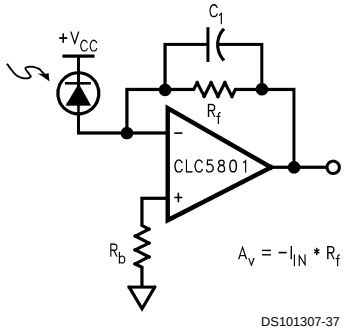


FIGURE 8. Transimpedance Amplifier Configuration

Figure 9 shows the equivalent noise analysis schematic for this circuit. The complete expression for the amplifier stage output rms noise is shown in *Equation (3)*.

$$e_{no(rms)} = \sqrt{(i_n R_b)^2 + (i_n R_f)^2 + e_n^2 + 4kTR_f + 4kTR_b} \quad (3)$$

Application Information (Continued)

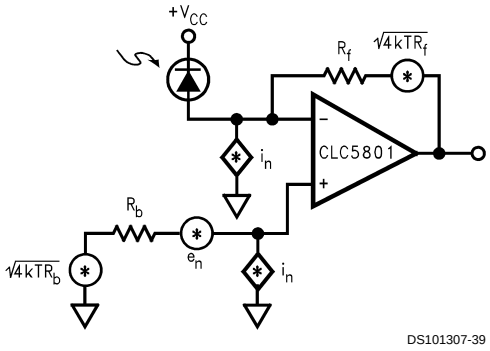


FIGURE 9. Transimpedance Amplifier Noise Model

Low Noise Integrator

The Circuit in *Figure 10* implements a deBoo integrator. Integration linearity is maintained through positive feedback. The CLC5801's low input offset voltage and matched inputs allowing bias current cancellation provide for very precise integration. Stability is maintained through the constraint on the circuit elements.

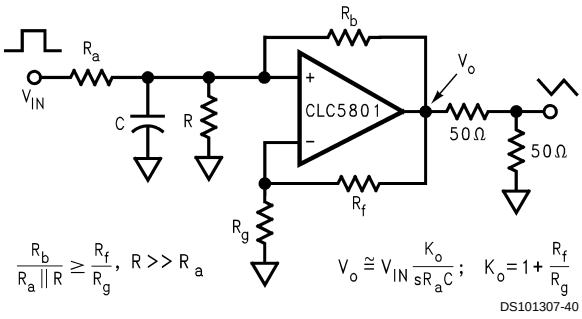


FIGURE 10. Low Noise Integrator

High-Gain Sallen-Key Active Filters

The CLC5801 is well suited for high-gain Sallen-key type of active filters. *Figure 11* shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods as discussed in OA-21 enables the proper selection of components for these high-frequency filters.

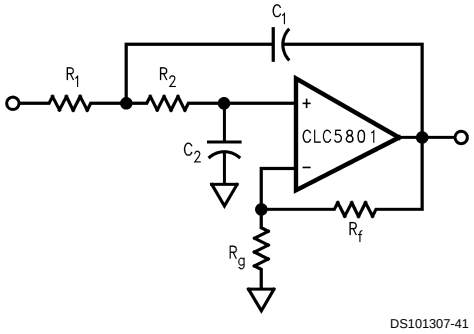


FIGURE 11. Sallen-Key Active Filter Topology

Low Noise Magnetic Media Equalizer

The circuit in *Figure 12* implements a high-performance low-noise equalizer for such applications as magnetic tape channels. The circuit combines an integrator with a bandpass filter to produce the low-noise equalization.

The circuit's simulated frequency response is illustrated in *Figure 13*.

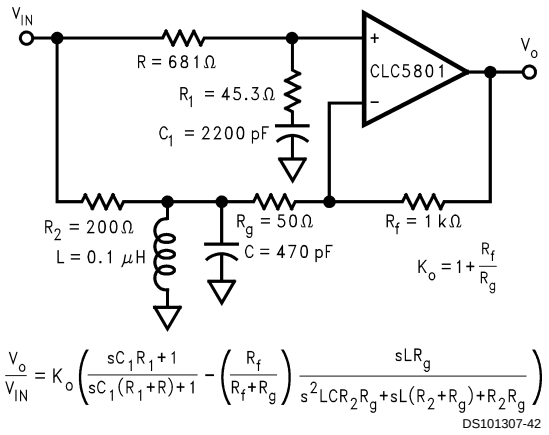


FIGURE 12. Low Noise Magnetic Media Equalizer

Application Information (Continued)

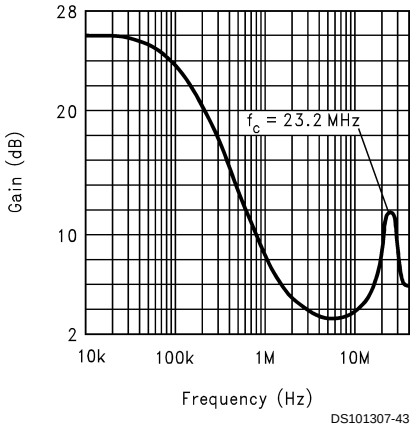


FIGURE 13. Equalizer Frequency Response

Low-Noise Phase-Locked Loop Filter

The CLC5801 is extremely useful as a Phase-Locked Loop filter in such applications as frequency synthesizers and data synchronizers. The circuit of *Figure 14* implements one possible PLL filter with the CLC5801.

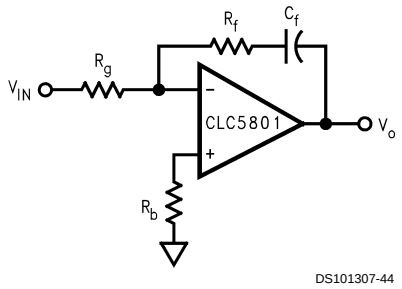
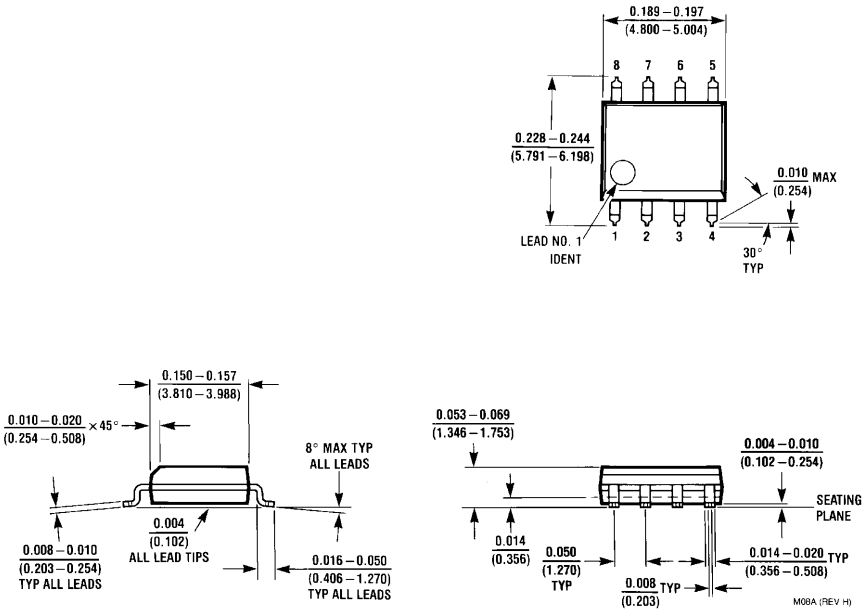


FIGURE 14. Phase-Locked Loop Filter

Printed Circuit Board Layout

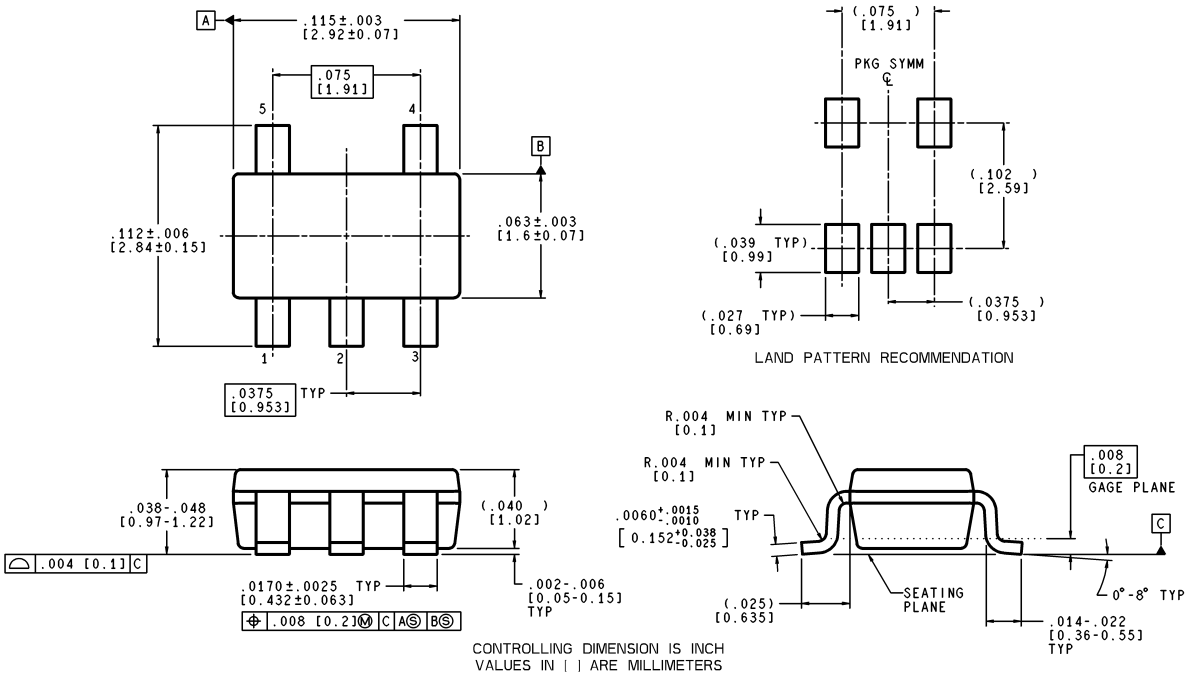
Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. National includes an evaluation board with samples as a guide for high frequency lay-out and as an aid in device testing and characterization.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
Order Numbers CLC5801IM and CLC5801IMX
NS Package Number MA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MF05A (Rev A)

5-Pin SOT23-5
Order Numbers CLC5801IM5 and CLC5801IM5X
NS Package Number MF05A

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