

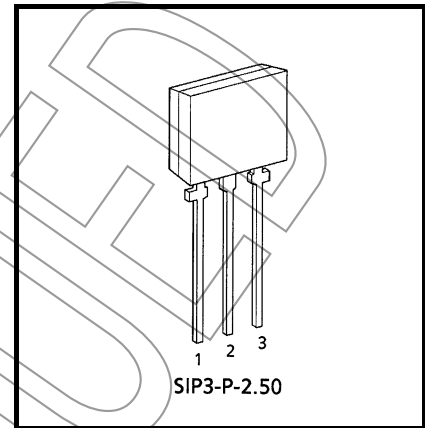
# TPD1024AS

## Low-side Power Switch for Motors, Solenoids, and Lamp Drivers

The TPD1024AS is a monolithic power IC for low-side switches. The IC has a vertical MOS FET output which can be directly driven from a CMOS or TTL logic circuit (e.g., an MPU). The device is equipped with an intelligent self-protection function.

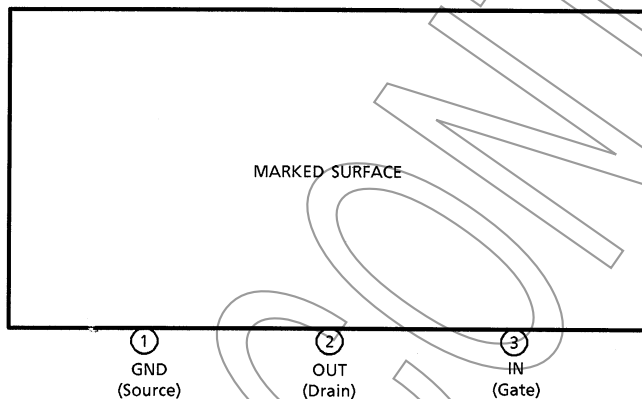
### Features

- A monolithic power IC with a new structure combining a control block and a vertical power MOS FET ( $\pi$ -MOS) on a single chip
- Can directly drive a power load from a CMOS logic.
- Built-in protection against overvoltage, load short-circuiting, and thermal shutdown
- Low on-resistance :  $R_{DS(ON)} = 0.5 \, \Omega$  (max) (@ $V_{IN} = 5 \, V$ ,  $T_j = 25^\circ C$ )
- Package : TPS that can be packed in tape.



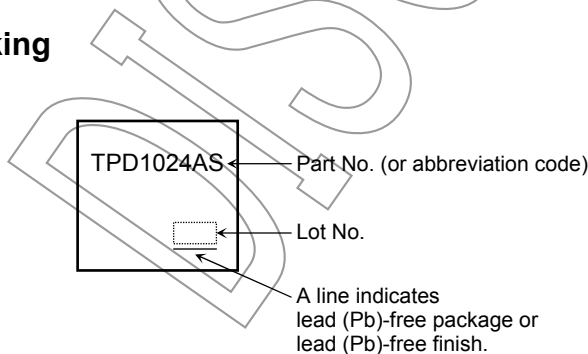
Weight: 0.54g (typ.)

### Pin Assignment

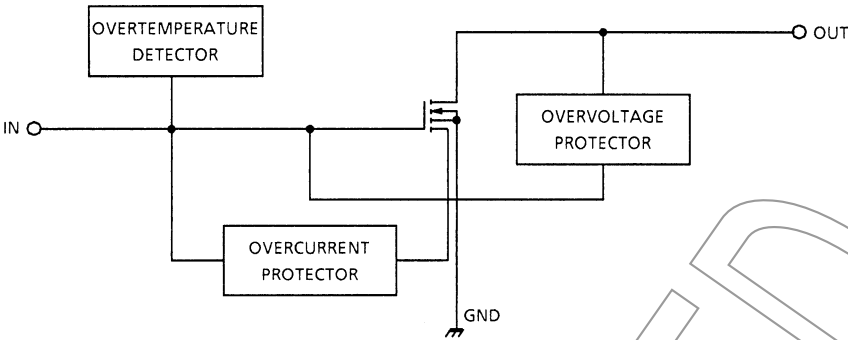


Note: Due to its MOS structure, this product is sensitive to static electricity.

### Marking



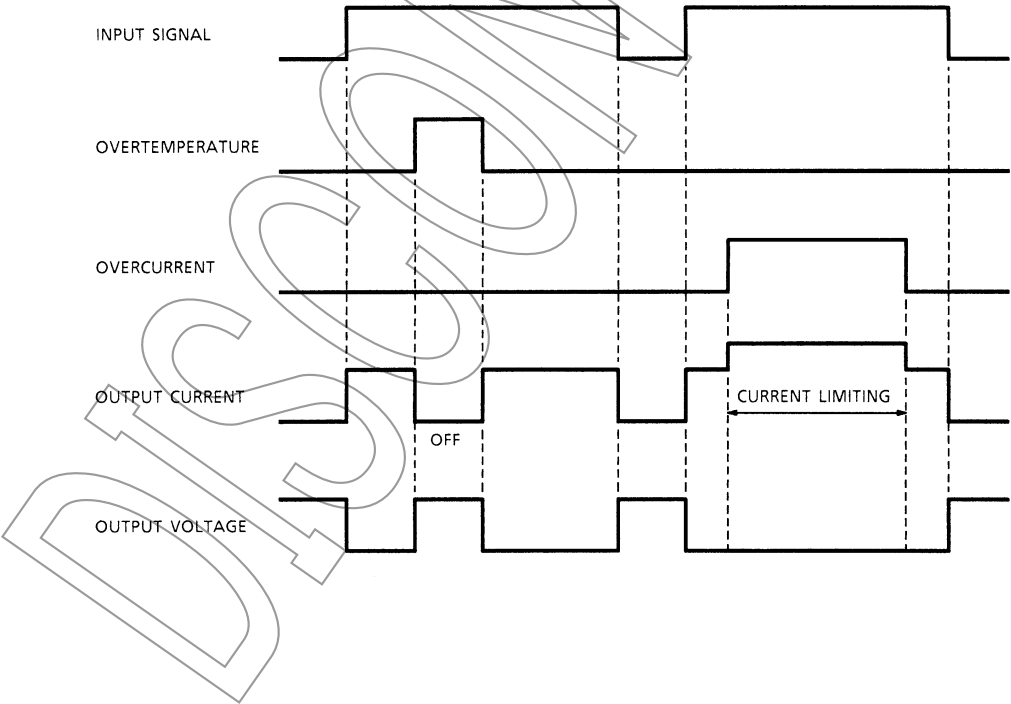
Block Diagram



Pin Description

Pin No.	Symbol	Function
1	GND	Ground pin.
2	OUT	Output pin. When current in excess of the typical current (3.5 A (typ.)) flows to the output pin, the current limiter operates to protect the IC.
3	IN	Input pin. Input is CMOS-compatible, with pull-down resistor connected. Even if the input is open, output will not accidentally turn on.

Timing Chart



## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$ (DC)	40	V
Output current	$I_D$	1.5	A
Input voltage	$V_{GS}$	- 0.5 to 6	V
Power dissipation	$P_D$	1.2	W
Operating temperature	$T_{opr}$	- 40 to 85	°C
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	- 55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

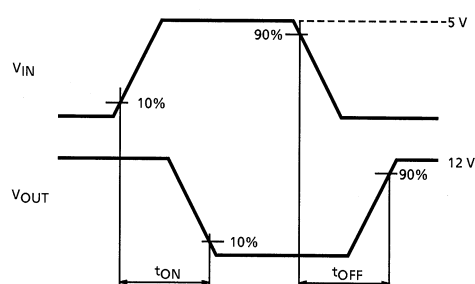
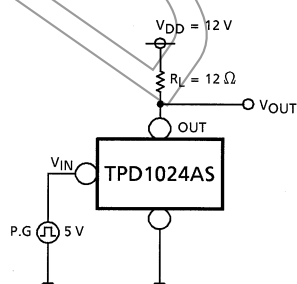
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

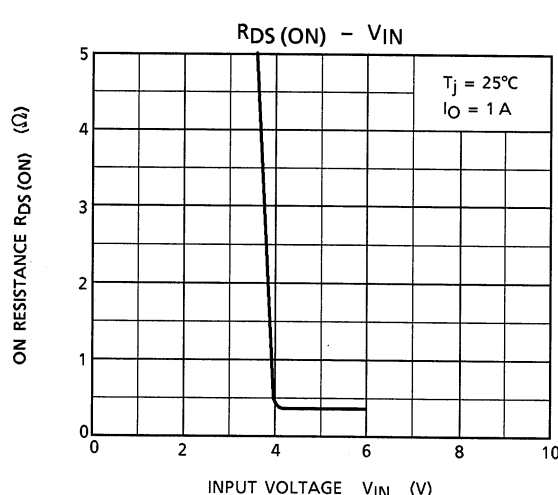
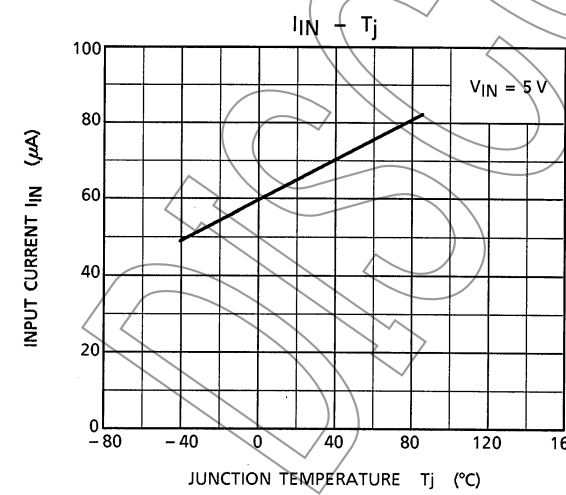
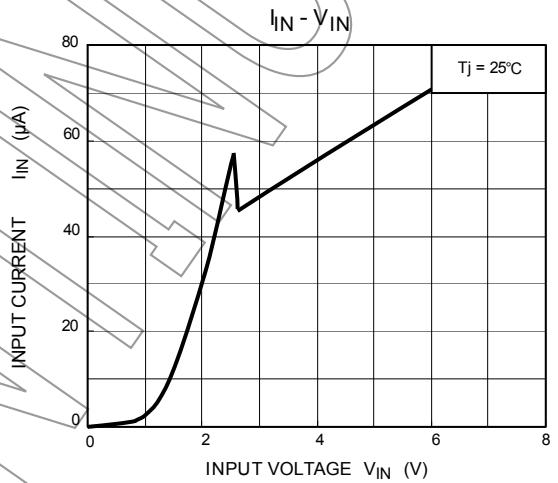
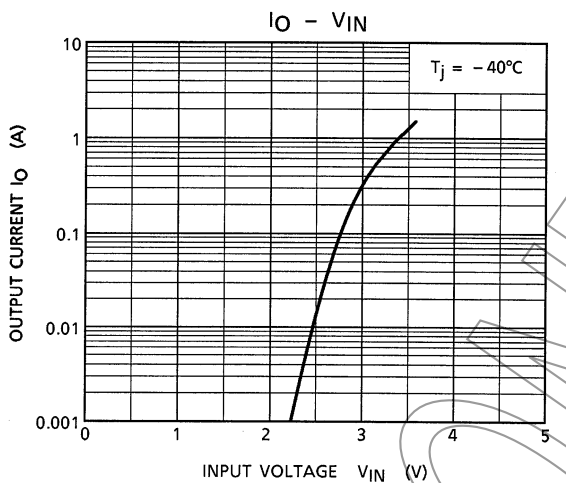
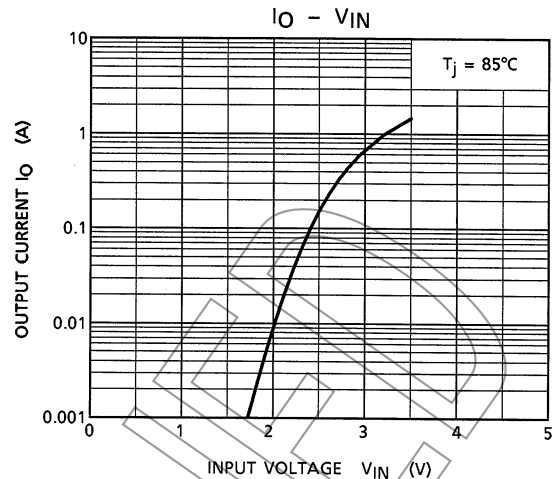
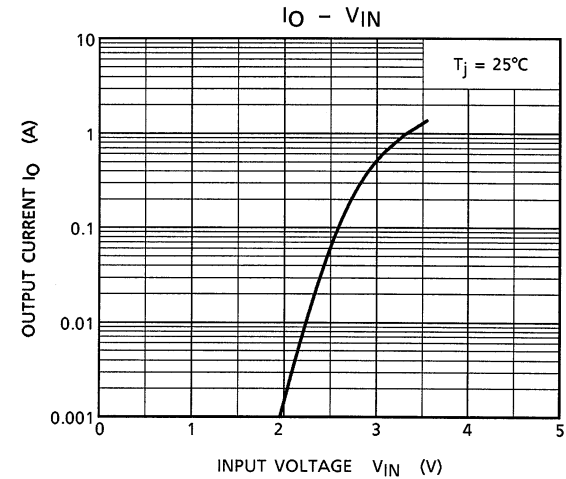
## Electrical Characteristics (Tj = 25°C)

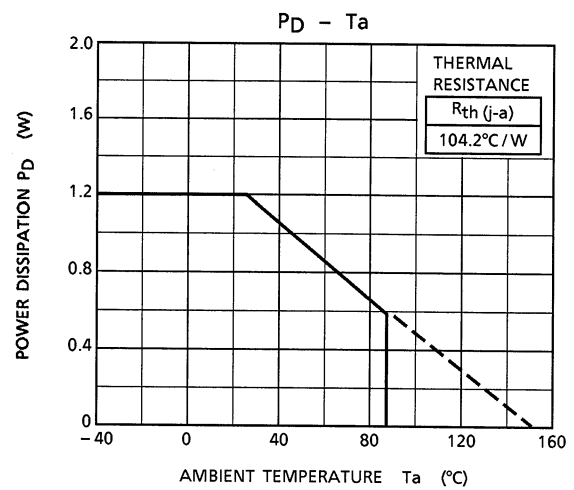
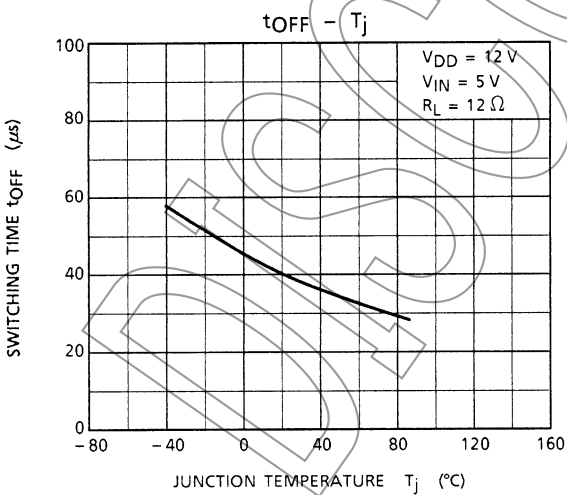
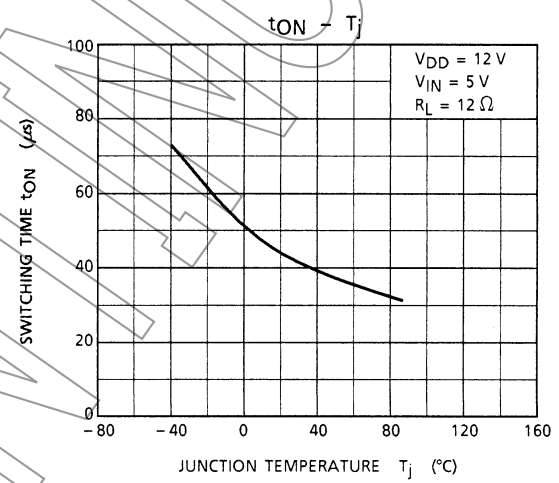
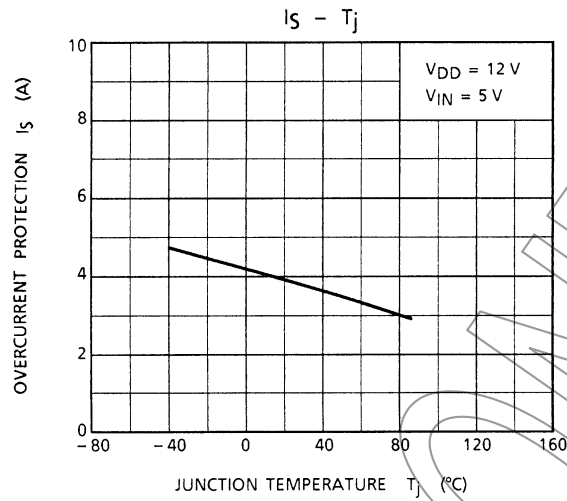
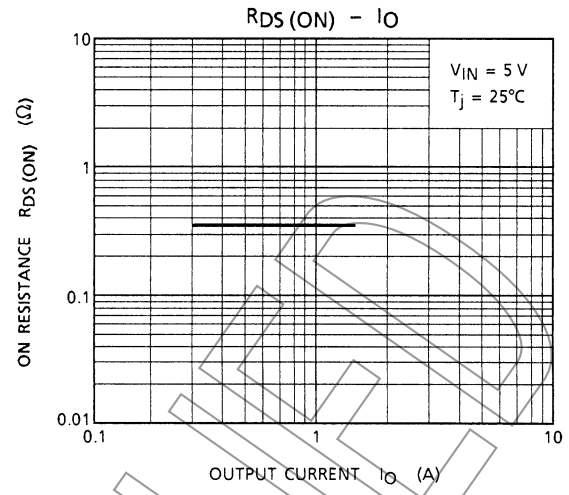
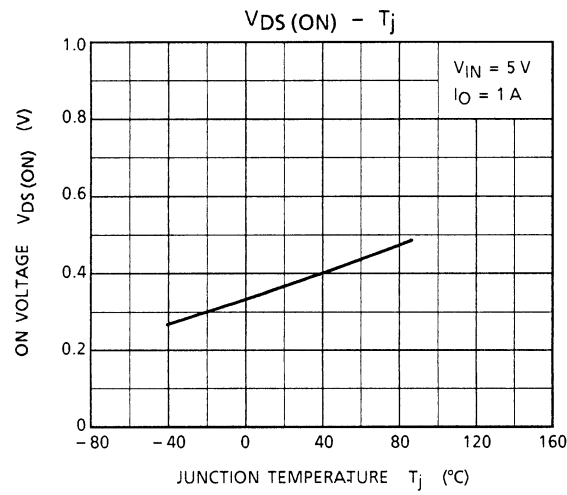
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	—	$V_{GS} = 0, I_D = 10 \text{ mA}$	40	—	—	V
Operating supply voltage	$V_{DD}$ (OPR)	—	—	—	—	18	V
Current at output off	$I_{DSS}(1)$	—	$V_{GS} = 0, V_{DS} = 40 \text{ V}$	—	—	3	mA
	$I_{DSS}(2)$	—	$V_{GS} = 0, V_{DS} = 24 \text{ V}$	—	—	100	μA
Input threshold voltage	$V_{th}$	—	$V_{GS} = 10 \text{ V}, I_D = 1 \text{ mA}$	0.8	—	2.5	V
Input current	$I_{GSS}$	—	$V_{GS} = 5 \text{ V}$ , at normal operation	—	—	300	μA
On-resistance	$R_{DS(ON)}$	—	$V_{GS} = 5 \text{ V}, I_D = 1 \text{ A}$	—	—	0.5	Ω
Thermal shutdown temperature	$T_S$	—	—	—	160	—	°C
Overcurrent protection	$I_S$	—	$V_{DS} = 12 \text{ V}, V_{GS} = 5 \text{ V}$	—	3.5	—	A
Switching time	$t_{ON}$	1	$V_{DS} = 12 \text{ V}, V_{GS} = 5 \text{ V}$ , $R_L = 12 \text{ Ω}$	—	50	—	μs
	$t_{OFF}$			—	10	—	μs
Diode forward voltage between drain and source	$V_{DSF}$	—	$I_F = 1.5 \text{ A}$	—	0.9	1.8	V
Avalanche energy	$E_A$	—	$L = 10 \text{ mH}$ , Single pulse	30	—	—	mJ

## Test Circuit 1

## Switching Time



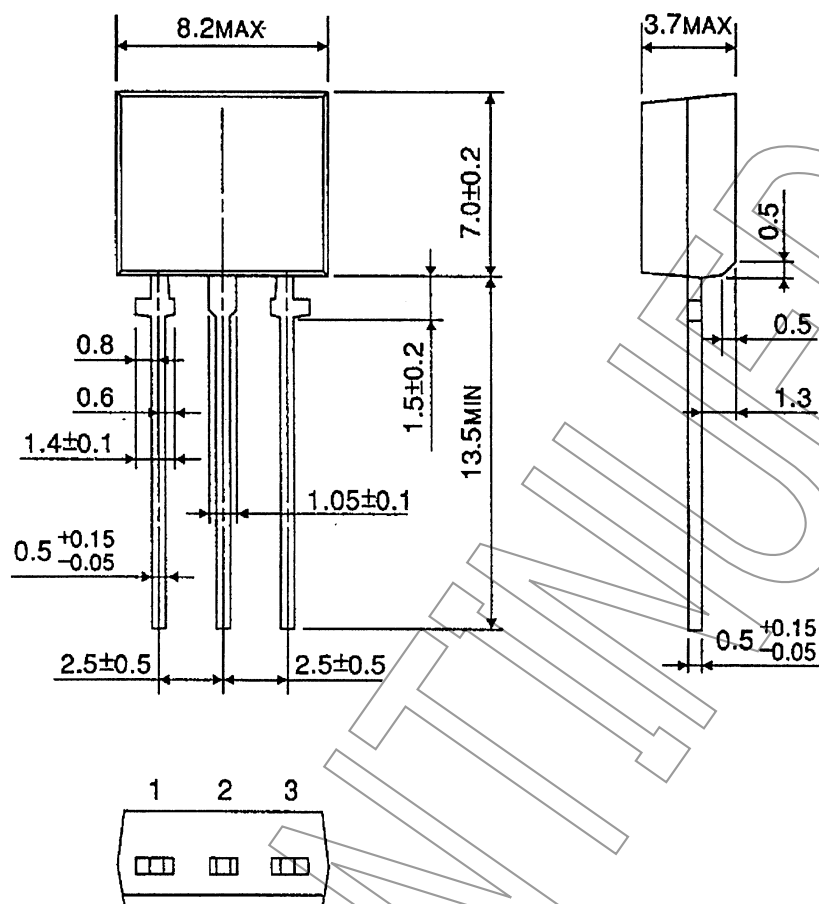




## Package Dimensions

SIP3-P-2.50

Unit : mm



Weight: 0.54g (typ.)

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