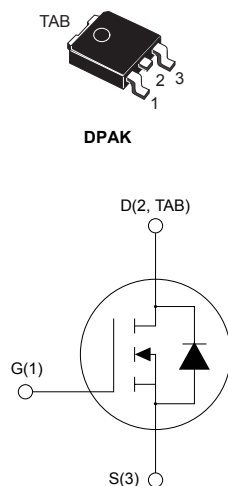


N-channel 650 V, 230 mΩ typ., 12 A MDmesh M5 Power MOSFET in a DPAK package



AM01475v1_noZen



Product status link

[STD16N65M5](#)

Product summary

Order code	STD16N65M5
Marking	16N65M5
Package	DPAK
Packing	Tape and reel

Features

Order codes	V_{DS} at $T_{jmax.}$	$R_{DS(on)}$ max.	I_D
STD16N65M5	710 V	279 mΩ	12 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	12	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	7.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	90	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_j	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 400\text{ V}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.38	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$,			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			± 100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$		230	279	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1250	-	pF
C_{oss}	Output capacitance			30		
C_{rss}	Reverse transfer capacitance			3		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	100	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	30	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 0$ to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge			8		
Q_{gd}	Gate-drain charge			12		

1. $C_{o(tr)}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 8\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	25	-	ns
$t_{r(v)}$	Voltage rise time			7		
$t_{f(i)}$	Current fall time			6		
$t_{c(off)}$	Crossing time			8		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		12	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				48	
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 12 A, V _{GS} = 0 V	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 12 A, di/dt = 100 A/μs	-	300		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)		3.5		μC
I _{RRM}	Reverse recovery current			23		A
t _{rr}	Reverse recovery time	I _{SD} = 12 A, di/dt = 100 A/μs	-	350		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)		4		μC
I _{RRM}	Reverse recovery current			24		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

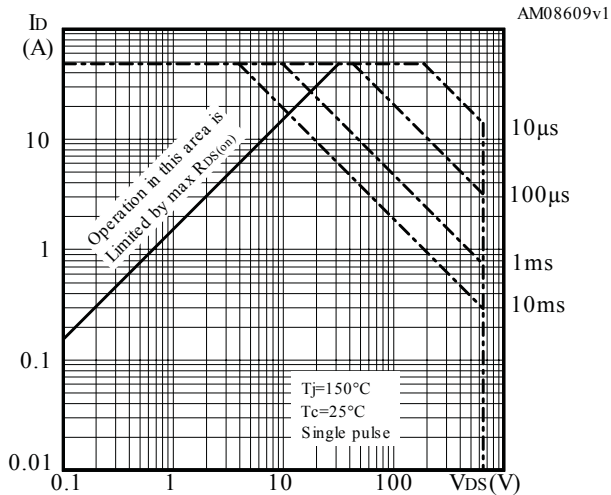


Figure 2. Thermal impedance

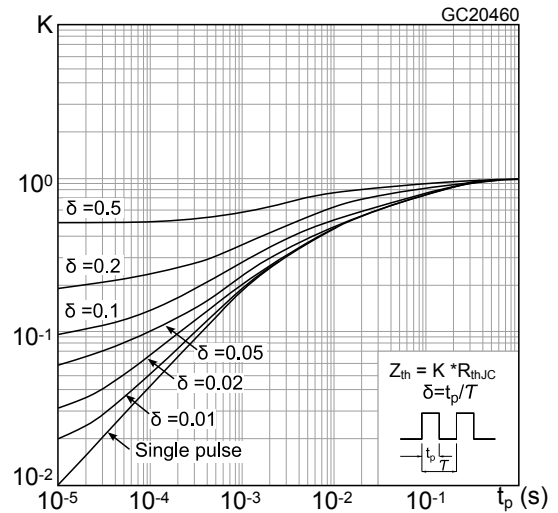


Figure 3. Output characteristics

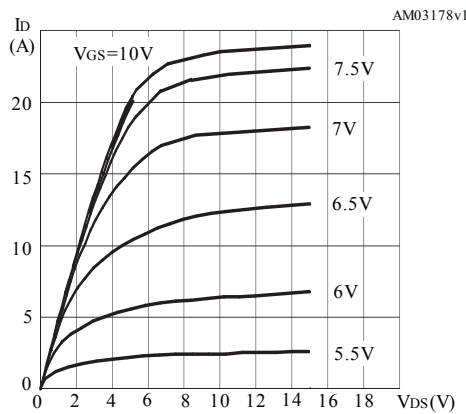


Figure 4. Transfer characteristics

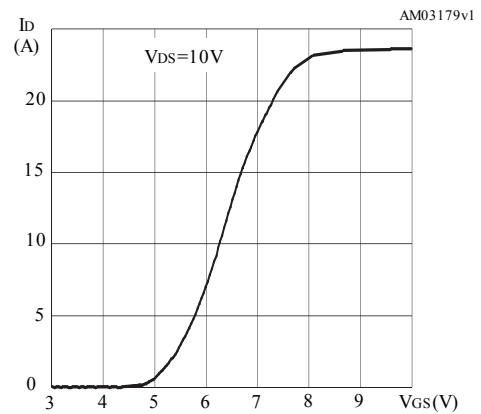


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

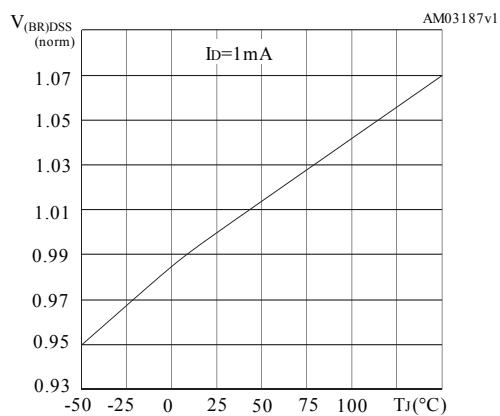


Figure 6. Static drain-source on resistance

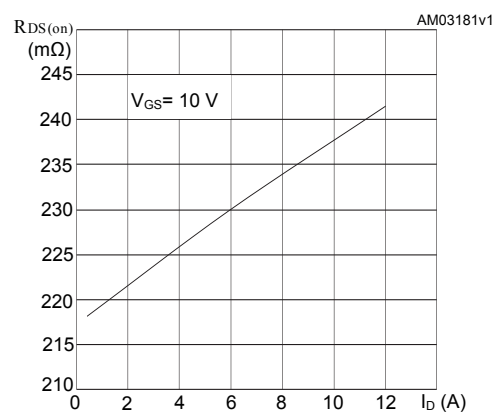


Figure 7. Output capacitance stored energy

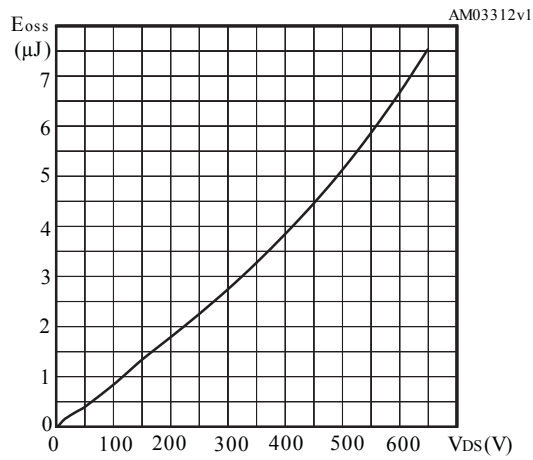


Figure 8. Capacitance variations

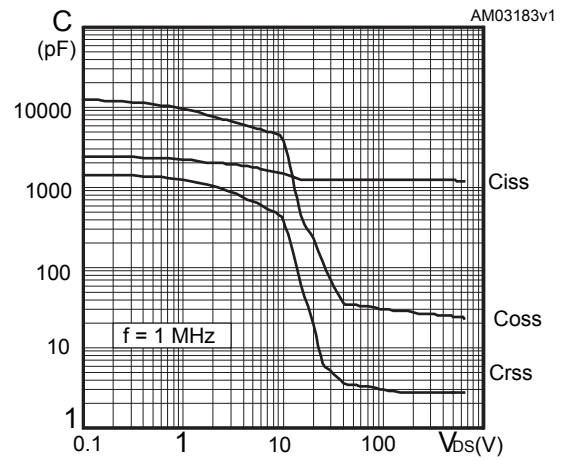


Figure 9. Gate charge vs gate-source voltage

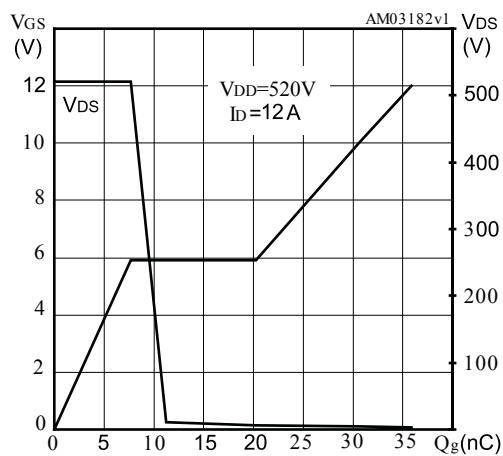


Figure 10. Normalized on resistance vs temperature

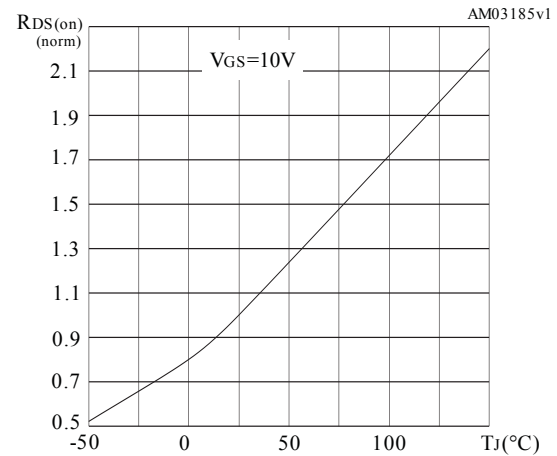


Figure 11. Normalized gate threshold voltage vs temperature

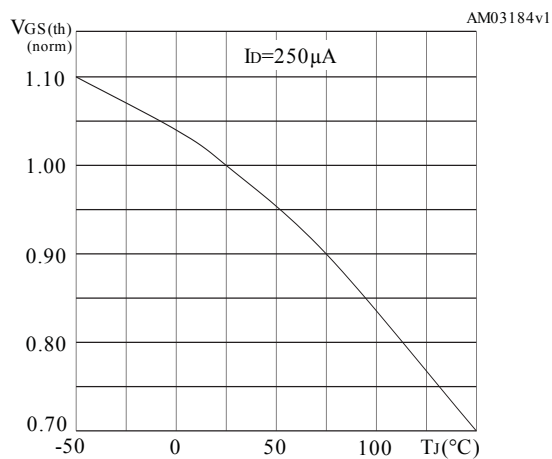


Figure 12. Source-drain diode forward characteristics

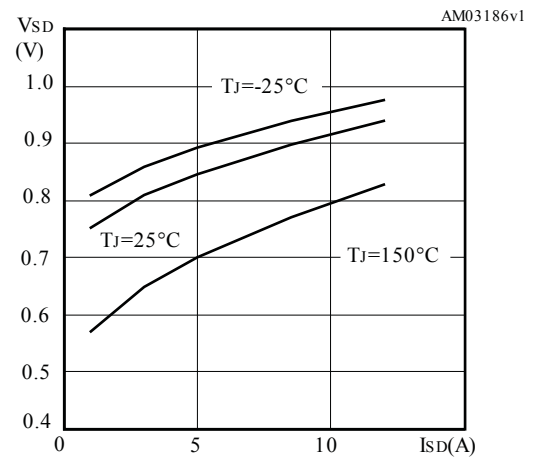
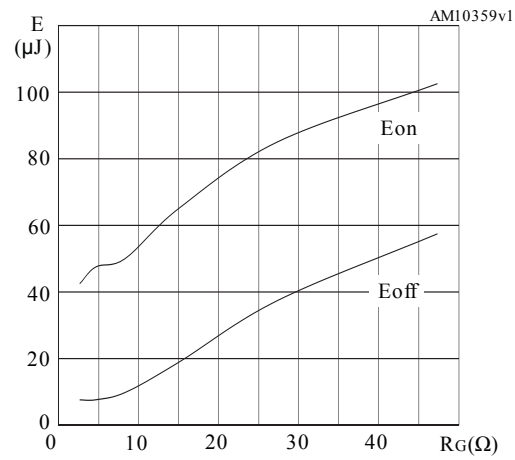
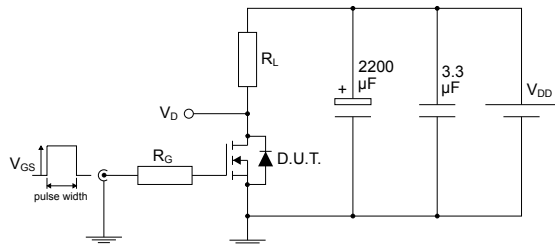


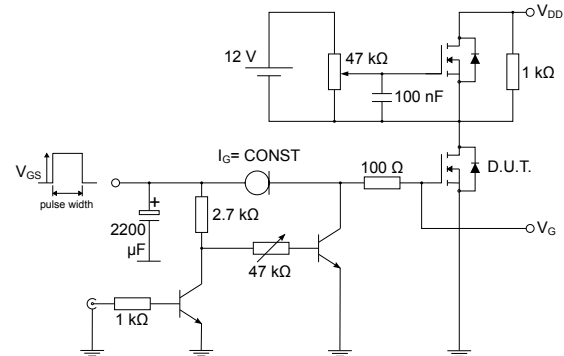
Figure 13. Switching energy vs gate resistance



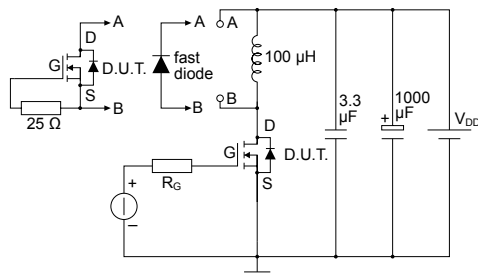
3 Test circuits

Figure 14. Test circuit for resistive load switching times


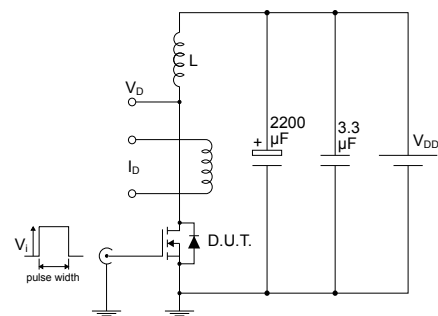
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Figure 15. Test circuit for gate charge behavior


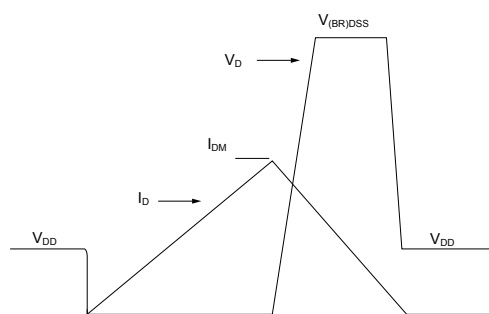
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Figure 16. Test circuit for inductive load switching and diode recovery times


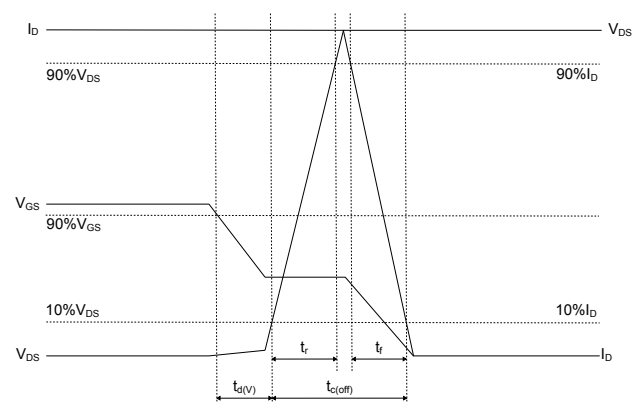
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


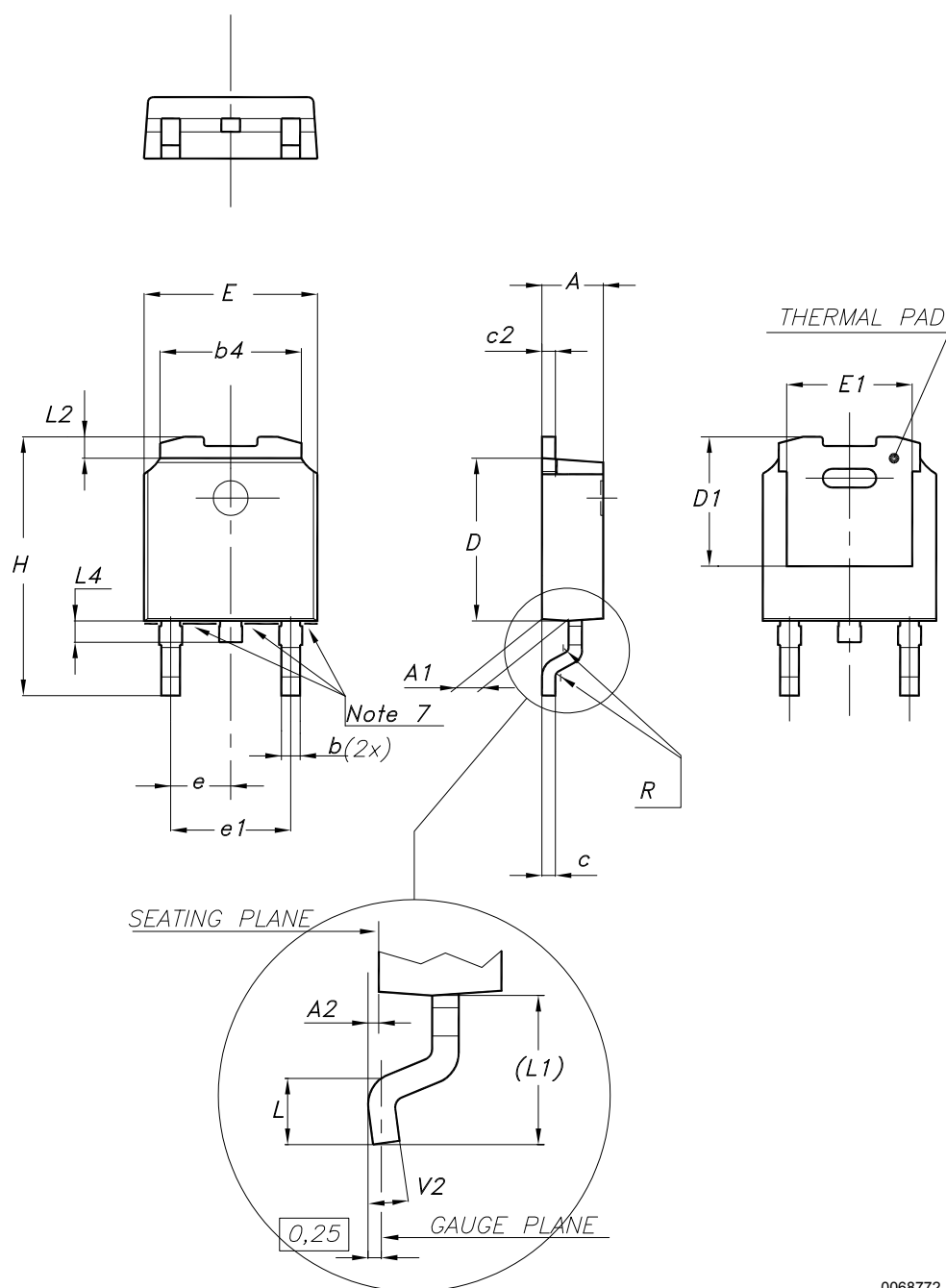
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20. DPAK (TO-252) type A2 package outline



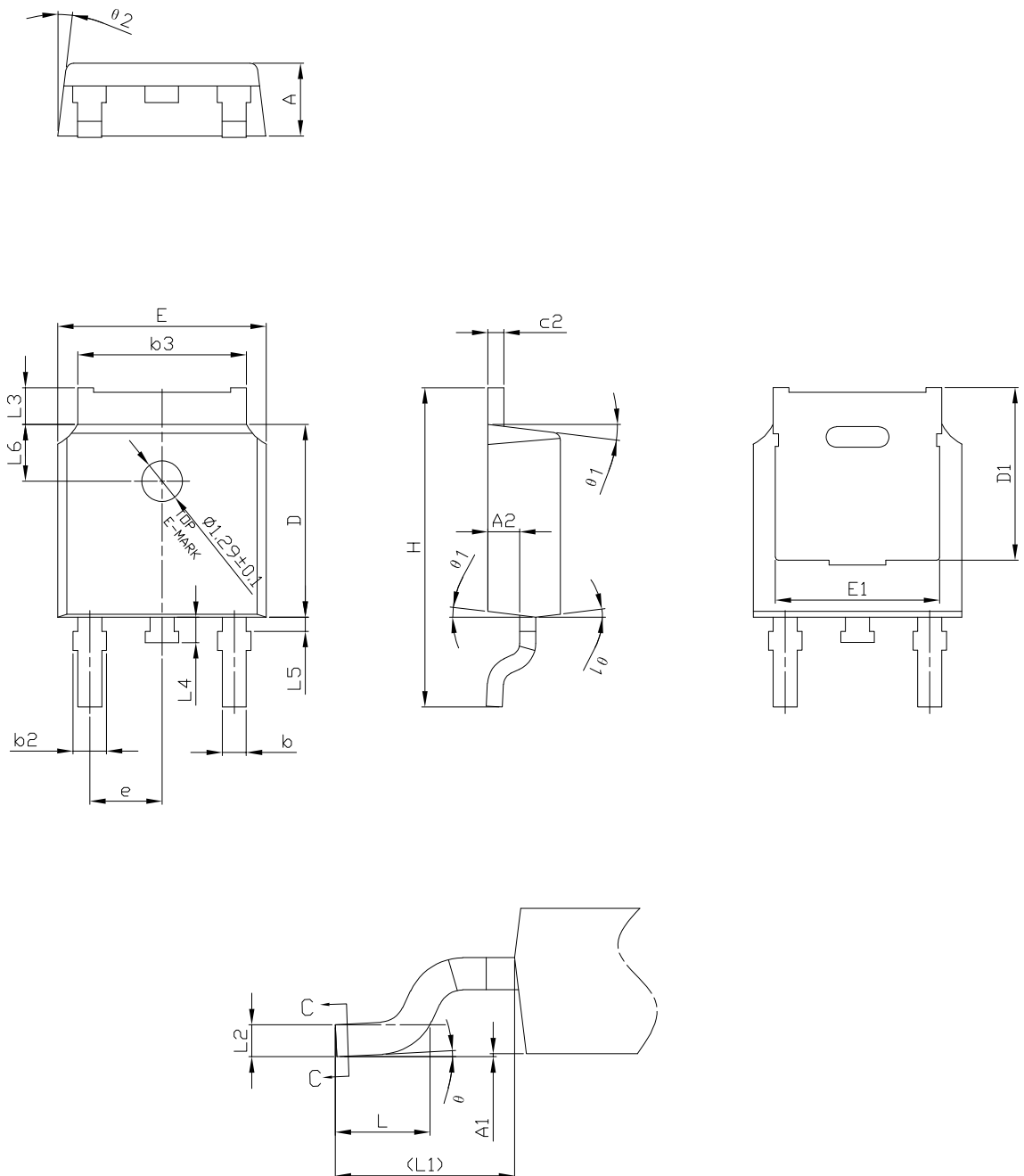
0068772_type-A2_rev34

Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C3 package information

Figure 21. DPAK (TO-252) type C3 package outline



0068772_type-C3_rev34

Table 9. DPAK (TO-252) type C3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

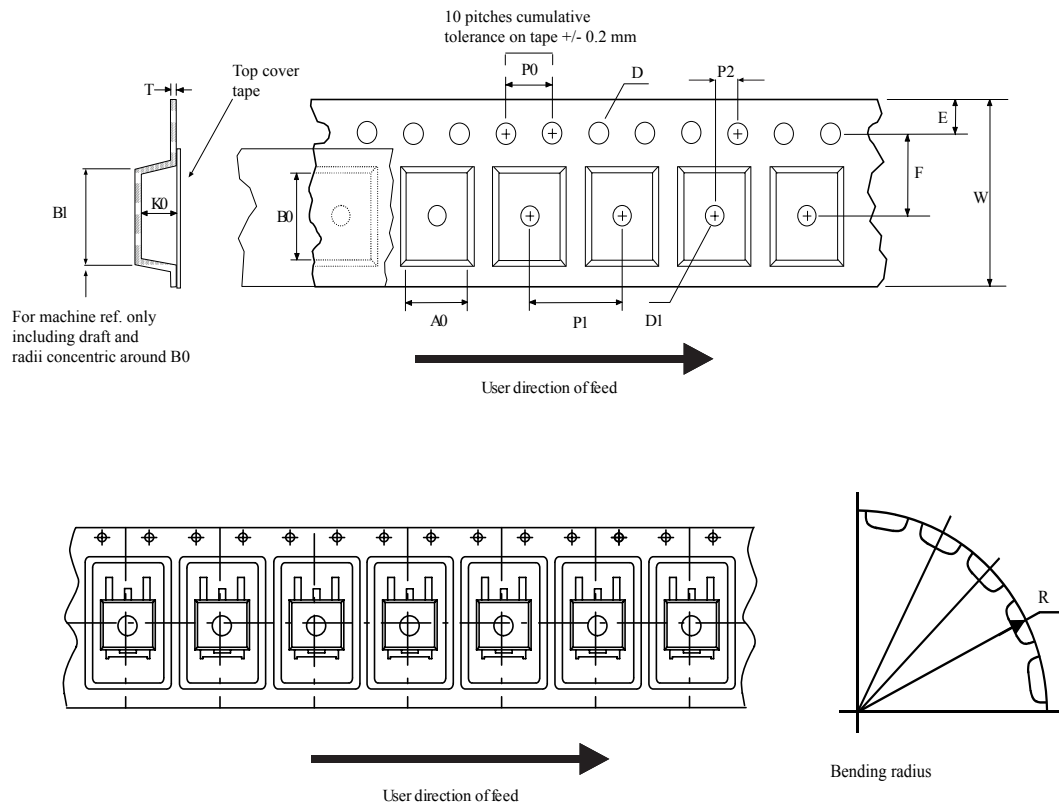
Technical drawing of a mechanical part. The drawing shows a top view and a side view. The top view is a rectangle with a width of 6.3 and a height of 6.5. The side view is a rectangle with a width of 11.2 and a height of 1.8 MIN. The part has two rectangular features on the top surface, each with a width of 1.5 and a height of 2.9. The distance between the centers of these two features is 4.572. The drawing includes section lines (hatching) and dimension lines with arrows. A section line A-A is shown at the bottom, and a section line B-B is shown on the right.

2) The device must be positioned within $\oplus 0.05 \text{ A B}$

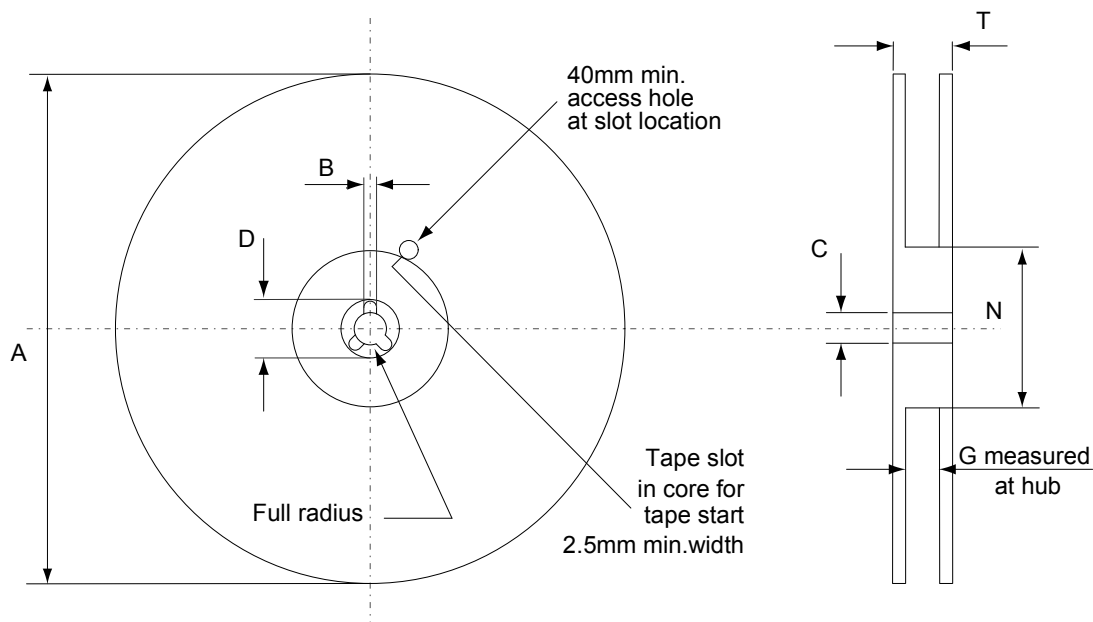
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4.3 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline



AM08852v1

Figure 24. DPAK (TO-252) reel outline


AM06038v1

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. Document revision history

Date	Version	Changes
09-Nov-2010	1	First release.
14-Oct-2011	2	Modified <i>Section 2.1: Electrical characteristics (curves)</i>: – <i>Figure 6, Figure 7, Figure 8, Figure 9, Figure 13 and Figure 14</i> – Added <i>Figure 15</i> Updated $R_{DS(on)}$ value in coverpage and in <i>Table 4</i> Updated values in <i>Table 6</i> Updated <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i>. Minor text changes.
20-Nov-2018	3	Removed maturity status indication from cover page. The document status is production data. The part number STB16N65M5 has been moved to a separate datasheet. Updated <i>Section 4 Package information</i>. Minor text changes.
15-May-2023	4	Updated <i>Section 4.1 DPAK (TO-252) type A2 package information</i>. Added <i>Section 4.2 DPAK (TO-252) type C3 package information</i>. Minor text changes.

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4.3	DPAK (TO-252) packing information	14
	Revision history	16

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