MN3646

2880-Bit High-Responsivity CCD Linear Image Sensor

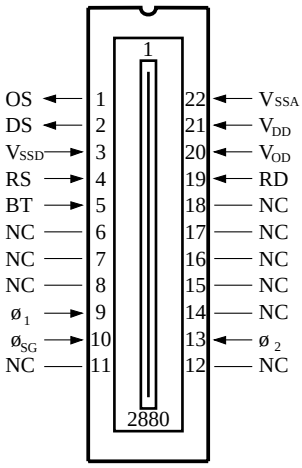
■ Overview

The MN3646 is a 2880-pixel high sensitivity CCD linear image sensor combining photo-sites using low dark output floating photodiodes and CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■ Features

- 2880 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Operates on +5V single power supply and can driven by 5V CMOS logic.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- Has a smooth spectral response that is close to the sensitivity of the human eye in the entire visible region.
- Large signal output of typically 1200mV at saturation can be obtained.
- Since a compensation output pin (DS) is provided in addition to the signal output pin (OS), it is possible to obtain a signal with a high S/N ratio by carrying out differential amplification of the OS and DS outputs.

■ Pin Assignments



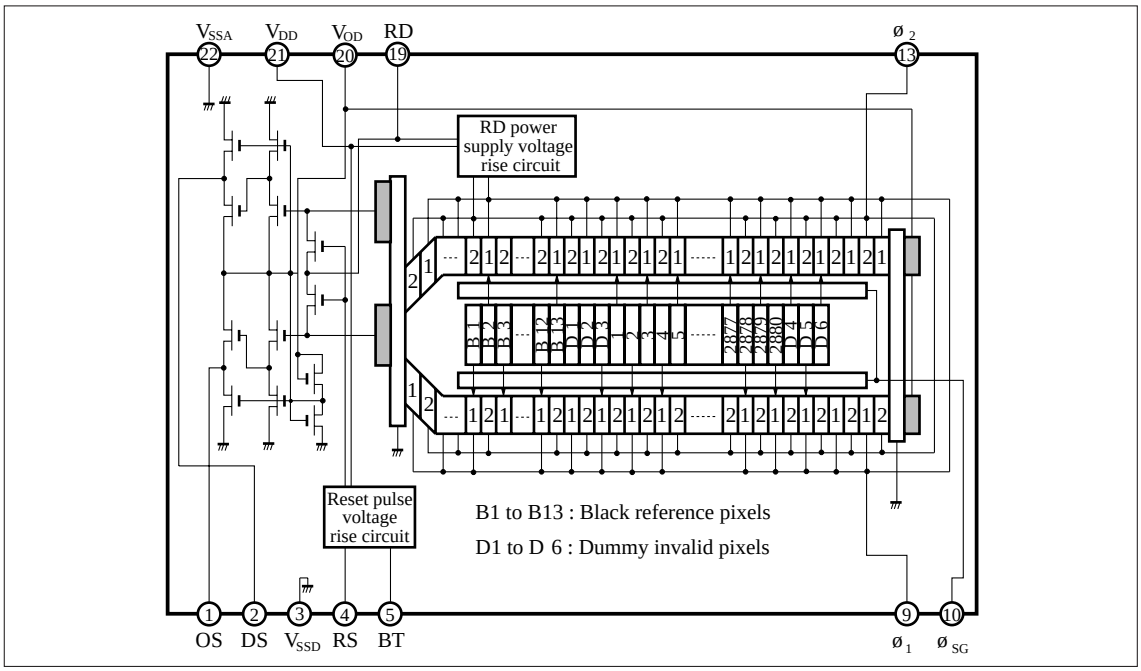
(Top View)

C20 WDIP022-G-0470

■ Application

- Barcode readers
- Measurement of position and dimensions of objects.

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C, V_{SSA}=V_{SSD}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +8.0	V
	V_{OD}	– 0.3 to +8.0	V
Input pin voltage	V_I	– 0.3 to +8.0	V
Output pin voltage	V_O	– 0.3 to +8.0	V
Operating temperature range	T_{opr}	–20 to + 60	˚C
Storage temperature range	T_{stg}	–40 to +100	˚C

■ Operating Conditions

• Voltage conditions (Ta=–20 to +60˚C, V_{SSA}=V_{SSD}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Internal digital circuit power supply voltage	V_{DD}	V_{DD}=V_{OD}	4.5	5.0	5.5	V
CCD output circuit power supply voltage	V_{OD}		4.5	5.0	5.5	V
CCD shift register clock High level	$V_{øH}$		4.5	5.0	5.5	V
CCD shift register clock Low level	$V_{øL}$		0	0.2	0.5	V
Shift gate clock High level	V_{SH}		4.5	5.0	5.5	V
Shift gate clock Low level	V_{SL}		0	0.2	0.5	V
Reset gate clock High level	V_{RH}		4.5	5.0	5.5	V
Reset gate clock Low level	V_{RL}		0	0.2	0.5	V
Boot gate clock High level	V_{BH}		4.5	5.0	5.5	V
Boot gate clock Low level	V_{BL}		0	0.2	0.5	V

• Timing conditions (Ta=–20 to +60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	f_C=1/2T, f_R=1/T=data rate	40	250	1000	kHz
Reset clock frequency	f_R	See timing diagram. Note 1	80	500	2000	kHz
Shift register clock rise time	$t_{ør}$	See timing diagram	0	60	100	ns
Shift regisster clock fall time	$t_{øf}$		0	60	100	ns
Shift clock rise time	t_{Sr}	See timing diagram Note 2	0	50	100	ns
Shift clock fall time	t_{Sf}		0	50	100	ns
Shift clock set up time	t_{Ss}		0	100	1000	ns
Shift clock pulse width	t_{Sw}		100	200	500	µs
Shift clock hold time	t_{Sh}		0	1.0	10	µs
Reset clock rise time	t_{Rr}	See timing diagram	0	20	50	ns
Reset clock fall time	t_{Rf}		0	20	50	ns
Reset clock set up time	t_{Rs}		50	100	—	ns
Reset clock pulse width	t_{Rw}		60	250	—	ns
Reset clock hold time	t_{Rh}		20	—	—	ns
Boost clock rise time	t_{Br}	See timing diagram Note 3	0	20	50	ns
Boost clock fall time	t_{Bf}		0	20	50	ns
Boosst clock set up time	t_{Bs}		20	30	—	ns
Reseet active period	t_{RBw}		100	—	—	ns
Boost clock hold time	t_{Bh}		200	—	—	ns

Note 1) Since the dark output of the CCD shift register region increases and the dynamic range decreases as the shift register clock frequency f_C becomes lower, use the device in the range of f_C at which the required dynamic range can be obtained.

Note 2) Care should be taken because making the shift clock pulse width t_{Sw} smaller has the tendency to increase the lag (= the image left over from the signal scanned during the previous period).

Note 3) A step will be present in the reset pulse waveform if the boost clock set up time t_{Bs} becomes too long.

■ Electrical Characteristics

• Clock input capacitance

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	$C_{ø}$	f =1MHz	—	550	650	pF
Shift gate clock input capacitance	C_S		—	150	200	pF
Reset gate clock input capacitance	C_R		—	15	30	pF
Boost gate clock input capacitance	C_B		—	20	30	pF

• DC characteristics (Ta=–20 to +60˚C, V_{SSA}=V_{SSD}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Digital power supply current	I_{DD}	V_{DD}=V_{OD} =+5V	—	0.5	1.0	mA
Analog power supply current	I_{OD}	f_R=500kHz	—	1.5	3.0	mA

■ Optical Characteristics

<Inspection conditions>

• Ta=25˚C, V_{DD}=V_{OD}=5V, V$ø_H$=V_{SH}=V_{RH}=V_{BH}=5V (pulse), f_C=250kHz, f_R=500kHz, T_{int} (accumulation time)=10ms

• Light source: Red-color LED (Peak wavelength: 660nm±10nm)

• Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).

• Load resistance = 100k Ohms

• These specifications apply to the 2880 valid pixels excluding the dummy pixels D1 to D6.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R		170	210	250	V/lx· s
Photo response non-uniformity	PRNU	Note 1	—	—	10	%
Odd/even bit non-uniformity	O/E	Note 2	—	—	3	%
Saturation output voltage	V_{SAT}	Note 3	800	1200	—	mV
Saturation exposure	SE	Note 3	3.2	5.7	—	mlx·s
Dark signal output voltage	V_{DRK}	Dark condition, see Note 4	—	0.2	1.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 4	—	0.1	2.0	mV
Shift register total transfer efficiency	STTE		92	—	—	%
Output impedance	Z_O		—	1.0	1.5	kΩ
Dynamic range	DR	Note 5	—	6000	—	
Signal output pin DC level	V_{OS}	Note 6	1.5	2.5	3.5	V
Compensation output pin DC level	V_{DS}	Note 6	1.5	2.5	3.5	V
Signal and compensation output pin DC level difference	$\lvert V_{OS} - V_{DS} \rvert$	Note 6	—	30	100	mV

Note 1) The photo response non-uniformity (PRNU) is defined by the following equation, where X_{ave} is the average output voltage of the 2880 valid pixels and Δx is the absolute value of the difference between X_{ave} and the voltage of the maximum (or minimum) output pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$PRNU = \frac{\triangle x}{X_{ave}} \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

Note 2) The odd/even bit non-uniformity (O/E) is defined by the following equation, where X_{ave} is the average output voltage of the 2880 valid pixels and Xn is the output voltage of the 'n'th pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$O/E = \frac{\sum_{n=1}^{2879} \lvert Xn - Xn_{+1} \rvert}{2879 \times X_{ave}} \times 100\ (\%)$$

In other words, this is the value obtained by dividing the average of the output difference between the odd and even pixels by the average output voltage of all the valid pixels. The incident light intensity shall be 50% of the standard saturation light intensity.

■ Optical Characteristics (continued)

Note 3) The Saturation output voltage (V_{SAT}) is defined as the output voltage at the point when the linearity of the photoelectric characteristics cannot be maintained as the incident light intensity is increased. (The light intensity of exposure at this point is called the saturation exposure.)

Note 4) The dark signal output voltage (V_{DRK}) is defined as the average output voltage of the 2880 pixels in the dark condition at Ta=25˚C and T_{int}=10ms. Normally, the dark output voltage doubles for every 8 to 10˚C rise in Ta, and is proportional to T_{int}.

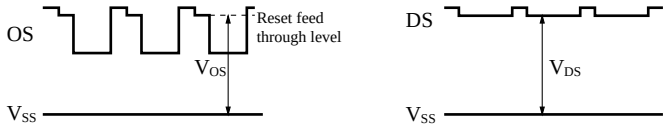
The dark signal output non-uniformity (DSNU) is defined as the difference between the maximum output voltage among all the valid pixels and V_{DRK} in the dark condition at Ta=25˚C and T_{int}=10ms.

Note 5) The dynamic range is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

Note 6) The signal output pin DC level (V_{OS}) and the compensation output pin DC level (V_{DS}) are the voltage values shown in the following figure.



■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	
2	DS	Compensation output	
3	V_{SSD}	Digital ground	Ground pin for the internal digital circuit.
4	RS	Reset clock	
5	BT	Boost clock	
6	NC	Non connection	
7	NC	Non connection	
8	NC	Non connection	
9	$ø_1$	Transfer clock (Phase 1)	
10	$ø_{SG}$	Shift clock	
11	NC	Non connection	
12	NC	Non connection	
13	$ø_2$	Transfer clock (Phase 2)	
14	NC	Non connection	
15	NC	Non connection	
16	NC	Non connection	
17	NC	Non connection	
18	NC	Non connection	
19	RD	Reset drain	Apply capacitance of 3,300pF externally.
20	V_{OD}	Analog power supply	
21	V_{DD}	Digital power supply	
22	V_{SSA}	Analog ground	Ground pin for the internal analog circuit.

Note 1) It is possible to expect improvement in the S/N ratio by connecting separately the analog power supply pins (V_{OD}, V_{SSA}) and the digital power supply pins (V_{DD}, V_{SSD}) respectively to the analog side pattern and the digital side pattern on the circuit board for driving the CCD.

Note 2) Connect all NC pins externally to V_{SSA}.

■ Construction of the Image Sensor

The MN3646 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of a 7µm floating photodiode and a 3µm channel stopper for each pixel, and 2880 of these devices are linearly arranged side by side at a pitch of 10µm.
- The photo detector's windows are 10µm × 200µm rectangle and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 13 optically shielded pixels (black reference pixels) which serve as the black reference.

b) CCD Transfer region (shift register)

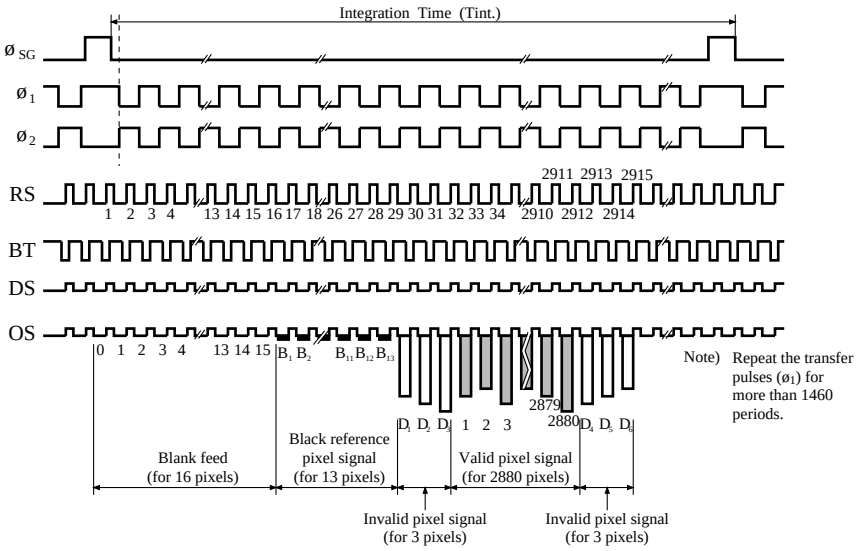
- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock ($ø_{SG}$). The optical signal electric charge transferred to this analog shift register is successively transferred out and guided to the output region.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register.

c) Output region

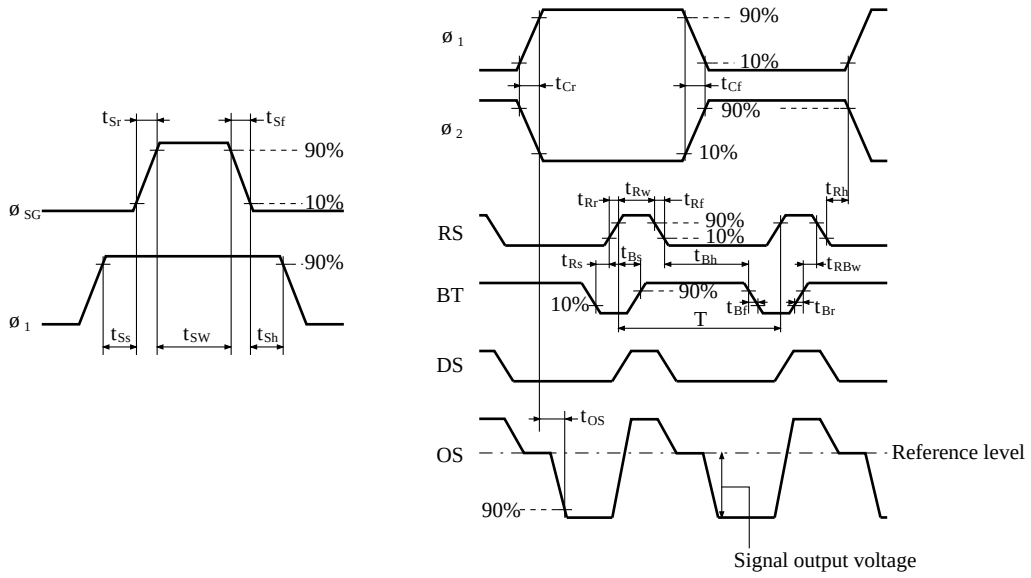
- The signal charge that is transferred to the output region is sent to the detector where impedance transformation is done using two source follower stages.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

■ Timing Diagram

(1) I/O timing

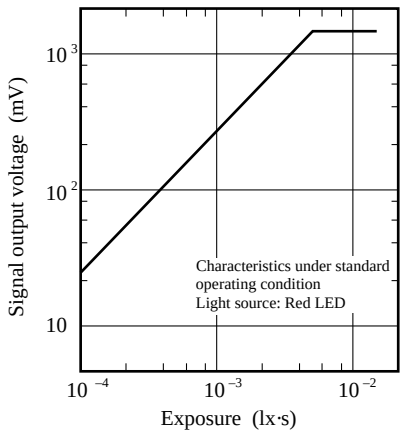


(2) Drive timing



■ Graphs and Characteristics

Photoelectric Conversion Characteristics



Spectral Response Characteristics