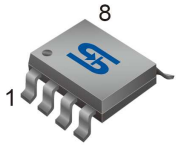
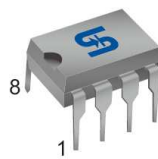


SOP-8



DIP-8



Pin Definition:

- | | |
|--------|------------|
| 1. SC | 5. Comp |
| 2. SE | 6. Vcc |
| 3. CT | 7. Ipk |
| 4. Gnd | 8. Vdriver |

General Description

TS34063 is a monolithic switching regulator and subsystem intended for use as DC to DC converter. It contains an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, drive and a high current output switch. The TS34063 is specifically designed to be incorporated in step-up, step-down and voltage inverting converter applications. TS34063 is offered in SOP-8 and DIP-8 package

Features

- Power forward control circuit
- Operating voltage from 3V to 40V
- Low standby current
- Current limit adjustable
- Output switch current up to 1.5A
- Variable oscillator frequency up to 100kHz(max.)
- Output voltage adjustable

Pin Description

Name	Description
SC	Switch Collector
SE	Switch Emitter
CT	Timing Capacitor
GND	Ground
COMP.	Comparator Inverting Input
V _{CC}	V _{CC} Collector
I _{PK}	IPK Sense
V _{DRIVER}	Driver

Applications

- Charger
- xD-ROM, xDSL products
- DC to DC converter

Ordering Information

Part No.	Package	Packing
TS34063CD C3	DIP-8	50pcs / Tube
TS34063CS RL	SOP-8	2.5Kpcs / 13" Reel

Absolute Maximum Rating

Parameter	Symbol	Maximum	Unit
Supply Voltage	V _{CC}	40	V
Comparator Input Voltage Range	V _{FB}	- 0.3 ~ 40	V
Switch Collector Output Voltage	V _{C(SW)}	40	V
Switch Emitter Voltage	V _{E(SW)}	40	V
Switch Collector to Emitter Voltage	V _{CE(SW)}	40	V
Driver Collector Voltage	V _{C(DRIVER)}	40	V
Driver Collector Current (note 1)	I _{C(DRIVER)}	100	mA
Output Switching Current	I _{SW}	1.5	A
Power Dissipation	DIP-8	1.0	W
	SOP-8	0.5	
Operating Ambient Temperature Range	T _{OPR}	-40 ~ +85	°C
Junction Temperature Range	T _J	0 ~ +125	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

Note: Maximum package power dissipation limits must be observed

Electrical Characteristics ($V_{CC} = 5V$, $T_a = 25^\circ C$; unless otherwise noted.)

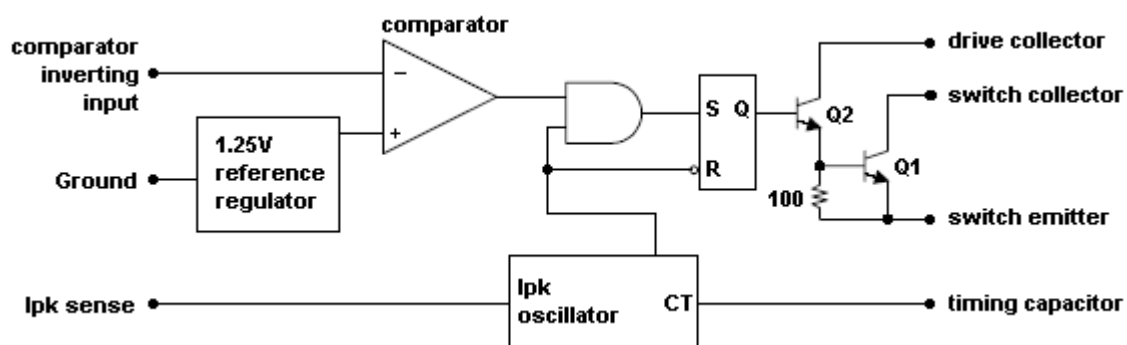
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator (OSC)						
Frequency	F_{OSC}	$C_T = 1nF$, $V_{pin5} = 0V$	24	33	42	KHz
Charge Current	I_{CHARGE}	$V_{CC} = 5V \sim 40V$	24	30	42	μA
Discharge Current	$I_{DISCHARGE}$	$V_{CC} = 5V \sim 40V$	140	200	260	μA
Discharge to Charge current ratio	$I_{DISCHARGE} / I_{CHARGE}$	Pin7 to V_{CC}	5.2	6.5	7.5	--
Current Limit Sense Voltage	$V_{IPK(SENSE)}$	$I_{DISCHARGE} = I_{CHARGE}$	250	--	350	mV
Output switch (note1)						
Saturation Voltage	$V_{CE(SAT)}$	$I_{SW} = 1A$, pin1, 8 connected	--	1.0	1.3	V
Saturation Voltage	$V_{CE(SAT)}$	$I_{SW} = 1A$, $I_d = 50mA$	--	0.45	0.7	V
DC current gain	H_{FE}	$I_{SW} = 1A$, $V_{CE} = 0.5V$	50	75	--	--
Collector off-state current	$I_{C(OFF)}$	$V_{CE} = 40V$	--	0.01	100	μA
Comparator						
Threshold Voltage	V_{REF}		1.225	1.25	1.275	V
Line regulation	REG_{LINE}	$V_{CC} = 3V \sim 40V$	--	--	6	mV
Total device						
Supply Current	I_{CC}	$V_{CC} = 5V \sim 40V$, $C_T = 1nF$, pin7= V_{CC} , pin5> V_{TH} , pin2=Gnd, remaining pins open	--	3	5	mA

Notes1: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible

Note 2: If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300mA$) and high driver currents ($\geq 30mA$), it may take up to 2 μs for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30KHz$, and is magnified at high temperature. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-darlington configuration is used, the following output drive condition is recommended: Forced Beta of output switch: $I_C \text{ output} / (I_C \text{ driver} - 7mA) \geq 10$

* The 100ohm resistor in the emitter of the driver divide requires about 7mA before the output switch conducts.

Block Diagram



Electrical Characteristics Curve

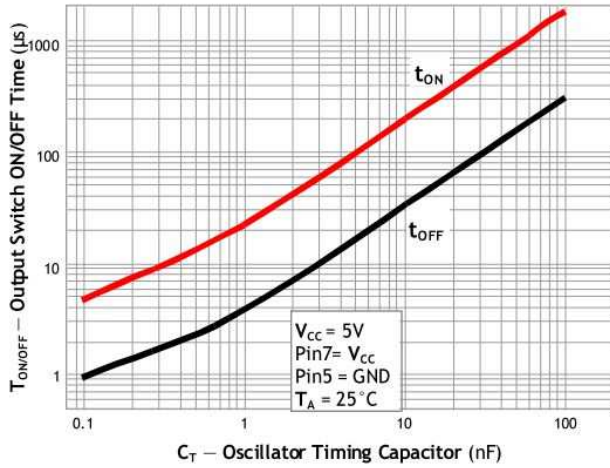


Fig 1. Output Switch ON-OFF TIME vs. Oscillator Timing Capacitor

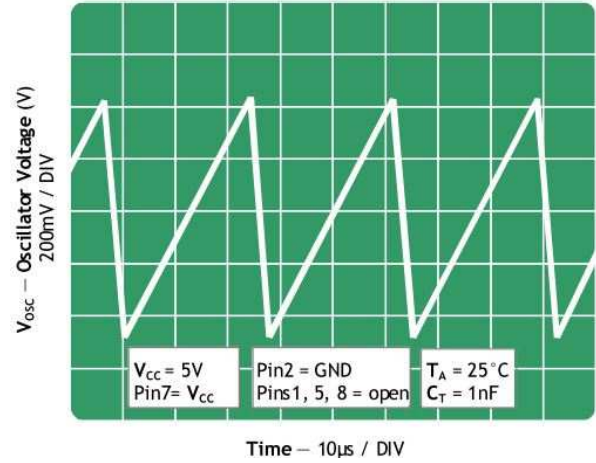


Fig 2. Timing Capacitor Wave Form

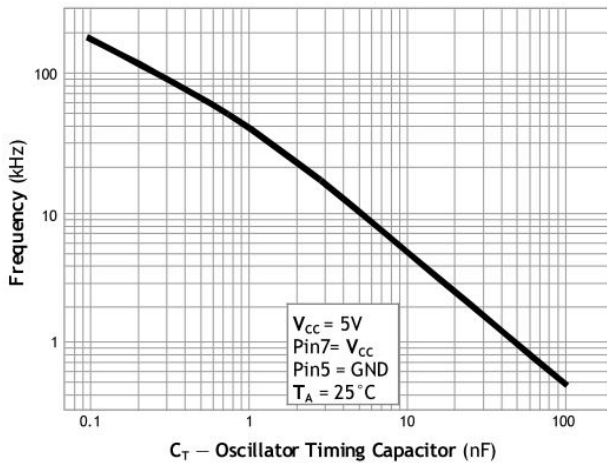


Fig 3. Oscillator Frequency vs. Timing Capacitor

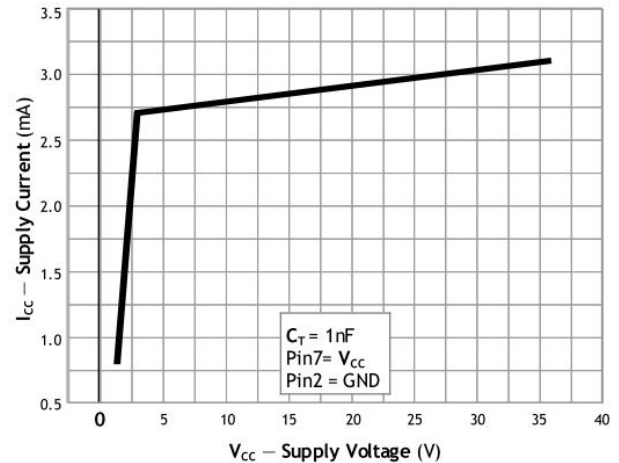


Fig 4. Standby Supply Current vs. Supply Voltage

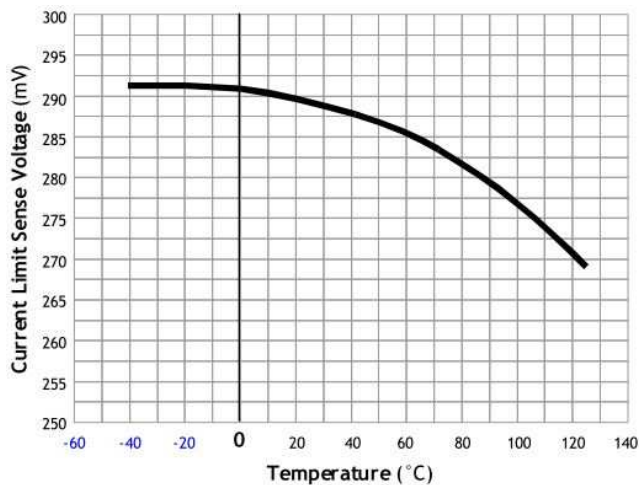
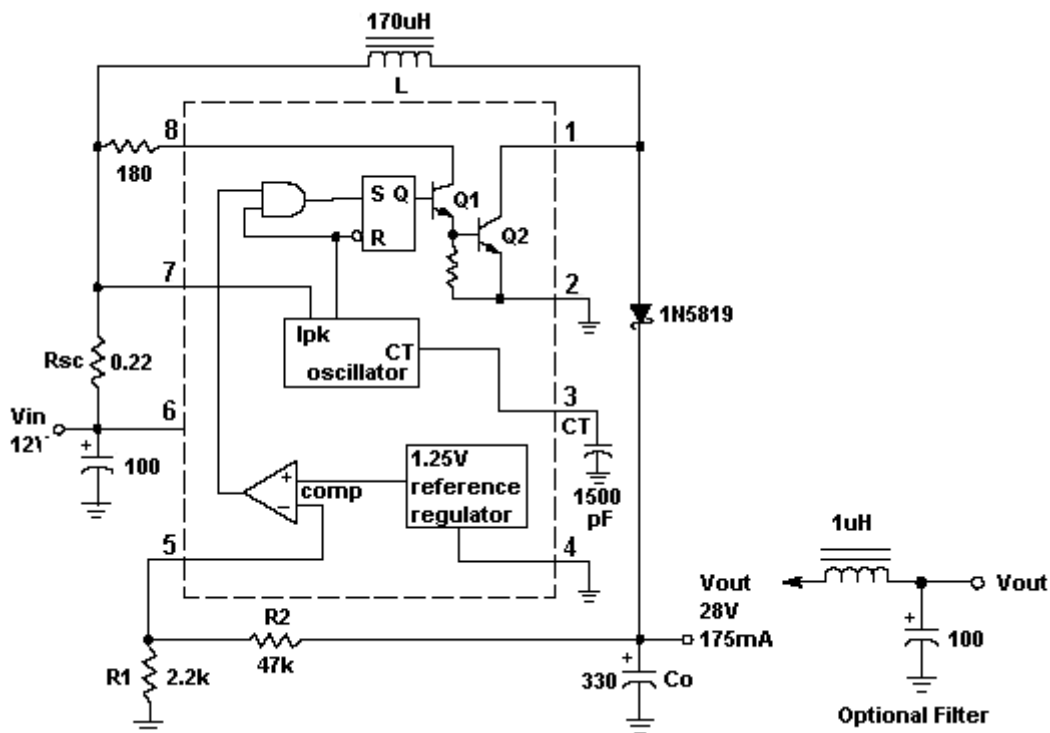


Fig 5. Current Limit Sense Voltage vs. Temperature

Typical Application Circuit



Test	Conditions	Results
Line Regulation	$V_{IN} = 8V \sim 16V$, $I_o = 175mA$	$30mV = \pm 0.05\%$
Load Regulation	$V_{IN} = 12V$, $I_o = 75mA$ to $175mA$	$10mV = \pm 0.017\%$
Output Ripple	$V_{IN} = 12V$, $I_o = 175mA$	$400mV_{pp}$
Efficiency	$V_{IN} = 12V$, $I_o = 175mA$	87.7%
Output Ripple with Optional Filter	$V_{IN} = 12V$, $I_o = 175mA$	$40mV_{pp}$

Figure 7. Step Up Converter

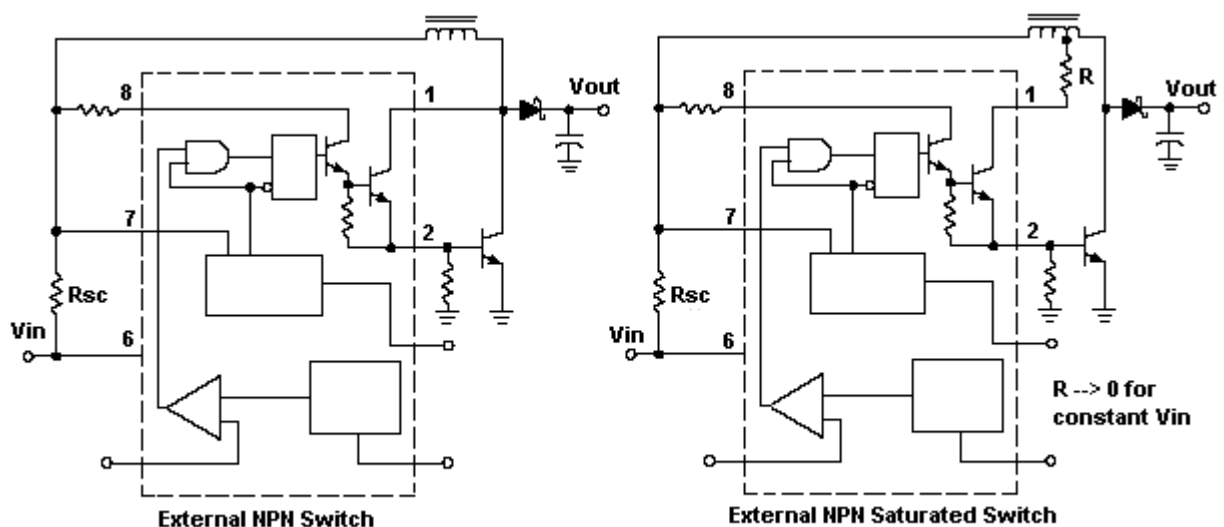
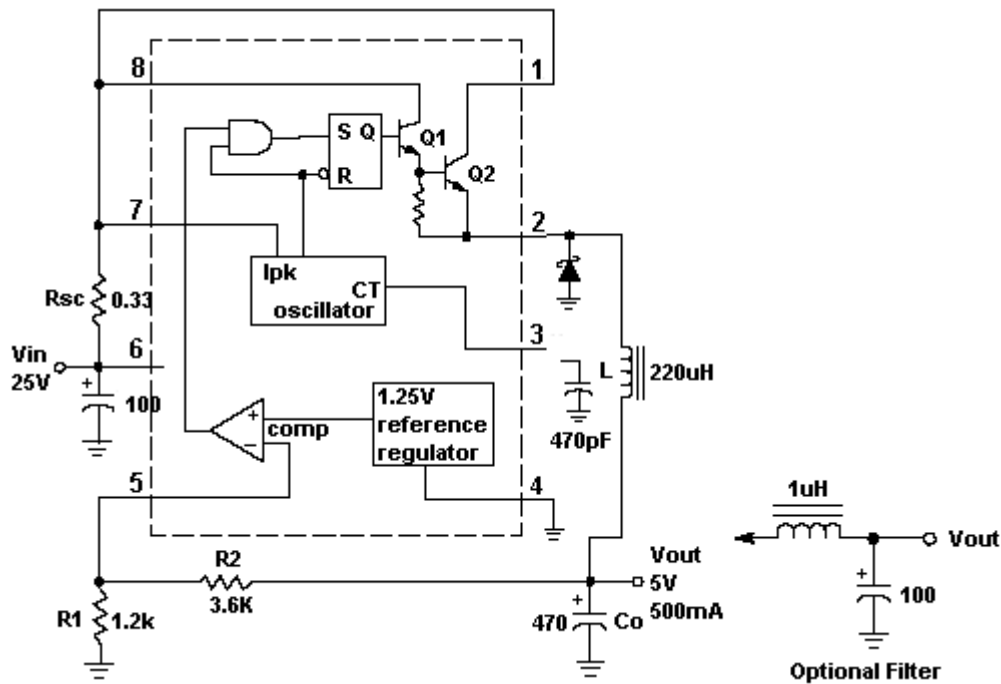


Figure 8. External Current Boost Connections for I_c Peak Greater than 1.5A

Typical Application Circuit (Continue)



Test	Conditions	Results
Line Regulation	$V_{IN} = 15V \sim 25V$, $I_o = 500mA$	$12mV = \pm 12\%$
Load Regulation	$V_{IN} = 25V$, $I_o = 50mA$ to $500mA$	$3mV = \pm 0.03\%$
Output Ripple	$V_{IN} = 25V$, $I_o = 500mA$	$120mV_{pp}$
Short Circuit Current	$V_{IN} = 25V$, $R_L = 0.1m\Omega$	$1.1A$
Efficiency	$V_{IN} = 25V$, $I_o = 500mA$	83.7%
Output Ripple with Optional Filter	$V_{IN} = 25V$, $I_o = 500mA$	$40mV_{pp}$

Figure 9. Step Down Converter

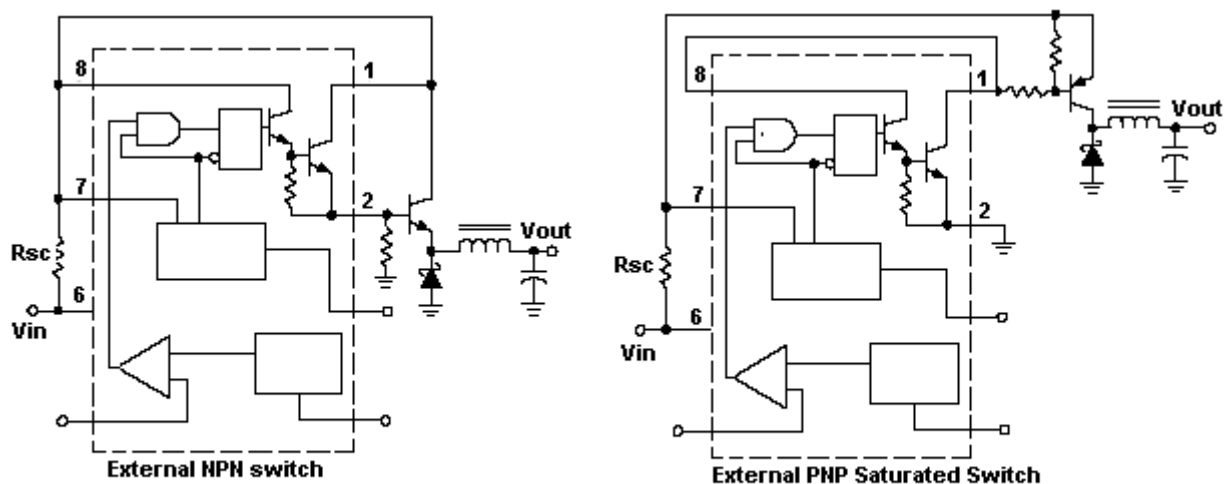
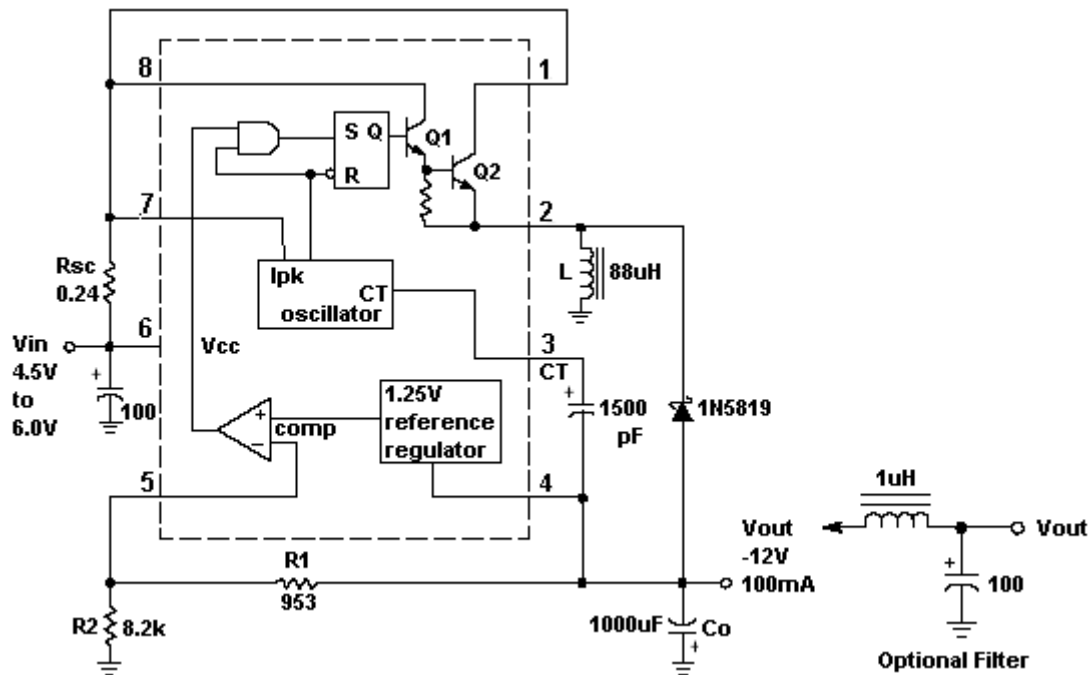


Figure 10. External Current Boost Connections for I_c Peak Greater than 1.5A

Typical Application Circuit (Continue)



Test	Conditions	Results
Line Regulation	$V_{IN} = 4.5V \sim 6V$, $I_o = 100mA$	$3mV = \pm 120.012\%$
Load Regulation	$V_{IN} = 5V$, $I_o = 10mA$ to $100mA$	$0.022V = \pm 0.09\%$
Output Ripple	$V_{IN} = 5V$, $I_o = 100mA$	$500mV_{pp}$
Short Circuit Current	$V_{IN} = 5V$, $R_L = 0.1\Omega$	$910mA$
Efficiency	$V_{IN} = 5V$, $I_o = 100mA$	62.2%
Output Ripple with Optional Filter	$V_{IN} = 5V$, $I_o = 100mA$	$70mV_{pp}$

Figure 11. Voltage Inverting Converter

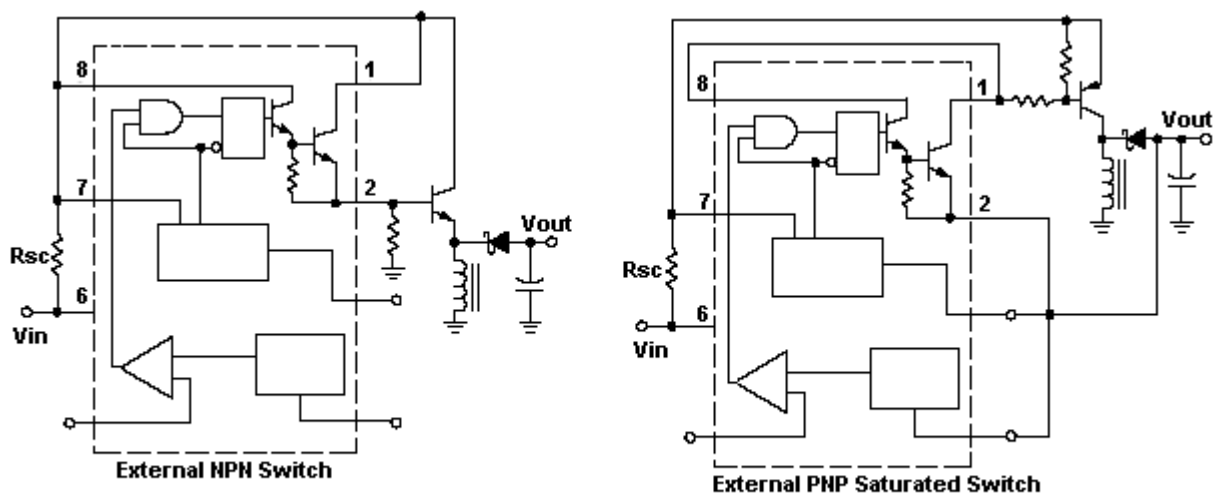


Figure 12. External Current Boost Connections for I_c Peak Greater than 1.5A

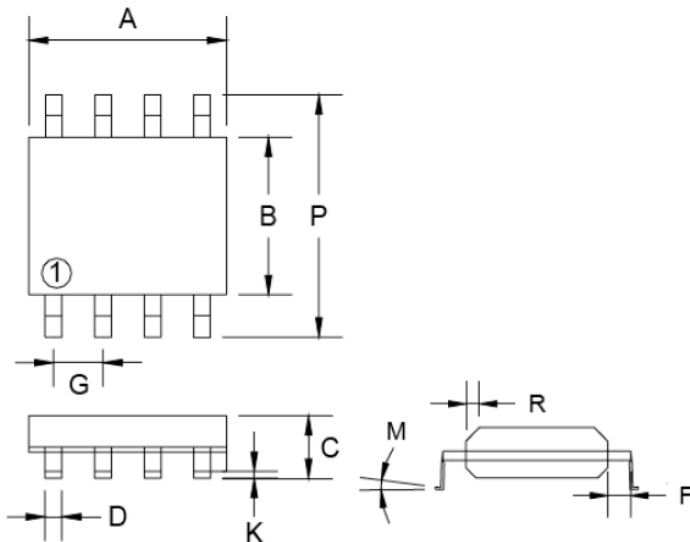
Design Formula Table

Test	Step Up	Step Down	Voltage Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_f - V_{in(min)}}{V_{cc(min)} - V_{sat}}$	$\frac{V_{out} + V_f}{V_{cc} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_f}{V_{cc} - V_{sat}}$
($t_{on} + t_{off}$)	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
CT	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk}(switch)$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$\left(\frac{0.3}{I_{pk}(switch)} \right)$	$\left(\frac{0.3}{I_{pk}(switch)} \right)$	$\left(\frac{0.3}{I_{pk}(switch)} \right)$
$L(min)$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk}(switch)} \right) * t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk}(switch)} \right) * t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk}(switch)} \right) * t_{on(max)}$
C_o	$\left(9 \frac{I_{out} * t_{on}}{V_{ripple(pp)}} \right)$	$\left(\frac{I_{pk}(switch)(t_{on} + t_{off})}{8V_{ripple(pp)}} \right)$	$\left(9 \frac{I_{out} * t_{on}}{V_{ripple(pp)}} \right)$

Terms and Definitions

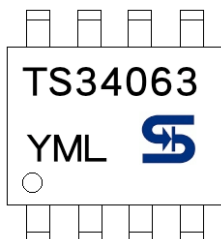
- V_{sat} = Saturation Voltage of the output switch.
- V_f = Forward Voltage drop of the rectifier.
The following power supply characteristics must be chosen:
- V_{in} = Normal input voltage
- V_{out} : Desired Output voltage, $|V_{out}| = 1.25 (1 + R_2 / R_1)$
- I_{out} : Desired output current.
- f_{min} : Minimum desired output switching frequency at the selected values for V_{in} and I_o .
- $V_{ripple(p-p)}$: Desired peak-to-peak output ripple voltage. in practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

SOP-8 Mechanical Drawing



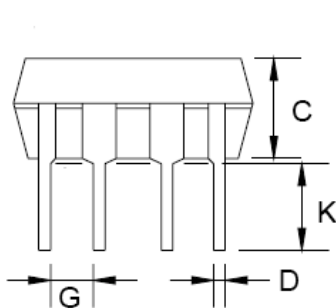
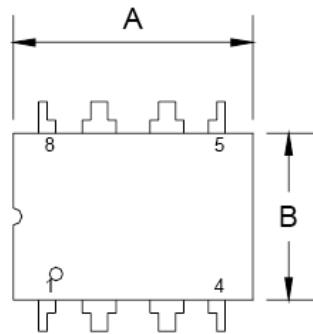
SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Marking Diagram



Y = Year Code
M = Month Code
 (A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
L = Lot Code

DIP-8 Mechanical Drawing



DIP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.45	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54 (typ)		0.10 (typ)	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10 ⁰	-	10 ⁰

Marking Diagram



Y = Year Code

M = Month Code

(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apr, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep,

J=Oct, **K**=Nov, **L**=Dec)

L = Lot Code

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