

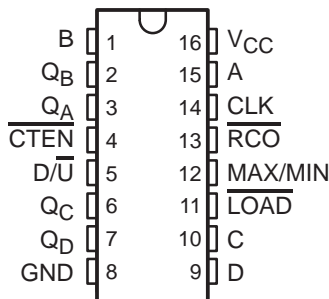
SN54HC191, SN74HC191

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

SCLS121B – DECEMBER 1982 – REVISED MAY 1997

- **Single Down/Up Count-Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presetable With Load Control**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC191 . . . J OR W PACKAGE
SN74HC191 . . . D OR N PACKAGE
(TOP VIEW)



description

The 'HC191 are 4-bit synchronous, reversible, up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

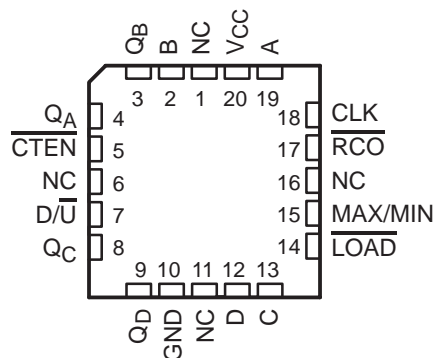
The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the count-enable ($\overline{\text{CTEN}}$) input is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up ($\text{D}/\overline{\text{U}}$) input. When $\text{D}/\overline{\text{U}}$ is low, the counter counts up, and when $\text{D}/\overline{\text{U}}$ is high, it counts down.

These counters feature a fully independent clock circuit. Change at the control ($\overline{\text{CTEN}}$ and $\text{D}/\overline{\text{U}}$) inputs that modifies the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, each of the outputs can be preset to either level by placing a low on the load ($\overline{\text{LOAD}}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of CLK. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock ($\overline{\text{RCO}}$) and maximum/minimum (MAX/MIN) count. MAX/MIN produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down, or maximum (9 or 15) counting up. $\overline{\text{RCO}}$ produces a low-level output pulse under those same conditions, but only while CLK is low. The counters can be easily cascaded by feeding $\overline{\text{RCO}}$ to $\overline{\text{CTEN}}$ of the succeeding counter if parallel clocking is used, or to CLK if parallel enabling is used. MAX/MIN can be used to accomplish look ahead for high-speed operation.

The SN54HC191 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC191 is characterized for operation from -40°C to 85°C .



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



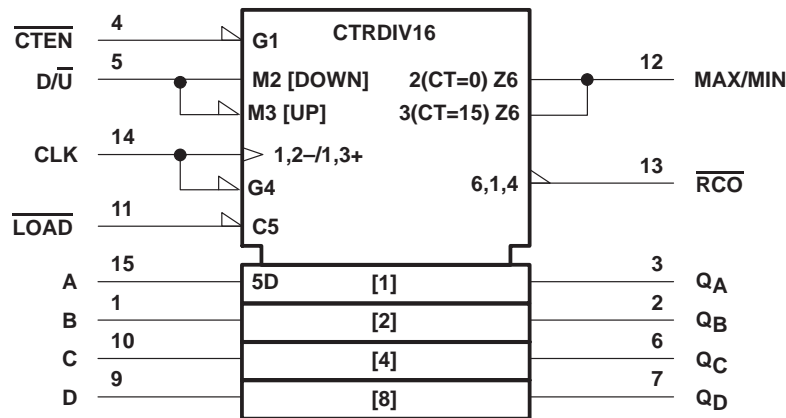
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SN54HC191, SN74HC191
4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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logic symbol†

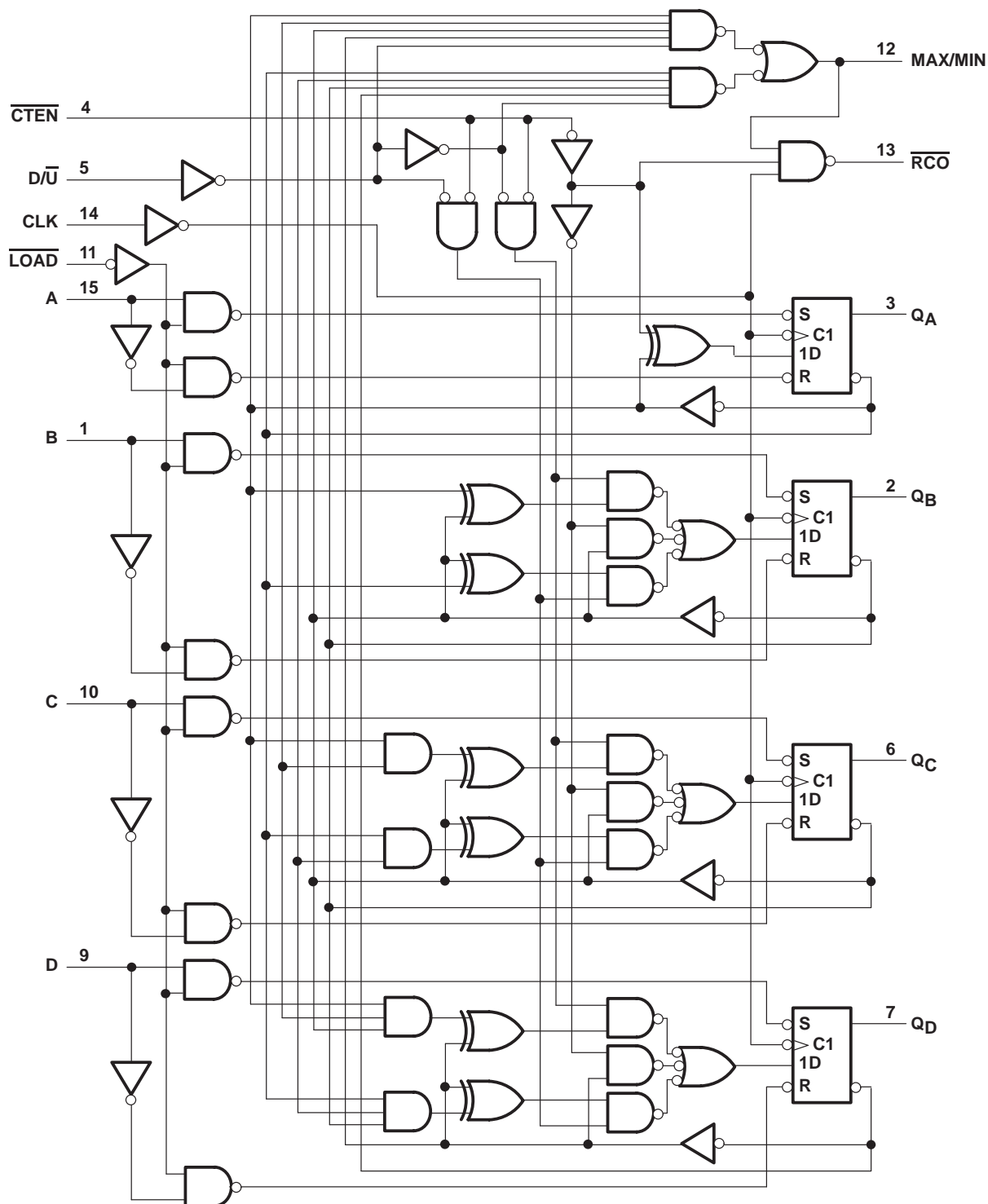


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

SN54HC191, SN74HC191 4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

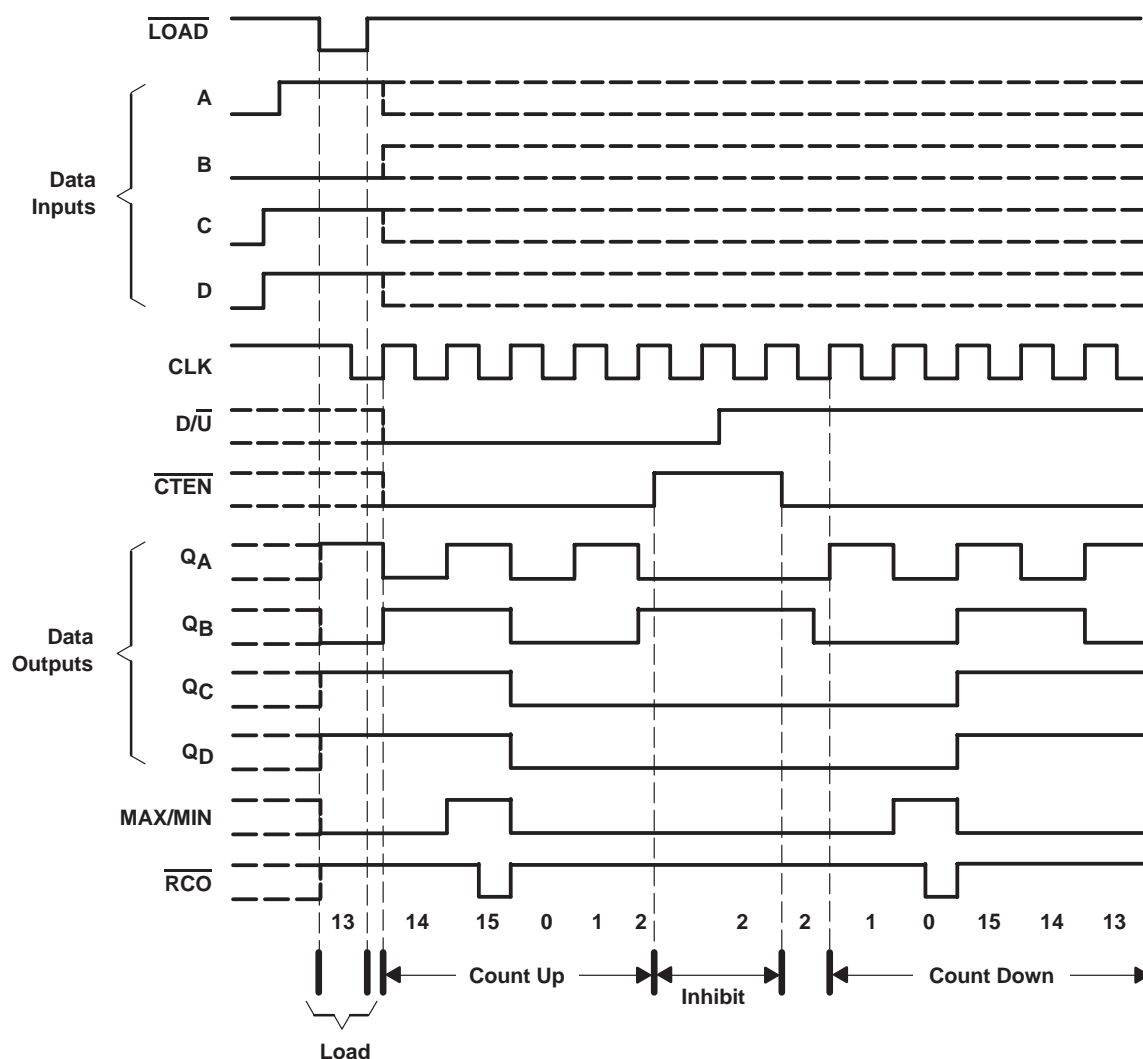
SN54HC191, SN74HC191 4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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typical load, count, and inhibit sequence

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



SN54HC191, SN74HC191

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC191			SN74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0	0.5		0	0.5		V
		$V_{CC} = 4.5$ V	0	1.35		0	1.35		
		$V_{CC} = 6$ V	0	1.8		0	1.8		
V_I	Input voltage		0	V_{CC}		0	V_{CC}		V
V_O	Output voltage		0	V_{CC}		0	V_{CC}		V
t_t^\ddagger	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000		0	1000		ns
		$V_{CC} = 4.5$ V	0	500		0	500		
		$V_{CC} = 6$ V	0	400		0	400		
T_A	Operating free-air temperature		–55	125		–40	85		°C

‡ If this device is used in the threshold region (from $V_{IL\max} = 0.5$ V to $V_{IH\min} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

SN54HC191, SN74HC191

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC191		SN74HC191		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	µA
C _i			2 V to 6 V		3	10		10		10	pF



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SN54HC191, SN74HC191

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC191		SN74HC191		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	0	4.2	0	2.8	0	3.3	MHz
		4.5 V	0	21	0	14	0	17	
		6 V	0	24	0	16	0	19	
t _w	$\overline{\text{LOAD}}$ low	2 V	120		180		150		ns
		4.5 V	24		36		30		
		6 V	21		31		26		
	CLK high or low	2 V	120		180		150		
		4.5 V	24		36		30		
		6 V	21		31		26		
t _{su}	Data before $\overline{\text{LOAD}}\uparrow$	2 V	150		230		188		ns
		4.5 V	30		46		38		
		6 V	25		38		32		
	$\overline{\text{CTEN}}$ before CLK \uparrow	2 V	205		306		255		
		4.5 V	41		61		51		
		6 V	35		53		44		
	D/ $\overline{\text{U}}$ before CLK \uparrow	2 V	205		306		255		
		4.5 V	41		61		51		
		6 V	35		53		44		
	$\overline{\text{LOAD}}$ inactive before CLK \uparrow	2 V	150		225		190		
		4.5 V	30		45		38		
		6 V	25		38		32		
t _h	Data after $\overline{\text{LOAD}}\uparrow$	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		
	$\overline{\text{CTEN}}$ after CLK \uparrow	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		
	D/ $\overline{\text{U}}$ after CLK \uparrow	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		

SN54HC191, SN74HC191

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC191		SN74HC191		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	42		14		17		
			6 V	24	48		16		19		
t_{pd}	$\overline{\text{LOAD}}$	Any Q	2 V		130	264		396		330	ns
			4.5 V		40	53		79		66	
			6 V		33	45		67		56	
	A, B, C, or D	$Q_A, Q_B, Q_C,$ or Q_D	2 V		135	240		360		300	
			4.5 V		36	48		72		60	
			6 V		30	41		61		51	
	CLK	$\overline{\text{RCO}}$	2 V		58	120		180		150	
			4.5 V		17	24		36		30	
			6 V		14	21		31		26	
		Any Q	2 V		107	192		288		240	
			4.5 V		31	38		58		48	
			6 V		26	32		49		41	
		MAX/MIN	2 V		123	252		378		315	
			4.5 V		39	50		76		63	
			6 V		32	43		65		54	
	D/ \overline{U}	$\overline{\text{RCO}}$	2 V		102	228		342		285	
			4.5 V		29	46		68		57	
			6 V		24	38		59		49	
		MAX/MIN	2 V		86	192		288		240	
			4.5 V		24	38		58		48	
			6 V		20	32		49		41	
	$\overline{\text{CTEN}}$	$\overline{\text{RCO}}$	2 V		50	132		198		165	
			4.5 V		15	26		40		33	
			6 V		13	23		34		28	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

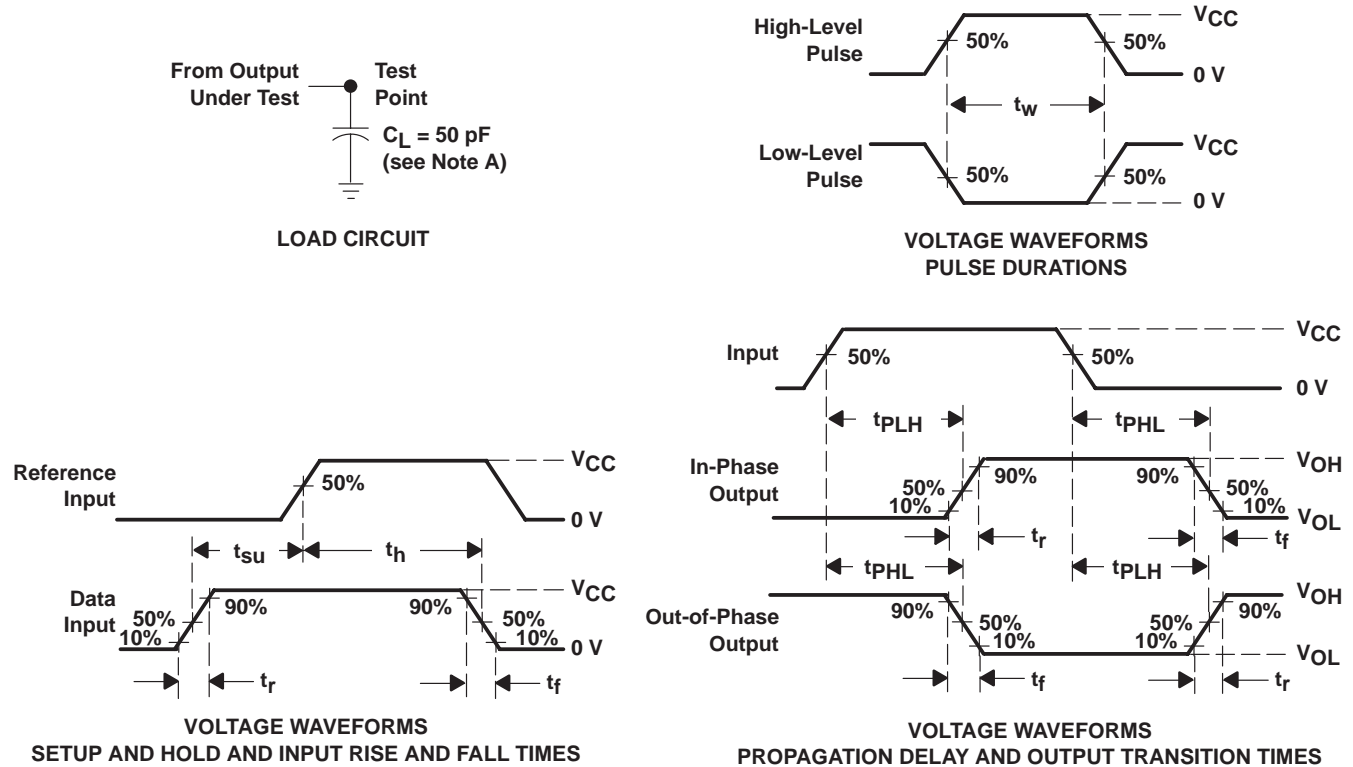
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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