EISA 9032

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Patent Pending

EISA Bus Master Interface Chip
Intel 82596 Mode

Features

- EISA Bus Master Interface Chip containing all control logic and 32 bits of address and data buffering
- BIOS PROM and Node ID PROM support
- 25 MHz or 33 MHz Clock
- Multiple local controller configuration modes (this specification describes Intel 82596 mode)
- Low power CMOS in 208 Pin Plastic QFP Package

General Description

The EISA 9032 is an EISA bus master chip which can be configured to connect with several local controllers. This specification describes the mode which supports Intel 82596CA LAN controllers. PLX also provides specifications for the other modes supported by the EISA 9032.

The 208 pin EISA 9032 is an enhanced version of the 128 pin EISA 9020BV. In addition to the bus interface logic contained in the EISA 9020BV, the EISA 9032 integrates all of the address and data buffers and other random logic.

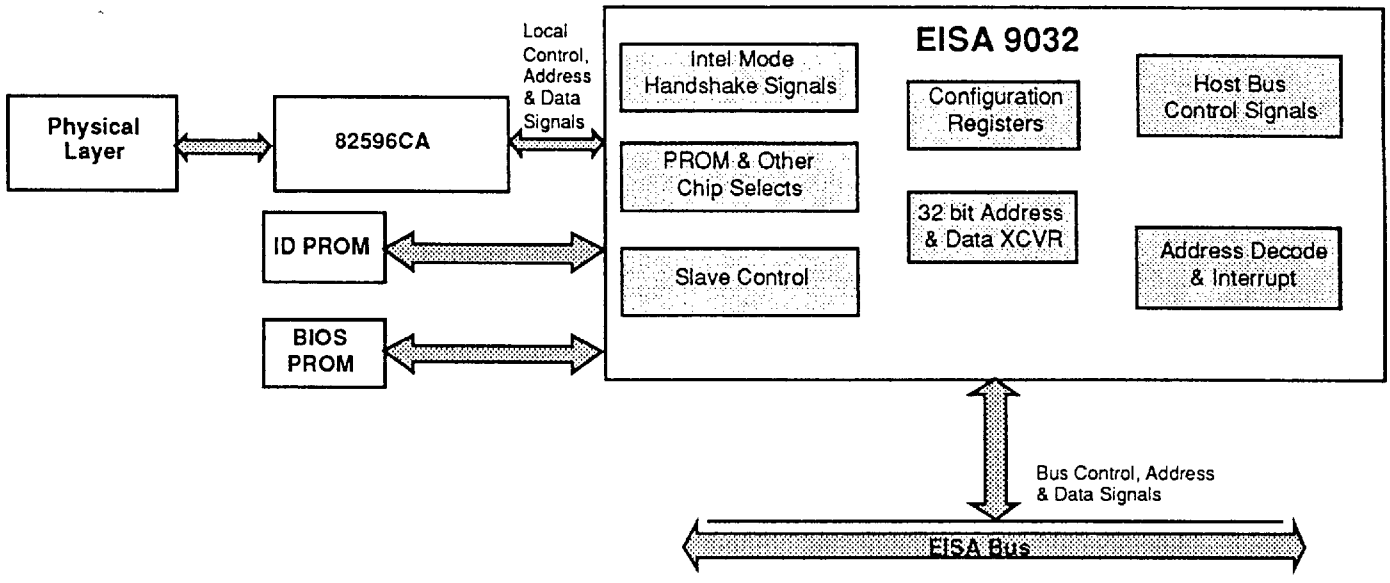

FIGURE 1. Typical Adapter Block Diagram

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SECTION 1 - INTRODUCTION

EISA 9032 GENERAL DESCRIPTION

The EISA 9032 is an EISA bus master interface chip which can be configured to connect with several local controllers. This data sheet describes only the mode which supports Intel's 82596CA Ethernet LAN controllers. The other modes supported by the EISA 9032 are described in separate data sheets which are available from PLX Technology.

EISA bus master adapters which use Intel 82596 LAN controllers and the EISA 9032 offer substantial performance advantages over slave adapters as LAN performance is significantly enhanced by the more efficient protocol processing of the 82596. The bus master implementation frees the host processor from managing bus data transfer operations, which improves overall system performance.

Using the PLX Technology 9000 series of bus master chips also reduces total hardware and software development costs for LAN adapter manufacturers designing EISA, Micro Channel and AT compatible boards. In addition to the EISA 9032 interface chip, PLX Technology provides the MCA 9020 and AT 9020, which are Micro Channel and AT bus master chips that have local interfaces similar to the EISA 9032. Therefore, by using the 9000 series, similar hardware designs and software drivers can be used for all three buses; EISA, AT and Micro Channel.

EISA 9032 FUNCTIONS

Configuration Registers

The EISA 9032 contains five internal configuration registers. These registers contain configuration data which is loaded from the host during I/O setup. Included in these registers are the interrupt request level, PREEMPT timer configuration, data size, I/O address decode bits, and PROM address decode bits. The EISA 9032 also provides four external user bits for application specific configuration information.

The EISA card ID information is supplied externally to the EISA 9032 and is contained in the Node ID PROM.

Specific EISA 9032 functions

EISA 9032 major functions include:

1. **Master Control Signal Protocol Converter.** The EISA 9032 converts all handshakes of the local controller to EISA signals.
2. **Slave controller.** The EISA 9032 includes an EISA slave interface for control of adapter board slave devices.
3. **Address decoder.** The EISA 9032 decodes host address bits LA23-LA13, and LA11-LA2. The EISA 9032 decodes these addresses to generate chip selects and access configuration registers.
4. **Interrupt generator.** The EISA 9032 can generate one of four host interrupts from one local interrupt, programmable through configuration registers.
5. **Address & Data Buffers.** The EISA 9032 incorporates 32 bit address and 32 bit data buffers.
6. **Clock.** The EISA 9032 runs from crystal or TTL oscillator and generates a 25 MHz or 33 MHz clock for external and internal use.
7. **User programmable configuration bits.** The EISA 9032 provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** All control, data & address signals generated by the EISA 9032 drive the EISA bus directly, without requiring external drivers.
9. **PREEMPT Timer.** Through the configuration registers the user may program a maximum time, 55 BCLKs or 23 BCLKs, which the adapter may hold the bus.
10. **Adapter ID mapping.** The adapter ID number is mapped into I/O space to allow the option to implement the adapter ID in an ID PROM.

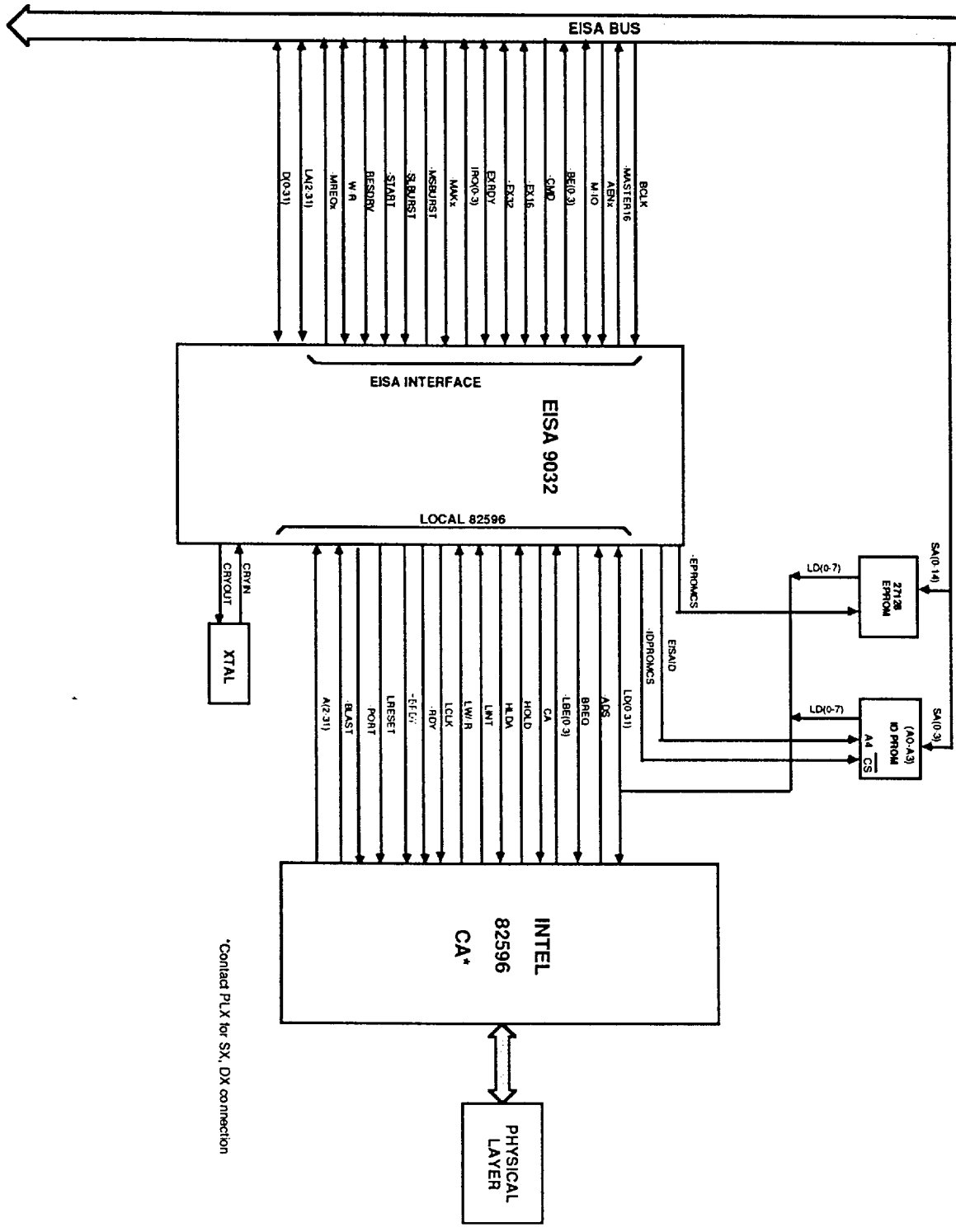


Figure 2. Low Cost EISA Direct Bus Master

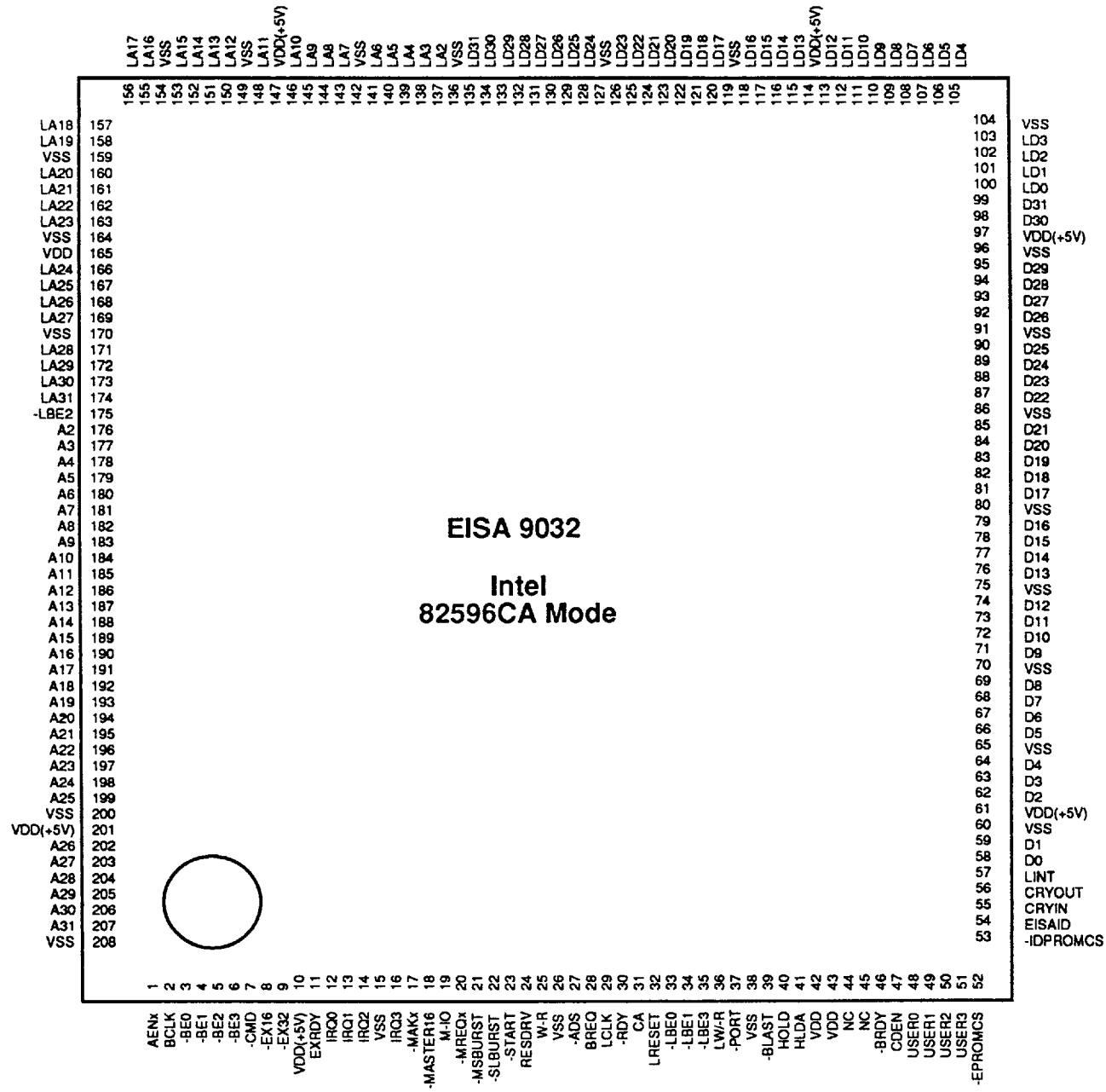


Figure 3.
Pin Out

SECTION 2 - CONFIGURATION REGISTERS AND ADDRESS DECODING

The EISA 9032 decodes the EISA Address signals to select the -PORT and CA signals, the Node ID PROM (which contains the EISA Board ID), the BIOS PROM and the EISA 9032's five internal configuration registers. These five registers provide essential configuration information to the EISA 9032 and the Ethernet adapter board. They are loaded at power-up and may be accessed dynamically through I/O slave cycles.

The -PORT, CA, Node ID PROM and four of the five configuration registers may be accessed through an ISA I/O address as well as an EISA slot specific address. The EISA 9032 offers the option of using ISA addressing to simplify converting software drivers written for AT boards to EISA board drivers. For boards with software drivers which use EISA slot specific addressing, the AT addressing mode is not required.

ADDRESS DECODING

In accordance with the EISA specification, "z" refers to the slot number.

-PORT and CA Address These signals may be activated on either a slot specific basis or through an ISA decode procedure. Bit 4 in Configuration Register 1 enables the ISA addressing mode.

If slot specific decode mode is selected (Bit4 of REGISTER 1 = 0) then:

CA is selected by Address 0z000h-0z007h

-PORT is selected by Address 0z008h-0z00fh

If the ISA address mode is selected (Bit 4 of Register 1 = 1) then:

-PORT and CA are selected by the ISA Address indicated in Register 1, Bits 5-7

EISA ID and Node ID PROM Address Both the EISA ID and the Ethernet Address reside in the same ID PROM. The four byte EISA ID and the Node ID PROM are selected through the EISA ID, -IDPROMCS, LA(2-11) and SA(0-3) signals as follows:

EISA Address (LA 2-11)	-IDPROMCS (Pin 53)	EISA ID (Pin 54)	System Address (SA3-0)	
0zC80h-83h	Active(0)	Active(1)	0h	EISA ID, First Byte
	Active(0)	Active(1)	1h	EISA ID, Second Byte
	Active(0)	Active(1)	2h	EISA ID, Third Byte
	Active(0)	Active(1)	3h	EISA ID, Fourth Byte
0zC90h-97h	Active(0)	Inactive(0)	0-5h	6 Ethernet ID Bytes
	Active(0)	Inactive(0)	6-7h	Spare PROM Bytes

Note: The EISA ID pin of the EISA 9032 and -IDPROMCS signals are decoded from the EISA address signals. The EISA ID pin of the EISA 9032 should be connected to the PROM address pin A4. The System Address (SA) signals are connected to the ID PROM as shown in figure 2. A typical PROM address map is as follows:

PROM Address A4-A0 (EISA ID pin plus SA3-0)	Data
00 - 05h	6 Ethernet ID Bytes
06 - 07h	Spare PROM Bytes
08 - 0Fh	Not used
10h	EISA ID, First Byte
11h	EISA ID, Second Byte
12h	EISA ID, Third Byte
13h	EISA ID, Fourth Byte
14 - 1Fh	Not used

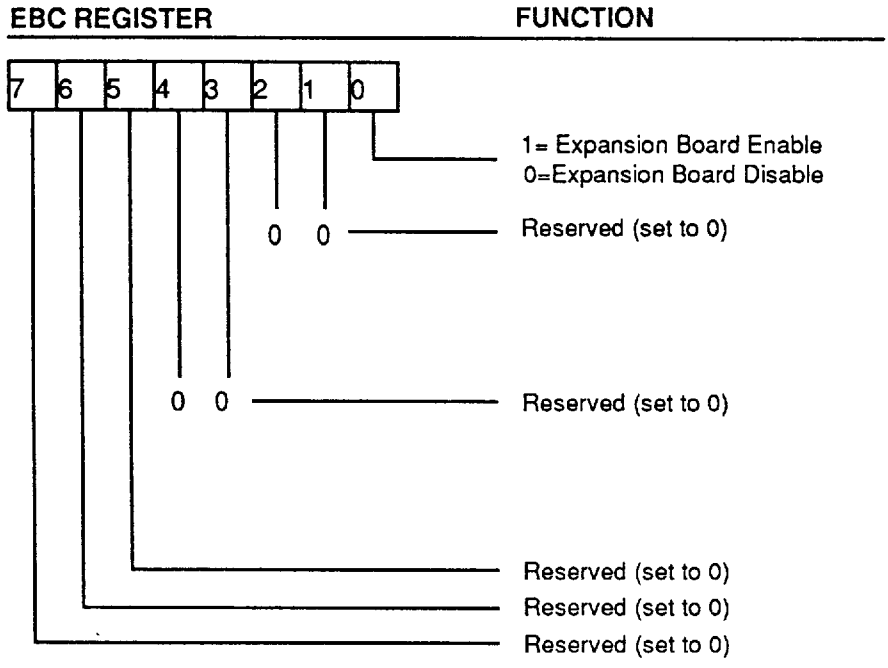
-EPROMCS Address This BIOS PROM chip select is decoded from address bits LA(13-23). The LA(13-16) bits are programmable in Configuration Register 2, Bits 2-5.

Configuration Register Address The five configuration registers reside in the EISA configuration space at 0zC8Xh where "z" is the slot number and "X" is the register address. The individual register slot specific addresses are listed in the heading of the register descriptions which follow.

For the EISA address of the configuration registers, see the table in Register 1.

CONFIGURATION REGISTERS

EBC Register- Expansion Board Control Bits Register; at 0zC84h



Bit 0 - Enables Expansion Board

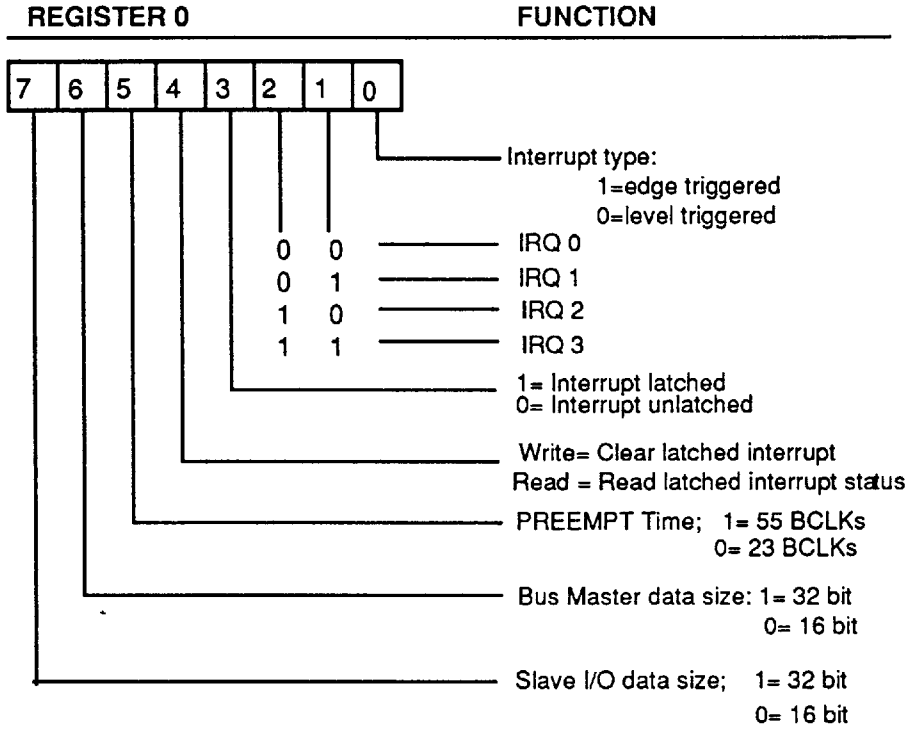
Bit 1-7 - Reserved

All register bits default to 0.

Register 0 ; at 0zC88h

This register contains configuration data that is written by the host during I/O set-up.

WRITE / READ



Bit 0 - Interrupt types: This bit defines whether the IRQ0-IRQ3 are level sensed or edge triggered.

Bit 0= 1, edge triggered

Bit 0= 0, level triggered (default)

Bit 1,2 - These bits select which EISA interrupt level is used when the 82596 asserts its interrupt request line.

Bit 3 - This bit specifies whether the interrupt is latched or unlatched; 1= latched mode. 0= unlatched mode (default)

Bit 4 - The user can write a 1 to this bit to clear the latch mode interrupt or read this bit for latched interrupt status (1 is interrupt present, 0 is no interrupt present).

Bit 5 - This bit specifies the amount of time the EISA 9032 may hold the bus after a PREEMPT condition. When this bit is set to 1, the EISA 9032 allows the 82596 to hold the bus 55 BCLKs after PREEMPT. At this point, the EISA 9032 removes HLDA to the 82596 which allows the 82596 nine BCLKs to release the bus. When this bit is set to 0, the EISA 9032 holds the bus for 23 BCLKs after PREEMPT before removing HLDA.

Bit 6 - This bit specifies the data width for bus master transfers. If the specific 82596 chip used supports 32 bit transfers, then this bit selects between a 32 bit or 16 bit bus master interface. If this bit is set to 1, the bus master data size is 32 bits. If set to zero, the bus master data size is 16 bits.

Bit 7 - This bit specifies the data width for slave access to the 82596. This bit is dependent on the 82596 and I/O board. When set to 1, the slave I/O data size is 32 bits. When set to 0, the data size is 16 bits. The 82596CA should be set to 32 bits. The 82596SX and DX should be set to 16 bits.

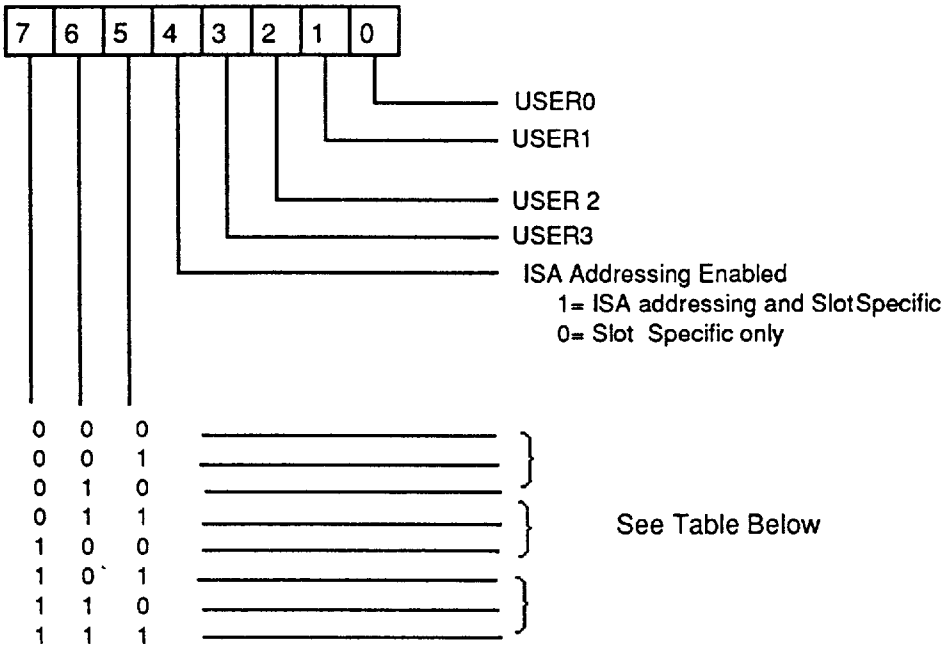
All register bits default to 0.

Register 1 ; at I/O address 0zC89h

This register is loaded at power-up during I/O board configuration. It is used to control external logic through bits 0-3. Register 1 also contains the ISA alias I/O address decode range to select the I/O address of the board in the ISA mode.

WRITE / READ

REGISTER 1 **FUNCTION**



BITS 7	6	5	Base Range	CA	-PORT	EBC Register	Reg 0	Reg 1	Reg 2	Reg 3	Node ID	EISA ID
0	0	0	100-11F	110-117	118-11F	Not Accessible	108	109	10A	10F	100-105	Not Accessible
0	0	1	120-13F	130-137	138-13F	"	128	129	12A	12F	120-125	"
0	1	0	140-15F	150-157	158-15F	"	148	149	14A	14F	140-145	"
0	1	1	160-17F	170-177	178-17F	"	168	169	16A	16F	160-165	"
1	0	0	300-31F	310-317	318-31F	"	308	309	30A	30F	300-305	"
1	0	1	320-33F	330-337	338-33F	"	328	329	32A	32F	320-325	"
1	1	0	340-35F	350-357	358-35F	"	348	349	34A	34F	340-345	"
1	1	1	DISABLED	-	-	-	-	-	-	-	-	-

Bits 0-3 - These bits connect directly to the USER_PINs and allow Configuration Register control of external logic.

Bits 5-7 - These bits select the I/O address of the board in ISA mode.

All register bits default to 0.

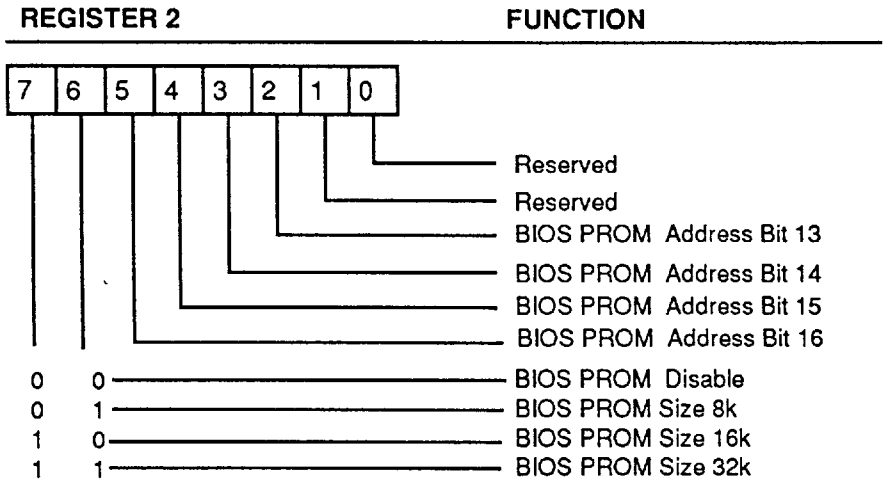
Register 2; at I/O address 0zC8Ah

This register selects the BIOS PROM address range and the BIOS PROM size. The BIOS PROM starting address and size is placed in this register during card configuration. For BIOS PROM selection, address bits LA23-LA13 are specified below:

LA23	LA22	LA21	LA20	LA19	LA18	LA17	LA16	LA15	LA14	LA13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

The EISA 9032 decodes the above value for LA23-LA17 and matches LA16-LA13 with bits 2-5. -EPROMCS will asserted upon a valid decode and match of LA23-LA13.

WRITE / READ



Bits 0-1 - Reserved

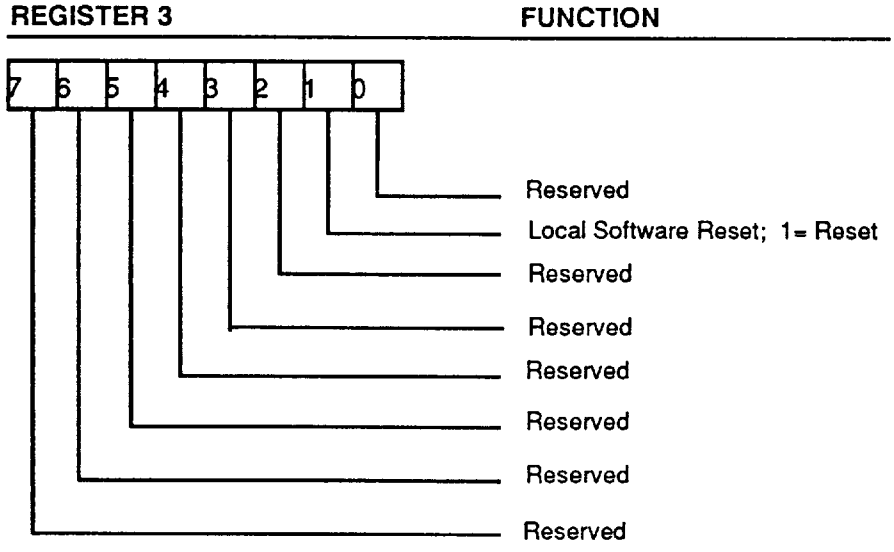
Bits 2-5 - These bits are compared against host addresses LA16-LA13 for determining a BIOS PROM access.

Bits 6-7 - These bits specify the BIOS PROM size as indicated above.

All register bits default to 0.

Register 3; at I/O address 0zC8Fh

This register enables EISA bus bursting and software RESET operation. It is loaded at power-up during board configuration.



Bit 0 - Reserved

Bit 1 - When this bit is set to 1, it allows the system to RESET the EISA 9032 by software. The contents of the EISA 9032's registers will **not** be RESET. The default condition is 0.

Bit 2-7 - Reserved

All register bits default to 0.

SECTION 3 - PIN SUMMARY

Pin Summary

Table 3.1 gives a summary of the host bus pins for the EISA 9032 device. The Host Interface consists of the pins for the EISA bus. Table 3.2 gives a summary of the local interface pins. The Local interface consists of the pins for the 82596 interface. The following abbreviations are used:

I/O - Input and Output Pin
I - Input Pin Only
O - Output Pin Only
TS - Three-state Pin
OC - Open Collector Pin
TP - Totem Pole Pin

Table 3.1 Host Interface - EISA Bus Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
AENx	1	I	-	-
BCLK	1	I	-	-
-BE(0-3)	4	I/O	TS	24
-CMD	1	I	-	-
-EX16	1	I/O	OC	24
-EX32	1	I/O	OC	24
EXRDY	1	I/O	OC	24
IRQ(0-3)	4	O	OC/TP*	6
-MAKx	1	I	-	-
-MASTER16	1	O	OC	24
M-IO	1	I/O	TS	24
-MREQx	1	O	TP	6
-MSBURST	1	O	TS	24
-SLBURST	1	I	-	-
-START	1	I/O	TS	24
RESDRV	1	I	-	-
W-R	1	I/O	TS	24
TOTAL PINS	**23**			

* OC in level triggered mode, TP in edge triggered mode.

Table 3.2. Local Bus Pin Summary for Intel 82596

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
-ADS	1	I	-	-
-BLAST	1	I	-	-
-BRDY	1	O	TP	4
BREQ	1	O	TP	4
CA	1	O	TP	4
CDEN	1	O	TP	4
CRYIN	1	I	-	-
CRYOUT	1	O	-	-
EISAID	1	O	TP	4
HOLD	1	I	-	-
HLDA	1	O	TP	4
-LBE(0-3)	4	I	-	-
LCLK	1	O	TP	4
LINT	1	I	-	-
LRESET	1	O	TP	4
LW/-R	1	I	-	-
-PORT	1	O	TP	4
-EPROMCS	1	O	TP	4
-IDPROMCS	1	O	TP	4
-RDY	1	O	TP	4
USER(0-3)	4	O	TP	4
TOTAL PINS	**27**			

Table 3.3 Buffer Control, Address and Data Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
LD (0-31)	32	I/O	TS	4
D (0-31)	32	I/O	TS	24
LA (2-31)	30	I/O	TS	24
A (2-31)	30	I	-	-
TOTAL PINS	**124**			

Table 3.4 Power, Ground and No Connect Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
NC	2	-	-	-
VDD	9	I	-	-
VSS	23	I	-	-
TOTAL PINS	**34**			

Table 3.5 Host Interface- EISA Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
AENx	Address Enable	I	1	This active high slot specific input signal indicates (when deasserted) that the EISA 9032 may respond to address and I/O commands.
BCLK	Bus Clock	I	2	This active high input is provided for synchronizing EISA bus events with the host system clock. BCLK operates at a frequency between 8.333 and 6 MHz with a duty cycle of 50 percent.
-BE(3) -BE(2) -BE(1) -BE(0)	Byte Enables	I/O	6 5 4 3	These active low I/O signals are the byte enables that identify the specific bytes addressed in a double word. These signals and the address lines LA(2-23), are pipelined from one cycle to the next -BE(3) enables the high byte (byte 3) of a double word while -BE(0) enables the low byte. During Slave cycles, BE(0-3) are used to generate address bits 0 and 1.
-CMD	Command Strobe	I	7	This active low input signal provides timing control within the EISA bus cycle. The system board asserts this signal on the rising edge of BCLK, simultaneous with the deassertion of the -START signal.
-EX16	16 Bit Slave	I/O	8	This active low I/O signal indicates an EISA memory or I/O slave is capable of transferring 16 bits of data.
-EX32	32 Bit Slave	I/O	9	This active low I/O signal indicates an EISA memory or I/O slave is capable of transferring 32 bit double word size. During 32 bit bus master transfers the EISA 9032 samples -EX32 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the EISA 9032 floats the -BE(0-3) and -START lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the EISA 9032 completes the cycle.
EXRDY	EISA Channel Ready Input and Output	I/O	11	This active high open collector signal lengthens a bus cycle from its standard one BCLK time. It is asserted by a memory or I/O device when it can not respond quickly enough. When EXRDY is low the EISA 9032 inserts wait cycles (one BCLK) until memory brings this signal high. The EISA 9032 pulls EXRDY low during slave cycles.
IRQ(3) IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	I/O	16 14 13 12	These signals are used to inform the system of the completion of a task. IRQ(0-3) selection is programmable in the configuration registers. They may be programmed to active high totem pole or active low open collector.

-MAKx	Master Acknowledge	I	17	This active low slot specific signal is asserted by the system board to grant access to the EISA bus. The signal is in response to the EISA 9032 asserting the -MREQx signal. The EISA 9032 must release the EISA bus within 7.68 usec after this signal is deasserted.
-MASTER16	16 Bit Bus Master	O	18	When this three-state output signal is asserted the EISA 9032 is a 16 bit bus master. This pin is programmable in the configuration registers.
M-IO	Memory or I/O	I/O	19	This three-state signal distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M-IO is low an I/O cycle is in progress.M-IO is pipelined from one EISA bus cycle to the next.
-MREQx	Master Request	O	20	This active low totem pole, slot specific, output signal is asserted by the EISA 9032 to request EISA bus access. The system board asserts -MAKx in response to this signal.
-MSBURST	Master Burst	O	21	The EISA 9032 asserts this active low output signal to indicate to the slave that it is executing burst cycles.
-SLBURST	Slave Burst	I	22	This active low input informs the EISA 9032 that the addressed slave supports burst cycles.
-START	Start Command	I/O	23	This active low three-state signal indicates the beginning of an EISA bus access. It is asserted for one BCLK period after the address is valid on the bus.
RESDRV	Bus Reset	I	24	This active high input signal provides a hard reset to the EISA 9032 chip. Internal logic is initialized by this signal and any transfer operations are aborted.
W-R	Write/Read	I/O	25	This Three-state pin indicates whether to perform an EISA bus write or read operation. When this pin is high a write operation is requested and when low a read.

Table 3.6 Local Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
-ADS	Address Strobe	I	27	This active low input signal indicates the Intel 82596 has begun a valid bus master cycle and that the 82596 pins A31-A2, -BE(0-3) and W/-R are being driven valid.
-BLAST	Last Burst Cycle	I	39	This pin connects to 82596 -BLAST pin.
-BRDY	Burst Ready	O	46	This pin connects to 82596 -BRDY pin.
BREQ	Bus Request	O	28	Bus Request to 82596. This signal is used to trigger the bus throttle timers.

CA	Channel Attention	O	31	This active high output is used to force the 82596 to begin executing memory resident commands. In other words, this signal wakes up the Intel 82596 and forces it to start executing command sequences from system memory. See Section 2 for the I/O address range.
CDEN	Card Enable	O	47	This totem pole output is asserted when the I/O board has been enabled through the EBC Register.
LCLK		O	29	This output signal provides the fundamental clocking for the 82596. The 82596CA clock input maybe connected driectly to this pin. The DX and SX should be connected through a divide by two flip-flop.
CRYIN	Crystal Input	I	55	This input pin provides the timing for all synchronous operations in the EISA 9032. It connects to either a TTL clock signal or directly to a crystal.
CRYOUT	Crystal Output	O	56	This output signal connects directly to crystal oscillator.It is a no connect pin when the the CRYIN pin connects to a TTL clock signal.
EISAID	EISA ID address bit		54	This address bit (comparable to ID PROM A4) is active during EISA product ID accesses. This signal is active when LA(2,3,4) = (0,0,0)
HOLD	Bus Hold Request	I	40	This active high input indicates the Intel 82596 needs to gain access to the host bus.
HLDA	Bus Hold Acknowledge	O	41	This active high totem pole output signal indicates the EISA 9032 has successfully gained access to the host bus. When the Intel 82596 receives this signal it begins bus master operation.
-LBE 3 -LBE 2 -LBE 1 -LBE 0	Byte Enable	I	35,175,34, 33	These active low input signals are used to indicate which bytes are involved with the current bus master memory access. -LBE(3) specifies the high byte and -LBE(0) specifies the low byte. When operating in 16 bit mode, these pins are redefined to carry the -BHE and -BLE signals into -LBE1 and -LBE0.
LINT	82596 Local Interrupt	I	57	This active high input is asserted when the 82596 has an interrupt pending. The EISA 9032 asserts one of four host interrupts when this signal is active. The host interrupt line that is asserted is programmable in Configuration Register 0, bits 1 and 2.
LRESET	Reset	O	32	This active high output signal provides a hard reset to the Intel 82596. It is also used to phase synchronize the clock for the EISA 9032 and Intel 82596.
LW/-R	Write or Read	I	36	This input pin specifies whether the current bus master access is a read or write operation. When this pin is high a write cycle is requested and when low a read cycle.

-PORT	Port	O	37	This active low output signal causes the Intel 82596 to latch data from the system data bus into a 32 bit internal register. When operating in 16 bit mode, this signal is activated twice for all CPU port access commands. This signal and the CA signal comprise the slave interface to the Intel 82596. The I/O address of the -PORT signal is programmable in configuration registers.
-EPROMCS	BIOS PROM Output Enable	O	52	This active low output pin connects to the output enable pin (-OE) of the BIOS Boot PROM. The EISA 9032 gates the data from the PROM onto the system data bus. The system memory address of the BIOS PROM is programmable in Configuration Register 2.
-IDPROMCS	ID PROM Output Enable	O	53	This active low output pin connects to the output enable pin (-OE) of the Node ID PROM. The EISA 9032 gates the data from the Node ID PROM onto the system data bus. The system I/O address of the ID PROM is programmable in Configuration Register 1.
-RDY	Ready	O	30	The EISA 9032 asserts this active low signal to inform the Intel 82596 that the current bus master access cycle may be completed. When this signal is high, the Intel 82596 inserts wait cycles in the current bus access.
USER3 USER2 USER1 USER0	User Defined Pins	O	51, 50, 49, 48	These totem pole output pins are controlled from Configuration Register 1 for each host interface. They control logic on the I/O board.

Table 3.7 Address and Data Pins

Symbol	Signal Name	I/O	Pin Number	Function
A(2-31)	Local Address	I	176-199, 202-207	These input signals connect directly to the 82596 address pins.
D(0-31)	EISA bus Data	I/O	58,59, 62-64, 66-69, 71-74, 76-79, 81-85, 87-90, 92-95, 98,99	These I/O signals connect directly to the EISA bus.

LA(2-31)	EISA bus Address	I/O	137-141, 143-146, 148, 150-153, 155-158, 160-163, 166-169, 171-174	These I/O signals connect directly to the EISA bus.
LD(0-31)	Local Data	I/O	100-103, 105-113, 115-118, 120-126, 128-135	These I/O signals connect directly to the 82596, the Mode ID PROM and the BIOS PROM.

Table 3.8 Power and Ground Pin Description

NC	No Connect	-	44, 45	No Connect
VDD	Power	I	10, 42, 43, 61, 97, 114, 147, 165, 201	Five Volt Power Supply Pins
VSS	Ground	I	15, 26, 38, 60, 65, 70, 75, 80, 86 , 91, 96, 104, 119, 127, 136, 142, 149, 154, 159, 164, 170, 200, 208	Ground Pins

SECTION 4 - BUS CYCLE DESCRIPTION

This section describes EISA 9032 local and EISA bus functionality with the 82596.

SLAVE CYCLES

In the slave mode, the EISA 9032 monitors the address lines LA (11:2) and -BE (3:0) for general I/O address decoding, slot-specific address decoding, and configuration register accessing. During the slave mode, -AENx has to be asserted low.

The configuration registers can be accessed through 8-bit I/O read or write cycles. These cycles are 6 BCLK periods long.

82596 Register Access

The 82596 registers are accessed through EISA slave I/O cycles. The EISA 9032 decodes the system address and drives CA or -PORT to the 82596. The EISA 9032 also drives the data direction signal, HDIR, to the data buffers to indicate whether the cycle is a read or a write.

-PORT is valid for addresses 0z0X0h-0z0X7h. CA is valid for addresses 0z0X8h - 0z0XFh.

EISA ID, Node ID and BIOS PROM Access

The EISA ID and Ethernet ID use the same ID PROM. The EISAID and -IDPROMCS signals are accessed through 8-bit I/O slave cycles. The EISAID signal should connect to the on board PROM address A4. The EISA 9032 decodes the system address and drives the -EPROMCS for BIOS PROM access.

EISA ID, Node ID and BIOSPROM accesses are executed by the EISA 9032 as 8 bit EISA slave cycles. EXRDY is not deasserted. The -IDPROMCS is valid for addresses 0zC80h-0zC83h, and 0zC90h-0zC97h.

Interrupts

The EISA 9032 provides four interrupt request lines, IRQ(3:0). LINT from the 82596 asserts the appropriate EISA interrupt request signals. If the EISA interrupt request line is programmed in the latched mode, reading bit 4 of register 0 will clear the interrupt request signal.

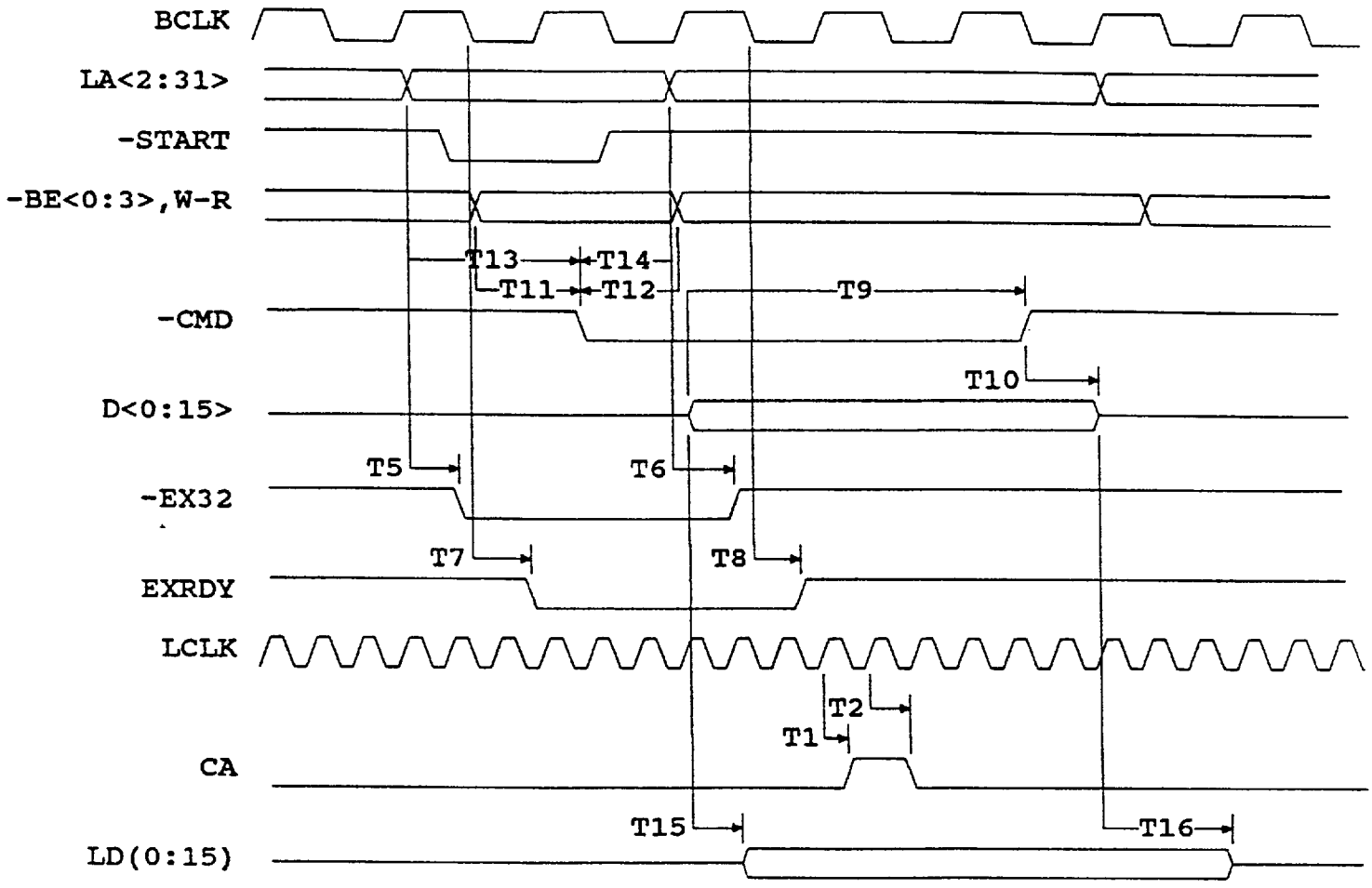
MASTER CYCLES

Bus Request

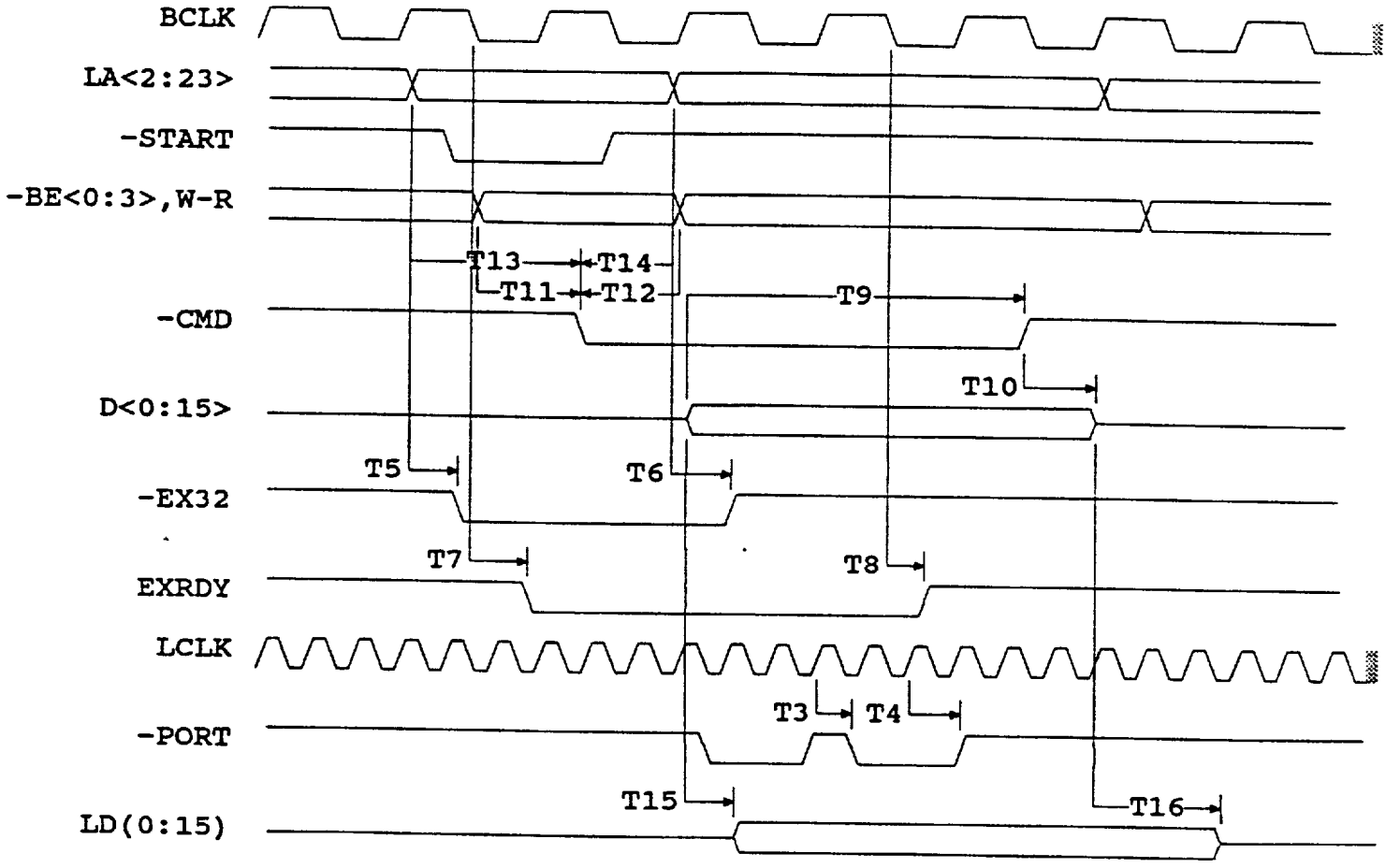
The 82596 initiates an EISA bus request by asserting HOLD to the EISA 9032. When the EISA 9032 detects HOLD, it drives -MREQx to the EISA bus and waits to receive -MAKx from motherboard. After the EISA 9032 detects -MAKx, it will assert HLDA to the 82596 and will enable the EISA 9032 internal address buffers.

Bus Arbitration

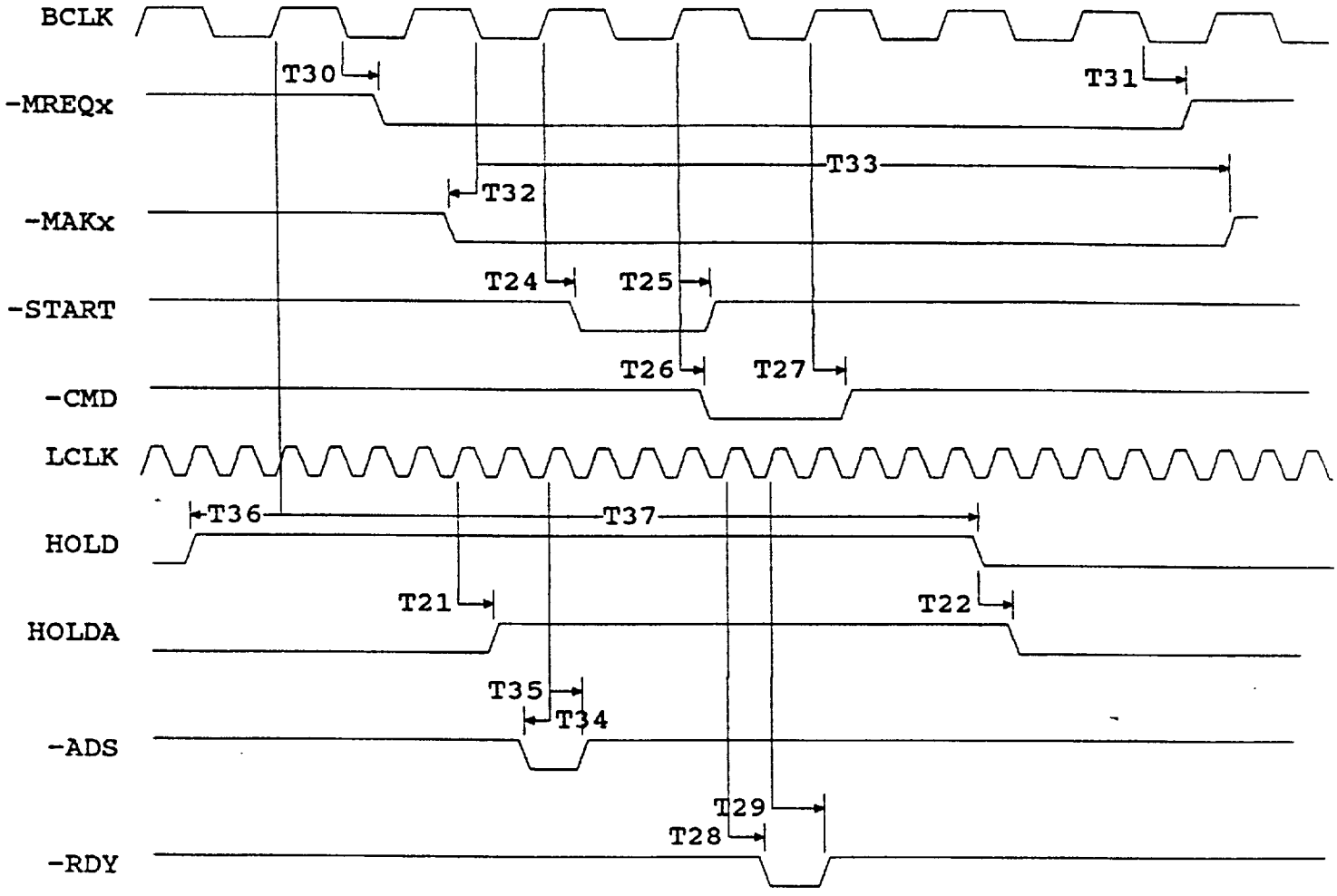
The centralized arbitration controller arbitrates the request, -MREQx ,and the system board asserts a bus grant signal, -MAKx, when the bus is available. An EISA bus master may be preempted by another device that requests use of the bus. The EISA 9032 allows the 82596 to hold the bus for 55 BCLKs or 23 BCLKs from the preemption after sampling its -MAKx signal negated. At this point, the EISA 9032 removes HLDA to the 82596 which allows 9 BCLKs for the 82596 to release the bus.



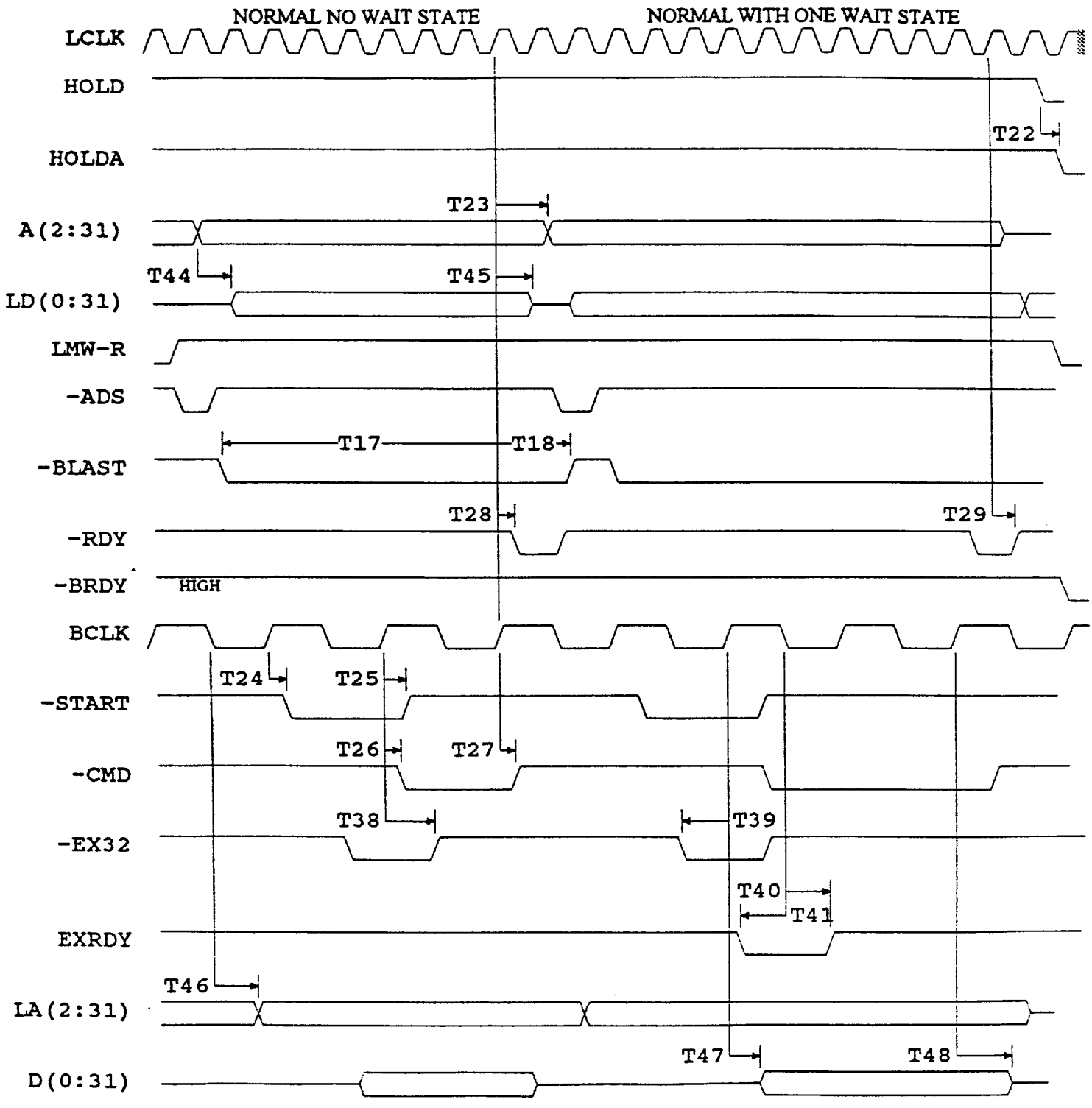
EISA 9032 CA WRITE TIMING



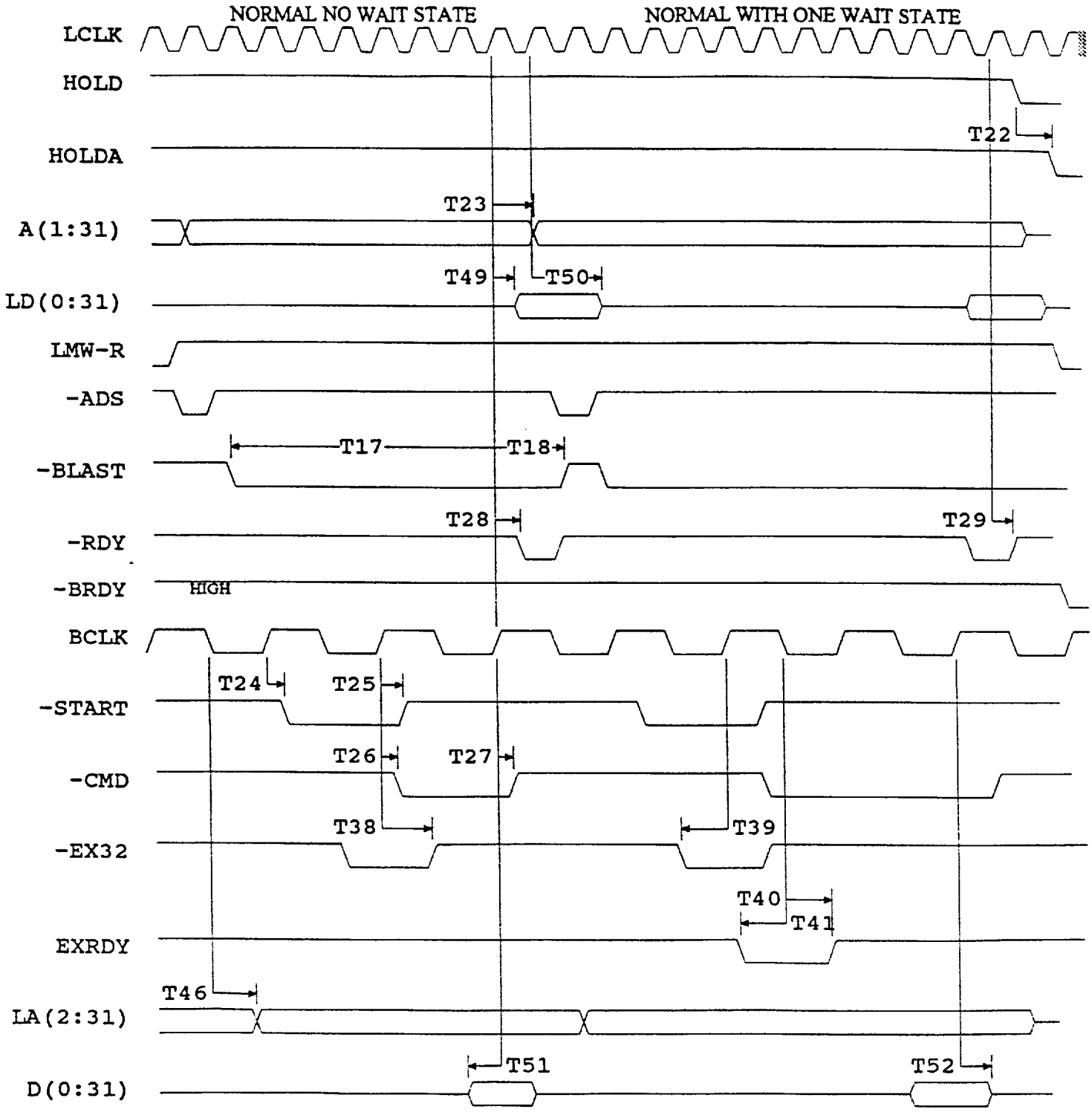
EISA 9032 PORT WRITE TIMING



EISA 9032 MASTER ARBITRATION



EISA 9032 NON-BURST WRITE



EISA 9032 NON-BURST READ

EISA 9032 TIMING

Symbol	Description	Min	Max
T1	LCLK rising to CA asserted delay		25
T2	LCLK rising to CA negated delay		25
T3	LCLK rising to -PORT asserted delay		25
T4	LCLK rising to -PORT negated delay		25
T5	LA(2:23) valid to -EX32 asserted delay		25
T6	LA(2:23) invalid to -EX32 negated delay		25
T7	BCLK falling to EXRDY asserted delay		30
T8	BCLK falling to EXRDY float delay		30
T9	D(0:15) to -CMD negated setup time	110	
T10	-CMD negated to D(0:15) hold time	25	
T11	-BE(0:3), W-R to -CMD asserted setup time	80	
T12	-CMD asserted to -BE(0:3), W-R hold time	25	
T13	LA(2:23) to -CMD asserted setup time	120	
T14	-CMD asserted to LA(2:23) hold time	25	
T15	D(0:15) valid to LD(0:15) valid delay		15
T16	D(0:15) tri-state to LD(0:15) tri-state delay		15
T17	-BLAST to LCLK rising setup time		15
T18	LCLK rising to -BLAST hold time	10	
T21	LCLK rising to HOLDA asserted delay		20
T22	HOLD negated to HOLDA negated delay		15
T23	LCLK rising to A(1:31) valid delay		25
T24	BCLK rising to -START asserted delay		25
T25	BCLK rising to -START negated delay		25
T26	BCLK rising to -CMD asserted delay		25
T27	BCLK rising to -CMD negated delay		25
T28	LCLK rising to -RDY asserted delay		15
T29	LCLK rising to -RDY negated delay		15
T30	BCLK falling to -MREQx asserted delay		33
T31	BCLK falling to -MREQx negated delay		33
T32	-MAKx to BCLK falling setup time	10	
T33	BCLK falling to -MAKx hold time	25	
T34	-ADS to LCLK rising setup time	10	
T35	LCLK rising to -ADS hold time	10	
T36	HOLD to BCLK rising setup time	20	
T37	BCLK rising to HOLD hold time	10	
T38	BCLK rising to -EX32 hold time	15	
T39	-EX32 to BCLK rising setup time	25	
T40	BCLK falling to EXRDY hold time	5	
T41	EXRDY to BCLK falling setup time	15	
T44	LCLK rising to LD(0:31) valid delay		25
T45	LCLK rising to LD(0:31) hold time	40	
T46	BCLK falling to LA(2:31) valid delay		25
T47	BCLK rising to D(0:31) valid delay		40
T48	BCLK rising to D(0:31) hold time	4	
T49	BCLK rising to LD(0:31) read data valid delay		25
T50	LCLK rising to LD(0:31) tri-state delay		25
T51	D(0:31) to BCLK rising setup time	15	

SECTION 6 - Electrical Specifications & Max Ratings

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0°C to+70°C	5V +/- 5%	Min = VSS Max = VDD

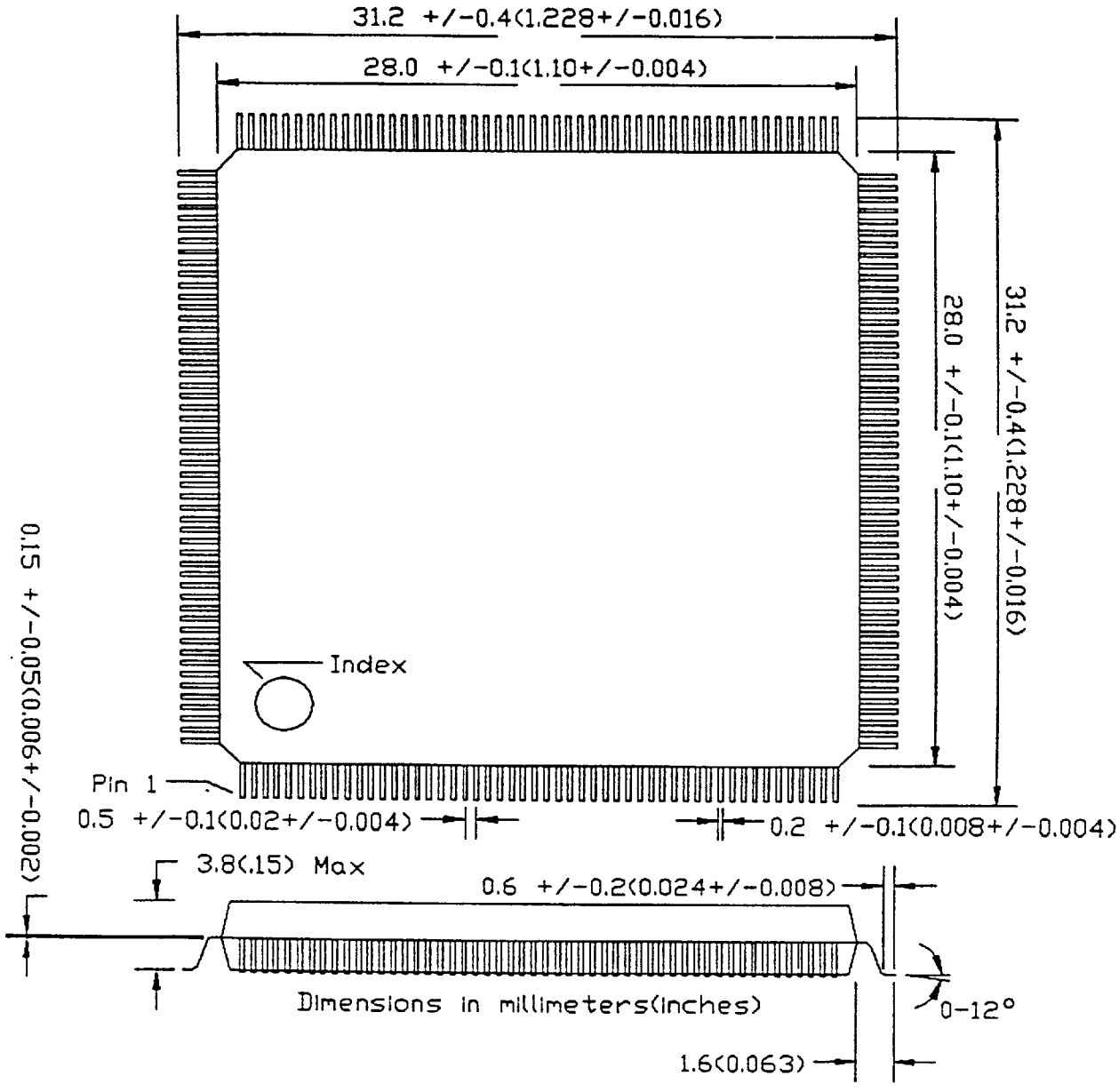
Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN =2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min, VIN=VIH or VIL	IOH = -4.0mA	2.4		V
VOL	Output Low Voltage		IOL per Tables 3.1-3.4		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS <= VIN <=VDD VDD = Max		-10	+10	uA
IOZ	Tri-state Output Leakage Current	VDD= Max VSS <= VIN <=VDD		-10	+10	uA
ICC	Power Supply Current	VDD= Max (Typical = 40 mA)			80	mA

Section 7 - Package Mechanical Dimensions



EISA 9032

APRIL 1993
Patent Pending

EISA Bus Master Interface Chip
National DP83932/4 Mode

Features

- EISA Bus Master Interface Chip containing all control logic and 32 bits of address and data buffering
- Supports EISA Burst Mode Data rates to 33 MBytes/sec
- BIOS PROM and Node ID PROM support
- 25 MHz or 33 MHz Clock
- Multiple local controller configuration modes (this specification describes National DP83932/4 SONIC/SONIC-T mode)
- Low power CMOS in 208 Pin Plastic QFP Package

General Description

The EISA 9032 is an EISA bus master chip which can be configured to connect with several local controllers. This specification describes the mode which supports National Semiconductor's DP83932 (SONIC) and DP83934 (SONIC-T) LAN controllers. PLX also provides specifications for the other modes supported by the EISA 9032.

The 208 pin EISA 9032 is an enhanced version of the 128 pin EISA 9010BV. In addition to the bus interface logic contained in the EISA 9010BV, the EISA 9032 integrates all of the address and data buffers and other random logic.

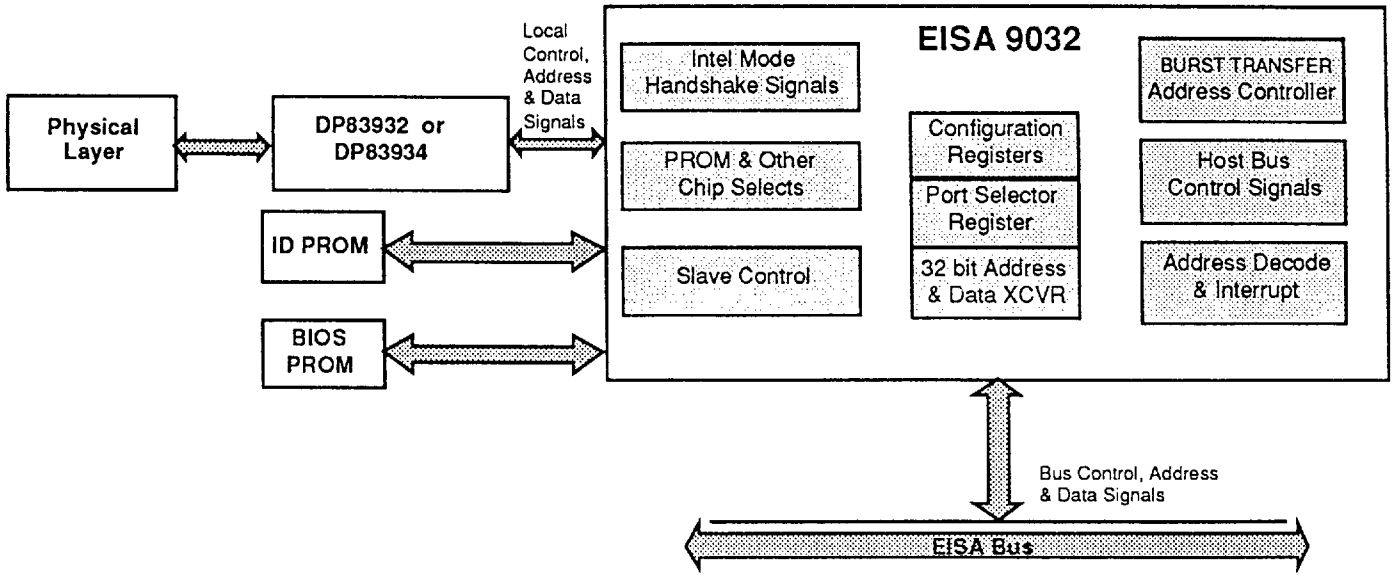


FIGURE 1. Typical Adapter Block Diagram

PLX Technology, Inc., 625 Clyde Avenue, Mountain View, CA 94043 (415) 960-0448 FAX (415) 960-0479

Table of Contents

Section 1	**Introduction** • General Description • Typical Adapter Diagram (Fig. 2) • Pin Out (Fig. 3)
Section 2	**Configuration Registers and Address Decoding**
Section 3	**Pin Description**
Section 4	**Bus Cycle Description**
Section 5	**Timing Diagrams**
Section 6	**Electrical Specifications and Maximum Ratings**
Section 7	**Package Mechanical Dimensions**

SECTION 1 - INTRODUCTION

EISA 9032 GENERAL DESCRIPTION

The EISA 9032 is an EISA bus master interface chip which can be configured to connect with several local controllers. This data sheet describes only the mode which supports National Semiconductor's DP83932 SONIC or DP83934 SONIC-T Ethernet LAN controllers. The other modes supported by the EISA 9032 are described in separate data sheets which are available from PLX Technology.

EISA bus master adapters which use National Semiconductor LAN controllers and the EISA 9032 offer substantial performance advantages over slave adapters as LAN performance is significantly enhanced by the more efficient protocol processing of the DP83932/4. The bus master implementation frees the host processor from managing bus data transfer operations, which improves overall system performance.

Using the PLX Technology 9000 series of bus master chips also reduces total hardware and software development costs for LAN adapter manufacturers designing EISA, Micro Channel and AT compatible boards. In addition to the EISA 9032 interface chip, PLX Technology provides the MCA 9010 and AT 9010, which are Micro Channel and AT bus master chips that have local interfaces identical to the EISA 9032. Therefore, by using the 9000 series, similar hardware designs and software drivers can be used for all three buses; EISA, AT and Micro Channel.

EISA 9032 FUNCTIONS

Data Transfer Modes

The EISA 9032 supports 32 bit Burst Data Transfers at up to 33 Megabytes per second of instantaneous data transfer rate. In addition, the EISA 9032 supports slave mode for initialization of registers and access to other adapter board slave devices such as BIOS ROM, Node ID PROM or other memory and I/O devices.

Configuration Registers

The EISA 9032 contains five internal configuration registers. These registers contain configuration data which is loaded from the host during I/O setup. Included in these registers are the interrupt request level, PREEMPT timer configuration, Port select data, data size, I/O address decode bits, and PROM address decode bits. The EISA 9032 also provides four external user bits for application specific configuration information.

The EISA card ID information is supplied externally to the EISA 9032 and is contained in the Node ID PROM.

Specific EISA 9032 functions

EISA 9032 major functions include:

1. **Master Control Signal Protocol Converter.** The EISA 9032 converts all handshakes of the local controller to EISA signals.
2. **Slave controller.** The EISA 9032 includes an EISA slave interface for control of adapter board slave devices.
3. **Address decoder.** The EISA 9032 decodes host address bits LA23-LA16, and LA11-LA2. The EISA 9032 decodes these addresses to generate chip selects and access configuration registers.
4. **Interrupt generator.** The EISA 9032 can generate one of four host interrupts from one local interrupt, programmable through configuration registers.
5. **Address & Data Buffer .** The EISA 9032 incorporates 32 bit address and 32 bit data buffers.
6. **Clock.** The EISA 9032 runs from crystal or TTL oscillator and generates a 25 MHz or 33 MHz clock for external and internal use.
7. **User programmable configuration bits.** The EISA 9032 provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** All control, data & address signals generated by the EISA 9032 drive the EISA bus directly, without requiring external drivers.
9. **PREEMPT Timer.** Through the configuration registers the user may program a maximum time, 55 BCLKs or 23 BCLKs, which the adapter may hold the bus.
10. **BURST Transfer Address Controller.** During EISA BURST transfers, the EISA 9032 generates A(2-9) to provide pipelined addresses required by the EISA bus.
11. **Adapter ID mapping.** The adapter ID number is mapped into I/O space to allow the option to implement the adapter ID in an ID PROM.

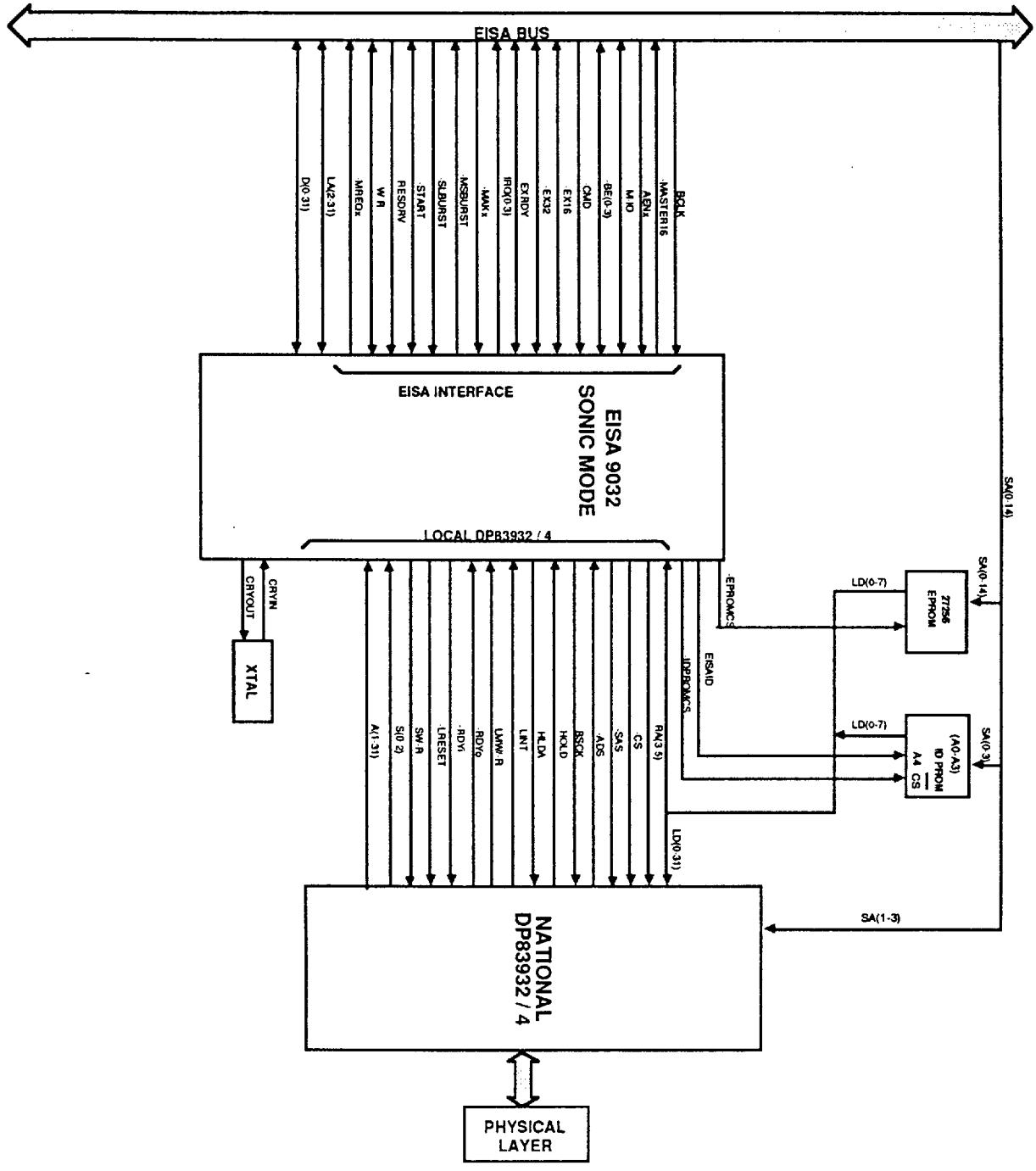


Figure 2. Low Cost EISA Direct Bus Master

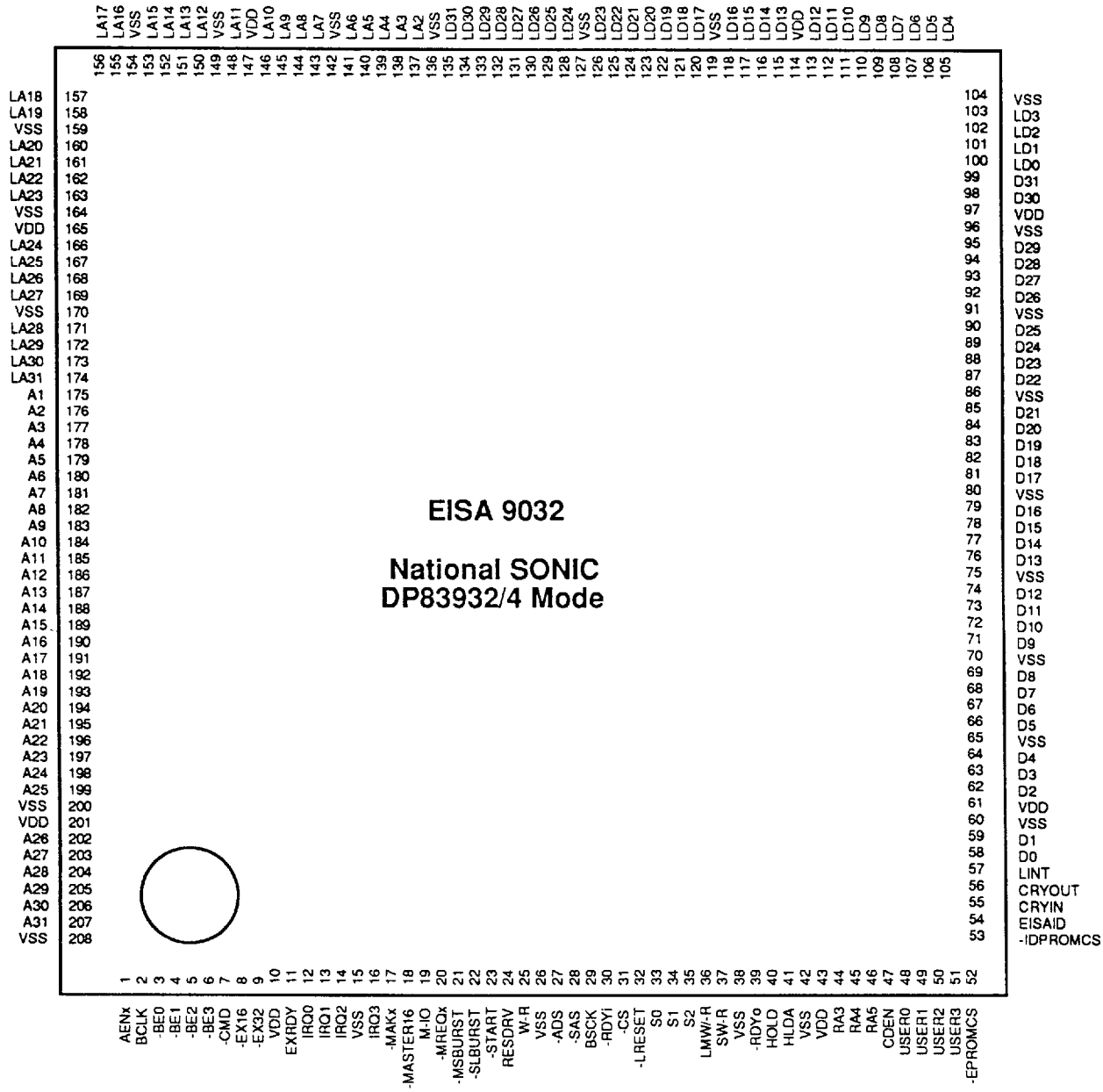


Figure 3.
Pin Out

SECTION 2 - CONFIGURATION REGISTERS AND ADDRESS DECODING

The EISA 9032 decodes the EISA Address signals to select the -CS signal, the Node ID PROM (the EISA board ID is included in the Node ID PROM), the BIOS PROM and the EISA 9032's five internal configuration registers. These five registers provide essential configuration information to the EISA 9032 and the Ethernet adapter board. They are loaded at power-up and may be accessed dynamically through I/O slave cycles.

The -CS, Node ID PROM and four of the five configuration registers may be accessed through an ISA I/O address as well as an EISA slot specific address. The EISA 9032 offers the option of using ISA addressing to simplify converting software drivers written for AT boards to EISA board drivers. For boards with software drivers which use EISA specific addressing, the AT addressing mode is not required. Bit 4 in Register 1 enables ISA addressing.

ADDRESS DECODING

In accordance with the EISA specification, "z" refers to the slot number.

-CS Address. This signal may be activated on either a slot-specific basis or through an ISA decode procedure. Bit 4 in Configuration Register 1 enables the ISA addressing mode.

If slot-specific decode mode is selected , then -CS is selected by Address 0z000h to 0z050h.

If the ISA slot-specific address mode is selected (Bit 4 of Register 1= 1), then-CS is selected by the ISA Address indicated in Register 1, Bits 5-7, in addition to the slot-specific addresses.

EISA ID and Node ID PROM Address Both the EISA ID and the Ethernet Address reside in the same ID PROM. The four byte EISA ID and the Node ID PROM are selected through the EISA ID, -IDPROMCS, LA(2-11) and SA(0-3) signals as follows:

EISA Address (LA 2-11)	-IDPROMCS	EISA ID (A4)	System Address (SA3-0)	
0zC80h-83h	Active(0)	Active(1)	0h	EISA ID, First Byte
	Active(0)	Active(1)	1h	EISA ID, Second Byte
	Active(0)	Active(1)	2h	EISA ID, Third Byte
	Active(0)	Active(1)	3h	EISA ID, Fourth Byte
0zC90h-97h	Active(0)	Inactive(0)	0-5h	6 Ethernet ID Bytes
	Active(0)	Inactive(0)	6-7h	Spare PROM Bytes

Note: The EISA ID pin of the EISA 9032 and -IDPROMCS signals are decoded from the EISA address and byte enable signals. The EISA ID pin of the EISA 9032 should be connected to the PROM address pin A4. The System Address (SA) signals are connected to the ID PROM through buffers as shown in figure 2. A typical PROM address map is as follows:

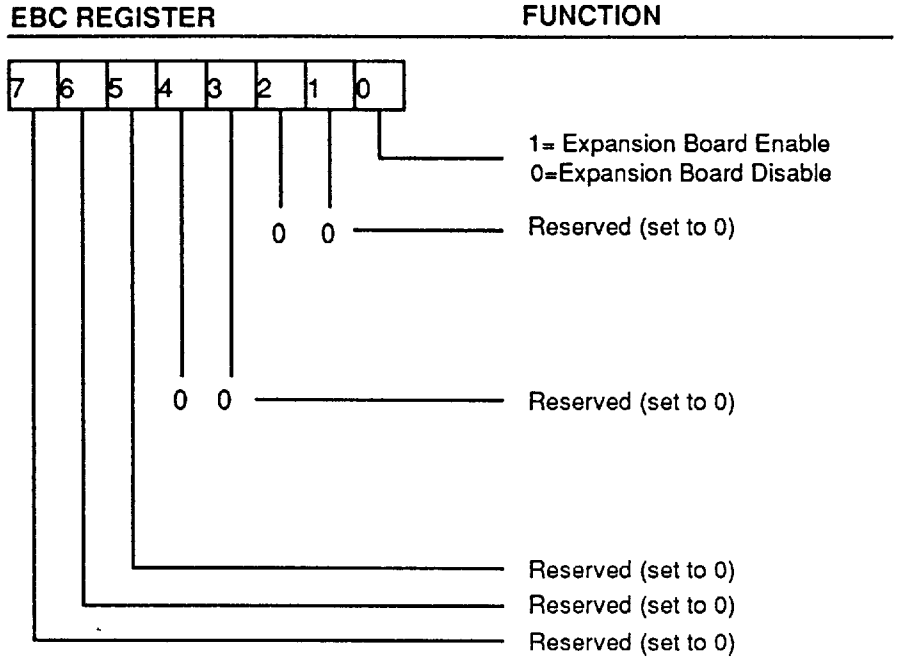
PROM Address A4-A0 (EISA ID plus SA3-0)	**Data**
00 - 05h	6 Ethernet ID Bytes
06 - 07h	Spare PROM Bytes
08 - 0Fh	Not used
10h	EISA ID, First Byte
11h	EISA ID, Second Byte
12h	EISA ID, Third Byte
13h	EISA ID, Fourth Byte
14 - 1Fh	Not used

-EPROMCS Address This BIOS PROM chip select is decoded from address bits LA(13-23), the LA(13-16) bits are programmable in Configuration Register 2, Bits 2-5.

Configuration Register Address The five configuration registers reside in the EISA configuration space at 0zC8Xh where "z" is the slot number and "X" is the register address.

CONFIGURATION REGISTERS

EBC Register- Expansion Board Control Bits Register; at 0zC84h



Bit 0 - Enables Expansion Board

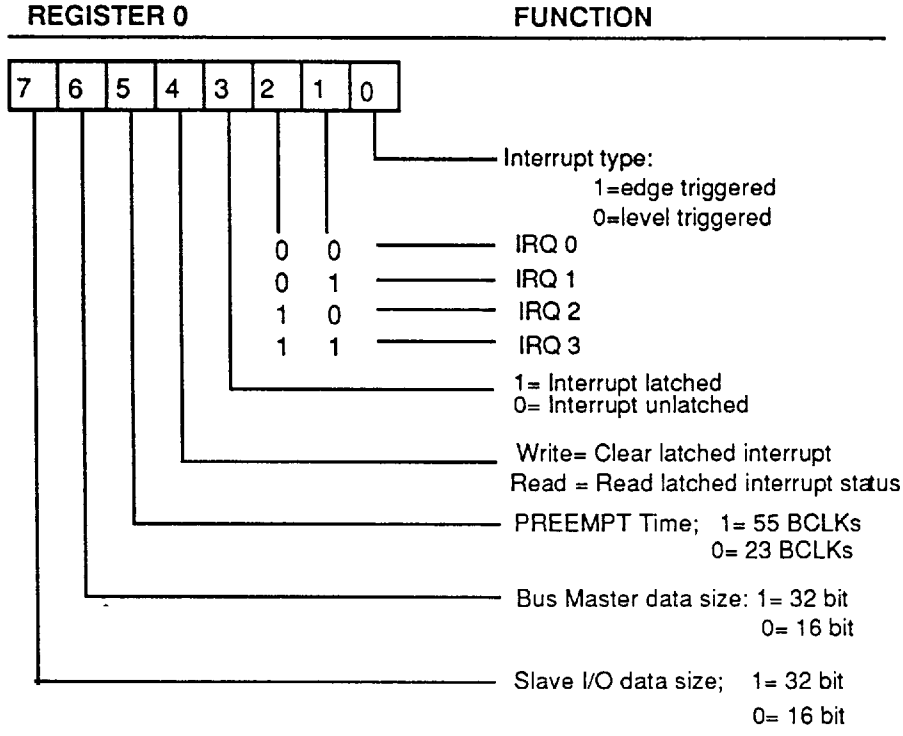
Bit 1-7 - Reserved

All register bits default to 0.

Register 0 ; at 0zC88h

This register contains configuration data that is written by the host during I/O set-up.

WRITE / READ



Bit 0 - Interrupt types: This bit defines whether the IRQ0-IRQ3 are level sensed or edge triggered.

Bit 0= 1, edge triggered

Bit 0= 0, level triggered (default)

Bit 1,2 - These bits select which EISA interrupt level is used when the DP83932/4 asserts its interrupt request line.

Bit 3 - This bit specifies whether the interrupt is latched or unlatched; 1= latched mode. 0= unlatched mode (default)

Bit 4 - The user can write a 1 to this bit to clear the latch mode interrupt or read this bit for latched interrupt status (1 is interrupt present, 0 is no interrupt present).

Bit 5 - This bit specifies the amount of time the EISA 9032 may hold the bus after a PREEMPT condition. When this bit is set to 1, the EISA 9032 allows the DP83932/4 to hold the bus 55 BCLKs after PREEMPT. At this point, the EISA 9032 removes HLDA to the DP83932/4 which allows the DP83932/4 nine BCLKs to release the bus. When this bit is set to 0, the EISA 9032 holds the bus for 23 BCLKs after PREEMPT before removing HLDA.

Bit 6 - This bit specifies the data width for bus master transfers. If this bit is set to 1, the bus master data size is 32 bits. If set to zero, the bus master data size is 16 bits. The DP83932/4 is normally set to 32 bits.

Bit 7 - This bit specifies the data width for slave access to the DP83932/4. This bit is dependent on the DP83932/4 and I/O board. When set to 1, the slave I/O data size is 32 bits. When set to 0, the data size is 16 bits. The DP83932/4 is normally set to 16 bits.

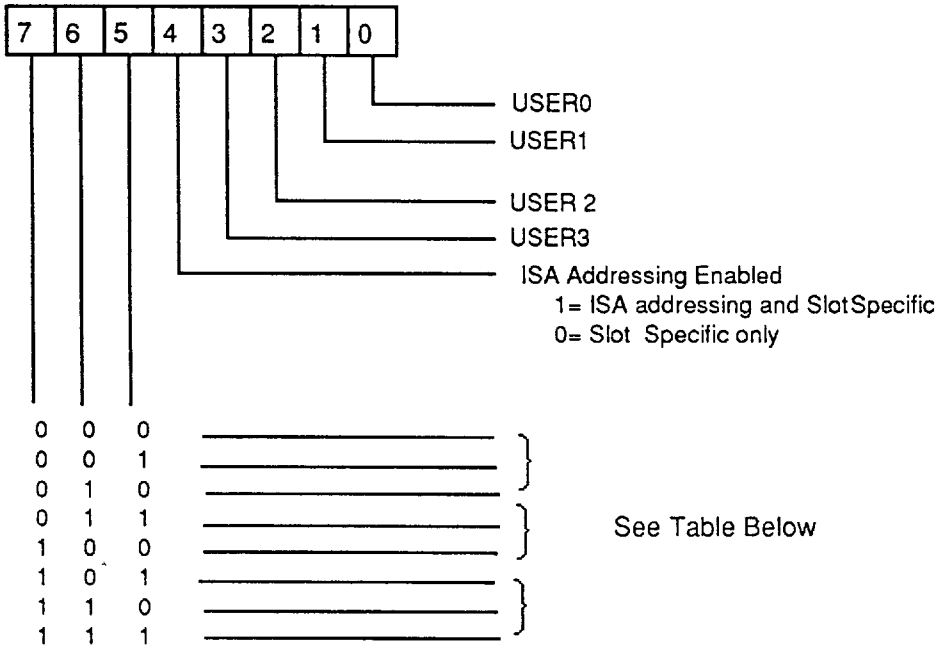
All register bits default to 0.

Register 1 ; at I/O address 0zC89h

This register is loaded at power-up during I/O board configuration. It is used to control external logic through bits 0-3. Register 1 also contains the ISA alias I/O address decode range to select the I/O address of the board in ISA mode.

WRITE / READ

REGISTER 1 **FUNCTION**



BITS 7	6	5	Base Range	-CS	EBC Register	Reg 0	Reg 1	Reg 2	Reg 3	Node ID	EISA ID
0	0	0	100-11F	110-11F	Not Accessible	108	109	10A	10F	100-105	Not Accessible
0	0	1	120-13F	130-13F	"	128	129	12A	12F	120-125	"
0	1	0	140-15F	150-15F	"	148	149	14A	14F	140-145	"
0	1	1	160-17F	170-17F	"	168	169	16A	16F	160-165	"
1	0	0	300-31F	310-31F	"	308	309	30A	30F	300-305	"
1	0	1	320-33F	330-33F	"	328	329	32A	32F	320-325	"
1	1	0	340-35F	350-35F	"	348	349	34A	34F	340-345	"
1	1	1	DISABLED	-	-	-	-	-	-	-	-

Bits 0-3 - These bits connect directly to the USER_PINs and allow Configuration Register control of external logic.

Bits 5-7 - These bits select the I/O address of the board in ISA mode.

All register bits default to 0.

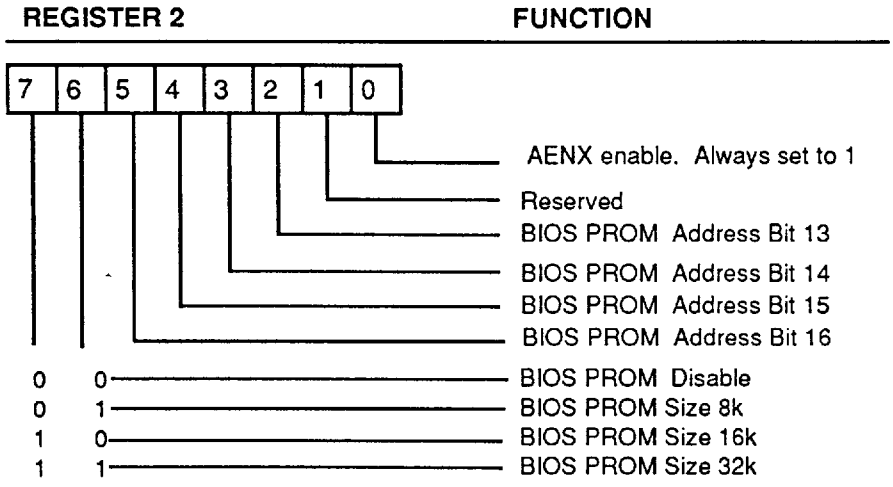
Register 2; at I/O address 0zC8Ah

This register selects the BIOS PROM address range and the BIOS PROM size. The BIOS PROM starting address and size is placed in this register during card configuration. For BIOS PROM selection, address bits LA23-LA13 are specified below:

LA23	LA22	LA21	LA20	LA19	LA18	LA17	LA16	LA15	LA14	LA13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

The EISA 9032 decodes the above value for LA23-LA17 and matches LA16-LA13 with bits 2-5. -EPROMCS will be asserted upon a valid decode and match of LA23-LA13.

WRITE / READ



Bit 0 - AENx enable. Always set to 1.

Bit 1 - Reserved

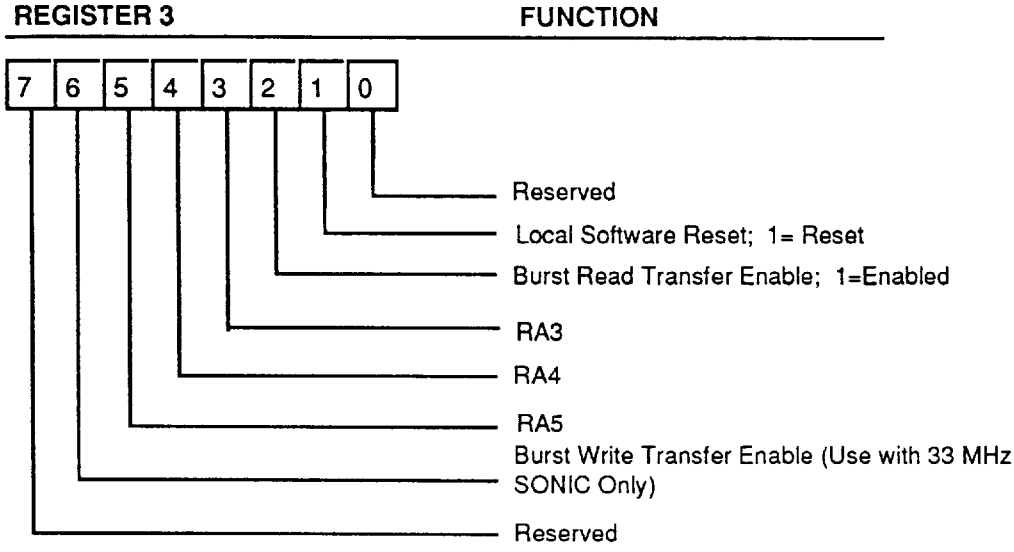
Bits 2-5 - These bits are compared against host addresses LA16-LA13 for determining a BIOS PROM access.

Bits 6-7 - These bits specify the BIOS PROM size as indicated above.

All register bits default to 0.

Register 3; at I/O address 0zC8Fh

This register enables EISA bus bursting and software RESET operation. It also contains DP83932/4 PORT select information. It is loaded at power-up during board configuration.



Bit 0 - Reserved

Bit 1 - When this bit is set to 1, it allows the system to RESET the EISA 9032 by software. The contents of the EISA 9032's registers will **not** be RESET. The default condition is 0.

Bit 2 - EISA Burst Read transfer mode is enabled. 25 MHz or faster DP83932/4 is required.

Bits 3-5 - Address bits which provide DP83932/4 PORT select information.

Bit 6 - EISA Burst Write Transfer Mode is enabled. This mode should be used only with 33 MHz SONIC or SONIC-T controller.

Bit 7 - Reserved

All register bits default to 0.

SECTION 3 - PIN SUMMARY

Pin Summary

Table 3.1 gives a summary of the host bus pins for the EISA 9032 device. The Host Interface consists of the pins for the EISA bus(but not including address, data pins see Table 3.3). Table 3.2 gives a summary of the local interface pins. The Local interface consists of the pins for the DP83932/4 interface. The following abbreviations are used:

I/O - Input and Output Pin
I - Input Pin Only
O - Output Pin Only
TS - Three-state Pin
OC - Open Collector Pin
TP - Totem Pole Pin

Table 3.1 Host Interface - EISA Bus Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
AENx	1	I	-	-
BCLK	1	I	-	-
-BE(0-3)	4	I/O	TS	24
-CMD	1	I	-	-
-EX16	1	I/O	OC	24
-EX32	1	I/O	OC	24
EXRDY	1	I/O	OC	24
IRQ(0-3)	4	O	OC/TP*	6
-MAKx	1	I	-	-
-MASTER16	1	O	OC	24
M-IO	1	I/O	TS	24
-MREQx	1	O	TP	6
-MSBURST	1	O	TS	24
-SLBURST	1	I	-	-
-START	1	I/O	TS	24
RESDRV	1	I	-	-
W-R	1	I/O	TS	24
TOTAL PINS	**23**			

* OC in level triggered mode, TP in edge triggered mode.

Table 3.2. Local Bus Pin Summary for National Semiconductor DP83932/4

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
-ADS	1	I	-	-
BSCK	1	O	TP	4
CDEN	1	O	TP	4
CRYIN	1	I	-	-
CRYOUT	1	O		
-CS	1	O	TP	4
EISAID	1	O	TP	4
HLDA	1	O	TP	4
HOLD	1	I	-	-
LINT	1	I	-	-
RA(3-5)	3	O	TP	4
LMW/-R	1	I	-	-
-EPROMCS	1	O	TP	4
-IDPROMCS	1	O	TP	4
-RDYi	1	O	TP	4
-RDYo	1	I	-	-
-LRESET	1	O	TP	4
S(0-2)	3	I	-	-
SW-R	1	O	TP	4
-SAS	1	O	TP	4
USER(0-3)	4	O	TP	4
TOTAL PINS	**28**			

Table 3.3 Buffer Control, Address and Data Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
LD (0-31)	32	I/O	TS	4
D (0-31)	32	I/O	TS	24
LA (2-31)	30	I/O	TS	24
A (1-31)	31	I	-	-
TOTAL PINS	**125**			

Table 3.4 Power, Ground and No Connect Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
NC	0	-	-	-
VDD	8	I	-	-
VSS	24	I	-	-
TOTAL PINS	**32**			

Table 3.5 Host Interface- EISA Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
AENx	Address Enable	I	1	This active high slot specific input signal indicates (when deasserted) that the EISA 9032 may respond to address and I/O commands.
BCLK	Bus Clock	I	2	This active high input is provided for synchronizing EISA bus events with the host system clock. BCLK operates at a frequency 8.333 MHz with a duty cycle of 50 percent.
-BE(3) -BE(2) -BE(1) -BE(0)	Byte Enables	I/O	6 5 4 3	These active low I/O signals are the byte enables that identify the specific bytes addressed in a double word. These signals and the address lines LA(2-23), are pipelined from one cycle to the next -BE(3) enables the high byte (byte 3) of a double word while -BE(0) enables the low byte. During slave cycles, BE(0-3) are used to generate address bits 0 and 1.
-CMD	Command Strobe	I	7	This active low input signal provides timing control within the EISA bus cycle. The system board asserts this signal on the rising edge of BCLK, simultaneous with the deassertion of the -START signal.
-EX16	16 Bit Slave	I/O	8	This active low I/O signal indicates an EISA memory or I/O slave is capable of transferring 16 bits of data. It is driven during slave accesses to SONIC or SONIC-T or SONIC-T registers. During 16 bit bus master transfers the EISA 9032 samples -EX16 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the EISA 9032 floats the -BE(0-3) and -START lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the EISA 9032 completes the cycle.
-EX32	32 Bit Slave	I/O	9	This active low I/O signal indicates an EISA memory or I/O slave is capable of transferring 32 bit double word size. During 32 bit bus master transfers the EISA 9032 samples -EX32 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the EISA 9032 floats the -BE(0-3) and -START lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the EISA 9032 completes the cycle.

EXRDY	EISA Channel Ready Input and Output	I/O	11	This active high open collector signal lengthens a bus cycle from its standard one BCLK time. It is asserted by a memory or I/O device when it can not respond quickly enough. When EXRDY is low the EISA 9032 inserts wait cycles (one BCLK) until memory brings this signal high. The EISA 9032 pulls EXRDY low during slave cycles.
IRQ(3) IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	O	16 14 13 12	These signals are used to inform the system of the completion of a task. IRQ(0-3) selection is programmable in the configuration registers. They may be programmed to active high totem pole or active low open collector.
-MAKx	Master Acknowledge	I	17	This active low slot specific signal is asserted by the system board to grant access to the EISA bus. The signal is in response to the EISA 9032 asserting the -MREQx signal. The EISA 9032 must release the EISA bus within 7.68 usec after this signal is deasserted.
-MASTER16	16 Bit Bus Master	O	18	When this three-state output signal is asserted the EISA 9032 is a 16 bit bus master. This pin is programmable in the configuration registers.
M-IO	Memory or I/O	I/O	19	This three-state signal distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M-IO is low an I/O cycle is in progress, M-IO is pipelined from one EISA bus cycle to the next.
-MREQx	Master Request	O	20	This active low totem pole, slot specific, output signal is asserted by the EISA 9032 to request EISA bus access. The system board asserts -MAKx in response to this signal.
-MSBURST	Master Burst	O	21	The EISA 9032 asserts this active low output signal to indicate to the slave that it is executing burst cycles. Burst transfers are programmable in the configuration registers.
-SLBURST	Slave Burst	I	22	This active low input informs the EISA 9032 that the addressed slave supports burst cycles.
-START	Start Command	I/O	23	This active low three-state signal indicates the beginning of an EISA bus access. It is asserted for one BCLK period after the address is valid on the bus.
RESDRV	Bus Reset	I	24	This active high input signal provides a hard reset to the EISA 9032 chip. Internal logic is initialized by this signal and any transfer operations are aborted.
W-R	Write/Read	I/O	25	This Three-state pin indicates whether to perform an EISA bus write or read operation. When this pin is high a write operation is requested and when low a read.

Table 3.6 Local Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
-ADS	Address Strobe	I	27	This active low input signal informs the EISA 9032 that the DP83932/4 has placed a valid address on the bus.
BSCK	Bus Clock	O	29	This active high clock provides the timing for the DP83932/4 DMA logic.
CDEN	Card Enable	O	47	This totem pole output is asserted when the I/O board has been enabled through the EBC Register.
CRYIN	Crystal Input	I	55	This input pin provides the timing for all synchronous operations in the EISA 9032. It connects to either a TTL clock signal or directly to a crystal.
CRYOUT	Crystal Output	O	56	This output signal connects directly to crystal oscillator.It is a no connect pin when the the CRYIN pin connects to a TTL clock signal.
-CS	Chip Select	O	31	The EISA 9032 asserts this active low signal when it has detected an access to the DP83932/4 's I/O registers. The DP83932/4 's ISA I/O address is programmable in Configuration Register 1, (0zC89h).
EISAID	EISA ID address bit	O	54	This address bit (comparable to ID PROM A4) is active during EISA product ID accesses. This signal is active when LA(2,3,4) = (0,0,0)
HLDA	Bus Hold Acknowledge	O	41	This active high totem pole output signal indicates the EISA 9032 has successfully gained access to the host bus. When the DP83932/4 receives this signal it begins bus master operation.
HOLD	Bus Hold Request	I	40	This active high input indicates the DP83932/4 needs to gain access to the host bus.
LINT	DP83932/4 Local Interrupt	I	57	This active high input is active when the DP83932/4 has an interrupt pending. The EISA 9032 asserts one of four host interrupts when this signal is active.The host interrupt line that is asserted is programmable in Configuration Register 0, bits 1 and 2.
RA(3-5)	Register Address 3-5	O	44,45,46	These three-state active high pins contain the contents of the DP83932/4 Port Selector Register. They determine one of the eight ports to be selected in the DP83932/4 when using ISA addressing.
-LRESET	Reset	O	32	This active low output signal is asserted and de-asserted synchronous to BSCK. It provides a hardware reset to the DP83932/4 .

LMW/-R	Memory Write or Read	I	36	This input signal is low when a bus master read operation is requested and high for a bus master write operation.
-EPROMCS	BIOS PROM Output Enable	O	52	This active low output pin connects to the output enable pin (-OE) of the BIOS Boot PROM. The EISA 9032 gates the data from the PROM onto the system data bus. The system memory address of the BIOS PROM is programmable in Configuration Register 2.
-IDPROMCS	ID PROM Output Enable	O	53	This active low output pin connects to the output enable pin (-OE) of the Node ID PROM. The EISA 9032 gates the data from the Node ID PROM onto the system data bus. The system I/O address of the ID PROM is programmable in Configuration Register 1.
-RDYi	Ready to DP83932/4	O	30	This active low output signal informs the DP83932/4 of the completion of a memory cycle. When it is high, the DP83932/4 inserts wait states. This signal is sampled by the DP83932/4 synchronously with BSCK.
-RDYo	Ready from DP83932/4	I	39	This active low input from the DP83932/4 is used during system slave accesses to the DP83932/4 's I/O registers. This signal is asserted when the DP83932/4 has completed the I/O cycle and is synchronous to BSCK clock.
S(0-2)	DP83932/4 Bus Status	I	33,34,35	These status signals from the DP83932/4 are used by the EISA 9032 to enable/disable BURST transfers. They indicate the current DP83932/4 bus operation.
-SAS	Slave Address Strobe	O	28	EISA 9032 asserts this output signal to indicate to the DP83932/4 that valid address is on the bus during a register write operation or when the DP83932/4 can begin sourcing data during a register read operation.
SW-R	Slave Read or Write	O	37	The EISA 9032 asserts this output signal to inform the DP83932/4 whether the current access is a read or write to DP83932/4 registers.
USER3 USER2 USER1 USER0	User Defined Pins	O	51,50, 49,48	These totem pole output pins are controlled from Configuration Register 1 for each host interface. They control logic on the I/O board.

Table 3.7 Address and Data Pins

Symbol	Signal Name	I/O	Pin Number	Function
A(1-31)	Local Address	I	175-199, 202-207	These input signals connect directly to the SONIC address pins.

D(0-31)	EISA bus Data	I/O	58,59, 62-64, 66-69, 71-74, 76-79, 81-85, 87-90, 92-95, 98,99	These I/O signals connect directly to the EISA bus.
LA(2-31)	EISA bus Address	I/O	137-141, 143-146, 148, 150-153, 155-158, 160-163, 166-169, 171-174	These I/O signals connect directly to the EISA bus.
LD(0-31)	Local Data	I/O	100-103, 105-113, 115-118, 120-126, 128-135	These I/O signals connect directly to the SONIC, the Mode ID PROM and the BIOS PROM.

Table 3.8 Power and Ground Pin Description

VDD	Power	I	10, 43, 61, 97, 114, 147, 165, 201	Five Volt Power Supply Pins
VSS	Ground	I	15, 26, 38, 42, 60, 65, 70, 75, 80, 86, 91, 96, 104, 119, 127, 136, 142, 149, 154, 159, 164, 170, 200, 208	Ground Pins

SECTION 4 - BUS CYCLE DESCRIPTION

This section describes EISA 9032 local and EISA bus functionality with the 83932/4.

SLAVE CYCLES

In the slave mode, the EISA 9032 monitors the lines LA (11:2) and -BE (3:0) for general I/O address decoding, slot-specific address decoding, and configuration register accessing. During the slave mode, -AENx has to be asserted low.

The configuration registers can be accessed through 8-bit I/O read or write cycles. These cycles are 6 BCLK periods long.

83932/4 Register Access

The 83932/4 registers are accessed through EISA slave I/O cycles. The EISA 9032 decodes the system address and drives -CS, -SAS, RA (3-5) and SW-R to the 83932/4.

-CS is valid for addresses 0z000h-0z050h.

EISA ID, Node ID and BIOS PROM Access

The EISA ID and Ethernet ID use the same ID PROM. The EISAID and -IDPROMCS signals are accessed through 8-bit I/O slave cycles. The EISAID signal should connect to the on board PROM address A4. The EISA 9032 decodes the system address and drives the -EPROMCS for BIOS PROM access.

EISA ID, Node ID and BIOSPROM accesses are executed by the EISA 9032 as 8 bit EISA slave cycles. EXRDY is not deasserted. The -IDPROMCS is valid for addresses 0zC80h-0zC83h, and 0zC90h-0zC97h.

Interrupts

The EISA 9032 provides four interrupt request lines, IRQ(3:0). LINT from the 83932/4 asserts the appropriate EISA interrupt request signals. If the EISA interrupt request line is programmed in the latched mode, reading bit 4 of register 0 will clear the interrupt request signal.

MASTER CYCLES

Bus Request

The 83932/4 initiates an EISA bus request by asserting HOLD to the EISA 9032. When the EISA 9032 detects HOLD, it drives -MREQx to the EISA bus and waits to receive -MAKx from motherboard. After the EISA 9032 detects -MAKx, it will assert HLDA to the 83932/4 and turn on the internal address buffers.

Bus Arbitration

The centralized arbitration controller arbitrates the request, -MREQx ,and the system board asserts a bus grant signal, -MAKx, when the bus is available. An EISA bus master may be preempted by another device that requests use of the bus. The EISA 9032 allows the 83932/4 to hold the bus for 55 BCLKs or 23 BCLKs from the preemption after sampling its -MAKx signal negated. At this point, the EISA 9032 removes HLDA to the 83932/4 which allows 9 BCLKs for the 83932/4 to release the bus.

Burst and Non-burst Modes of Operation

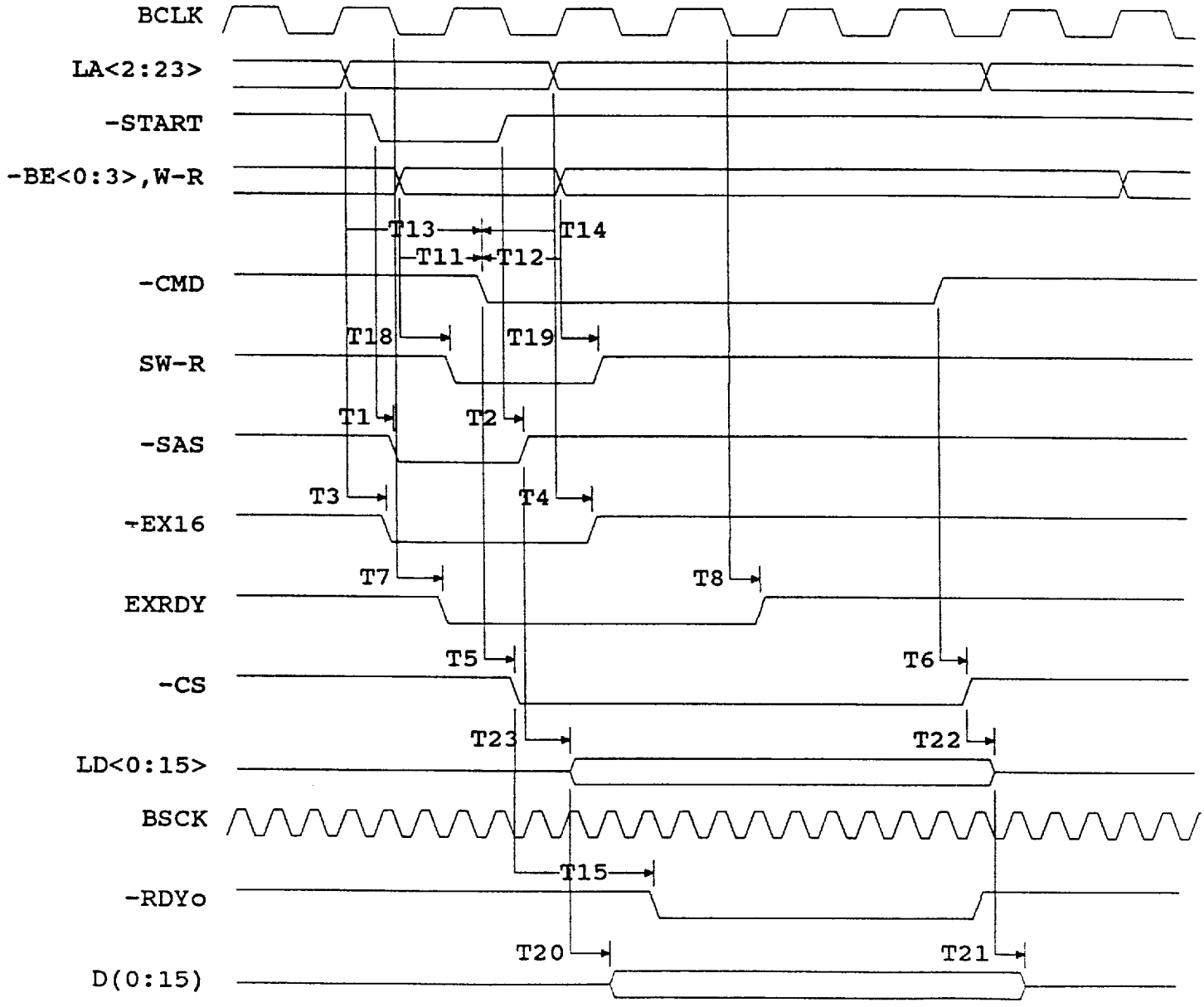
The EISA 9032 can be programmed for burst or non-burst data transfer modes. To execute burst cycles, burst mode must be enabled from configuration register 3. To start a burst cycle, the address must be 4 byte aligned, and subsequent addresses must be contiguous.

If burst mode is enabled, the EISA 9032 will monitor the -SLBURST signal at the beginning of the transfer to determine if the slave device that was addressed is capable of executing burst cycles. If the slave device does not respond with an active -SLBURST, the EISA 9032 will not execute burst cycles. (The EISA 9032 only supports 32 bit burst cycles.)

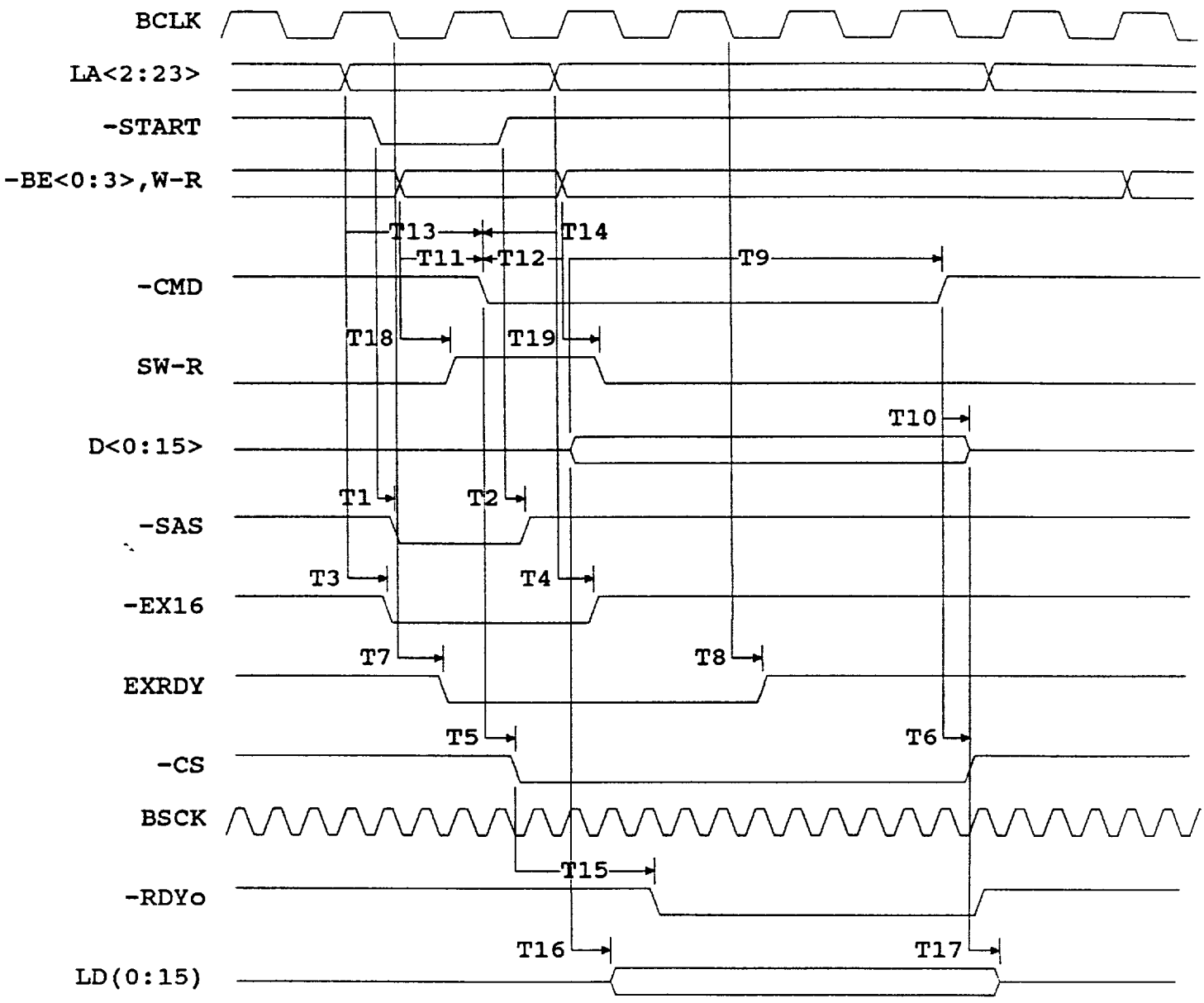
For mismatched translation EISA cycles, the EISA 9032 will monitor the -EX32 signal at the beginning of the transfer to determine if the system memory it addressed has the same bus width. If the -EX32 signal is not active, the EISA 9032 will function in the non-burst mode and will "back-off" the bus by floating -START, -LBE(3:0), and disabling the data buffers allow the motherboard to control the transfer.

1K Byte Page Address Boundary

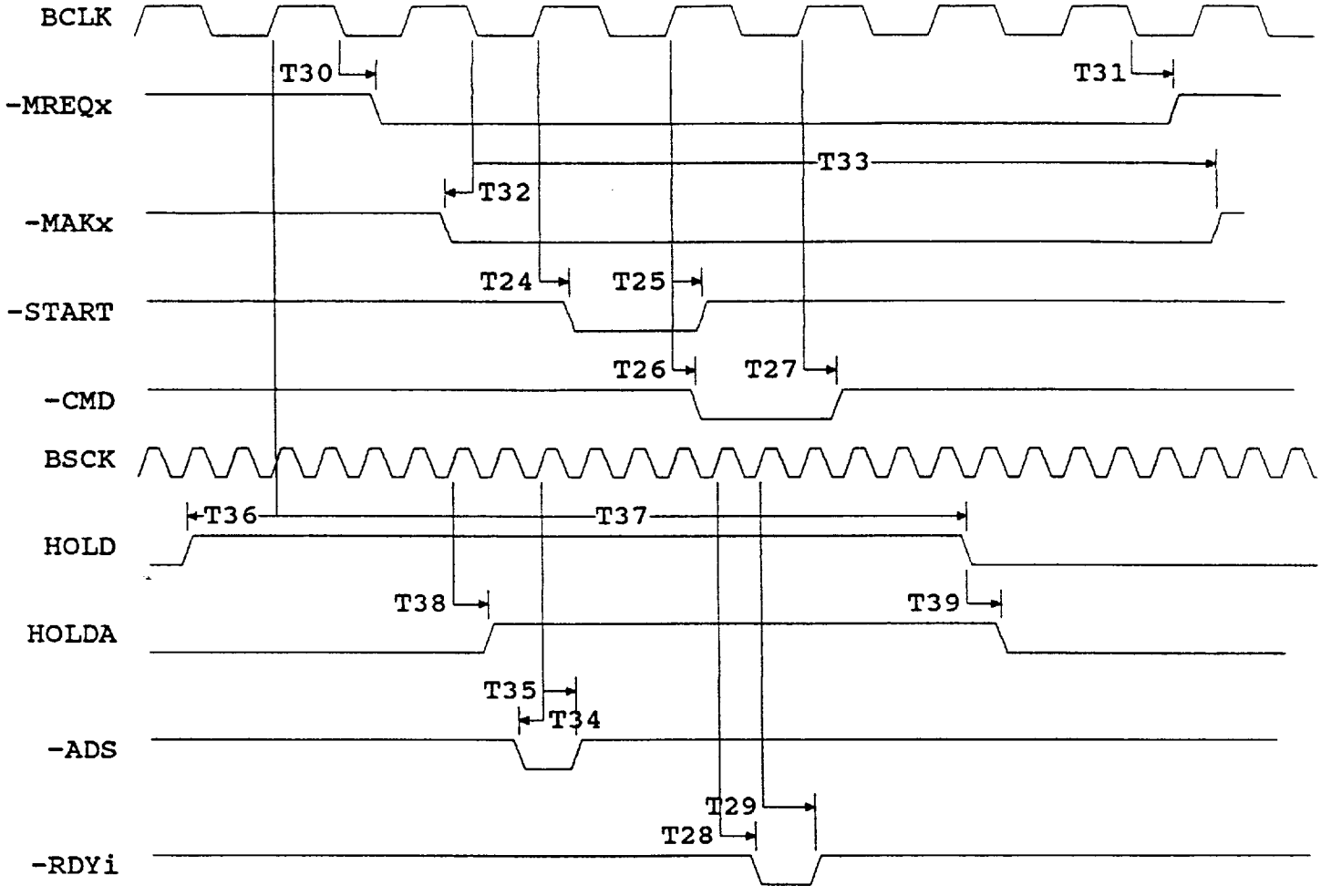
The EISA 9032 will not start a burst cycle if the 83932/4 address is at the 1K byte page boundary address. During the burst cycle, the EISA 9032 provides the support to detect the 1K byte page address boundary. At the 1K byte boundary, the EISA 9032 will exit out of burst mode. HOLD must be deasserted to relinquish the bus.



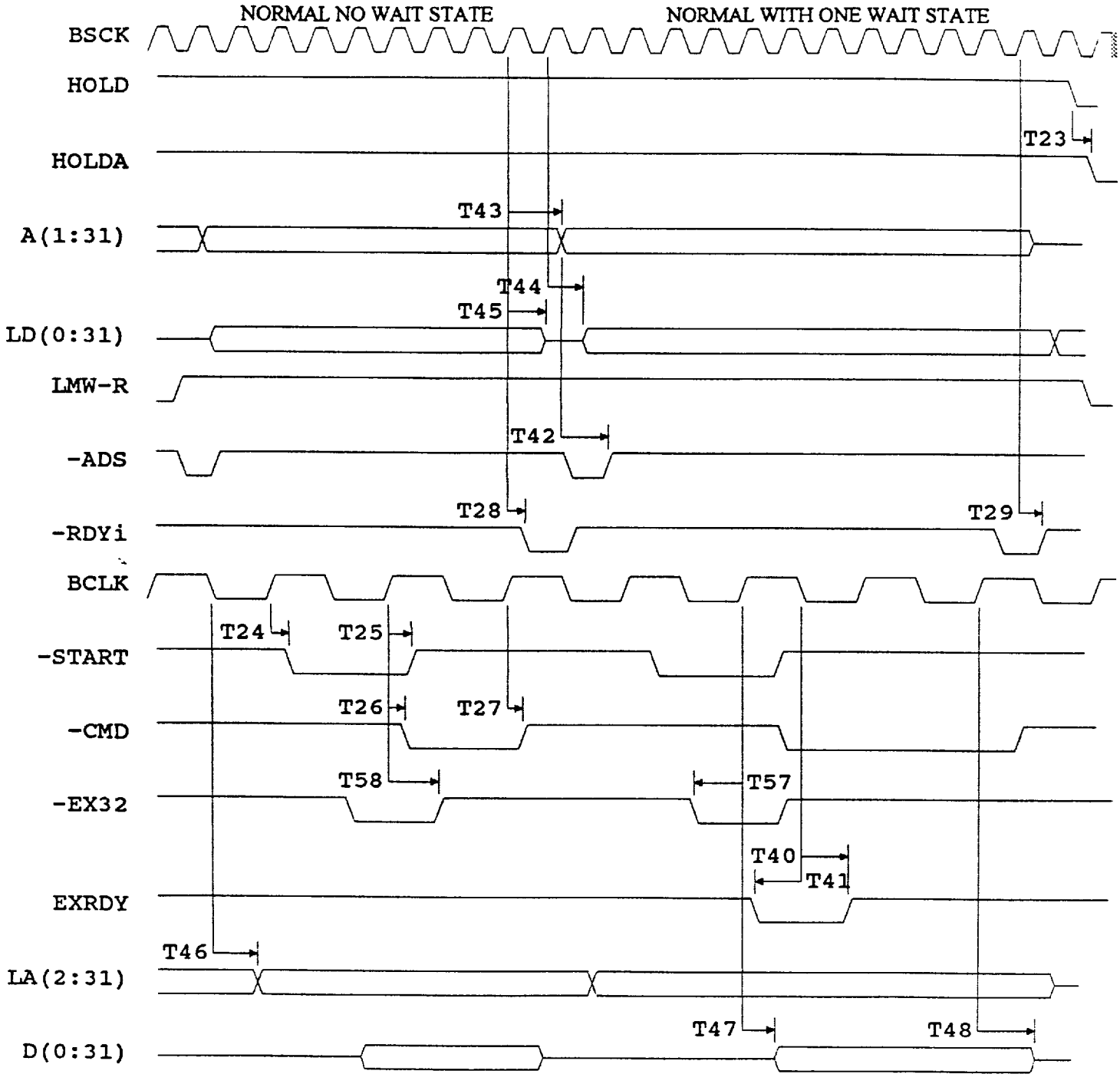
EISA 9032 SLAVE READ TIMING



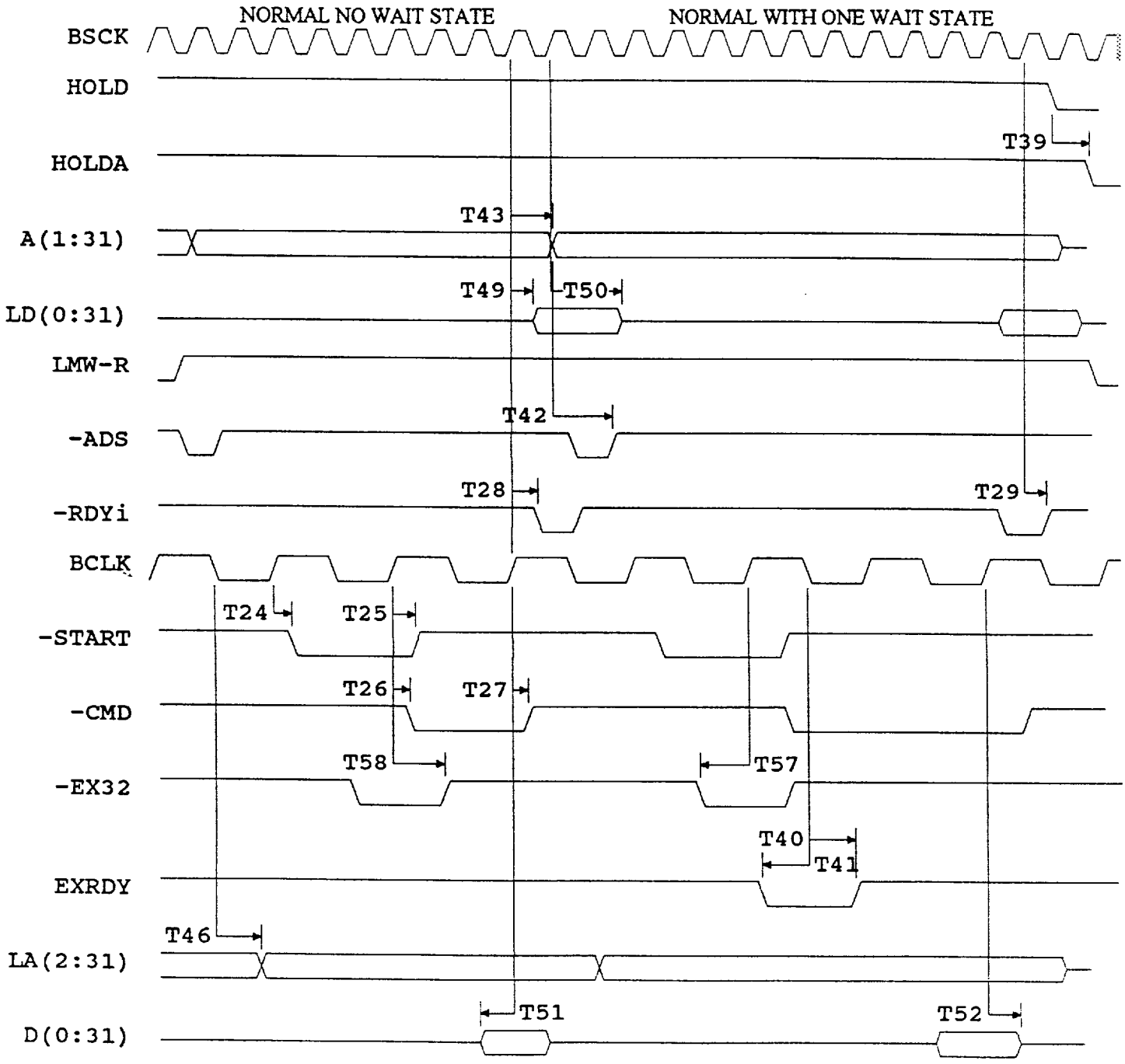
EISA 9032 SLAVE WRITE TIMING



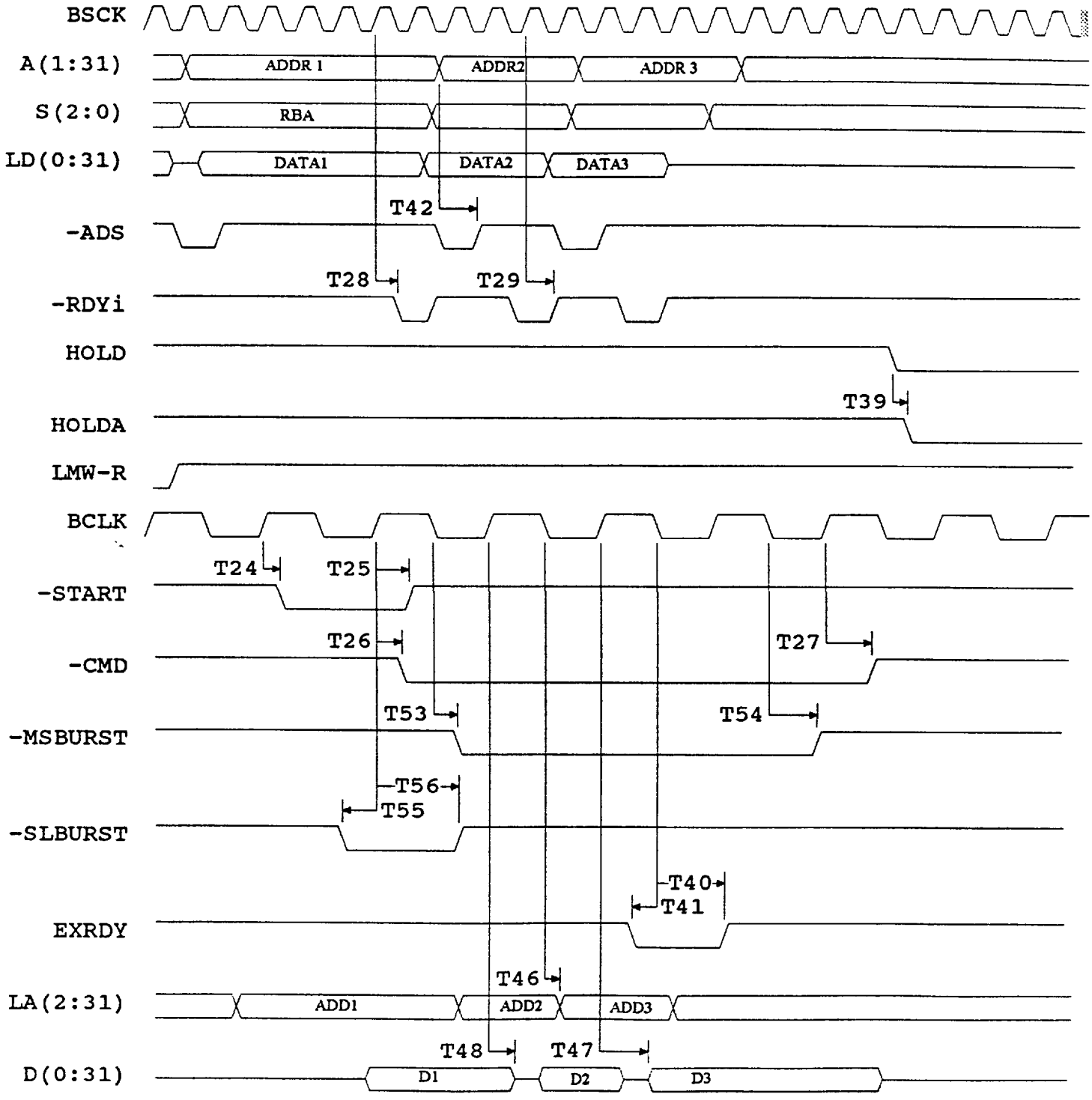
EISA 9032 MASTER ARBITRATION



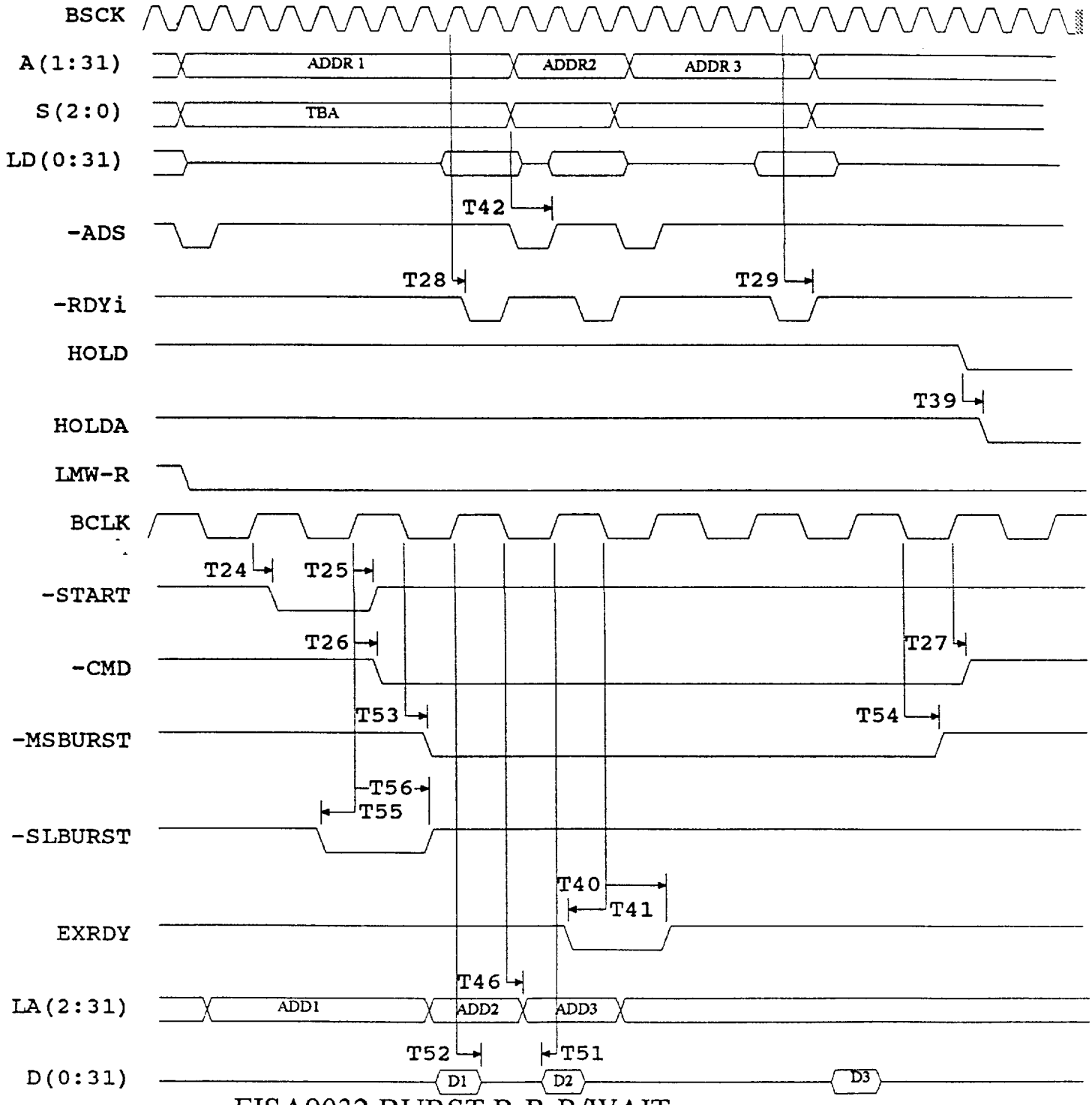
EISA 9032 NON-BURST WRITE



EISA 9032 NON-BURST READ



EISA 9032 BURST W-W-W/WAIT



EISA9032 BURST R-R-R/WAIT

EISA 9032 TIMING

Symbol	Description	Min	Max
T1	-START asserted to -SAS asserted delay		25
T2	-START negated to -SAS negated delay		25
T3	LA(2:23) valid to -EX16 asserted delay		25
T4	LA(2:23) invalid to -EX16 negated delay		25
T5	-CMD asserted to -CS asserted delay		25
T6	-CMD negated to -CS negated delay		25
T7	BCLK falling to EXRDY negated delay		30
T8	BCLK falling to EXRDY float delay		30
T9	D(0:15) to -CMD negated setup time	110	
T10	-CMD negated to D(0:15)hold time	25	
T11	-BE(0:3), W-R to -CMD asserted setup time	80	
T12	-CMD asserted to -BE(0:3), W-R hold time	25	
T13	LA(2:23) to -CMD asserted setup time	120	
T14	-CMD asserted to LA(2:23) hold time	25	
T15	-CS asserted to RDYo asserted delay		100
T16	D(0:15) valid to LD(0:15) valid delay		15
T17	D(0:15) tri-state to LD(0:15) tri-state delay		15
T18	W-R asserted to SW-R asserted delay		25
T19	W-R negated to SW-R negated delay		25
T20	LD(0:15) valid to D(0:15) valid delay		15
T21	LD(0:15) tri-state to D(0:15) tri-state delay		15
T22	-CS negated to LD(0:15) tri-state delay		15
T23	-SAS to LD(0:15) valid delay		60
T24	BCLK rising to -START asserted delay		25
T25	BCLK rising to -START negated delay		25
T26	BCLK rising to -CMD asserted delay		25
T27	BCLK rising to -CMD negated delay		25
T28	BSCK rising to -RDYi asserted delay		15
T29	BSCK rising to -RDYi negated delay		15
T30	BCLK falling to -MREQx asserted delay		33
T31	BCLK falling to -MREQx negated delay		33
T32	-MAKx to BCLK falling setup time	10	
T33	BCLK falling to -MAKx hold time	25	
T34	-ADS to BSCK rising setup time	10	
T35	BSCK rising to -ADS hold time	5	
T36	HOLD to BCLK rising setup time	15	
T37	BCLK rising to HOLD hold time	15	
T38	BSCK rising to HLDA asserted delay		20
T39	HOLD negated to HLDA negated delay		15
T40	BCLK falling to EXRDY hold time	5	
T41	EXRDY to BCLK falling setup time	15	
T42	A(1:31) valid to -ADS rising delay	30	
T43	BSCK rising to A(1:31) valid delay		25
T44	BSCK rising to LD(0:31) write valid delay		25
T45	BSCK rising to LD(0:31) write hold time	40	
T46	BCLK falling to LA(2:31) valid delay		25
T47	BCLK rising to D(0:31) write valid delay		40
T48	BCLK rising to D(0:31) write hold time	4	
T49	BCLK rising to LD(0:31) valid delay		25
T50	BSCK rising to LD(0:31) read tri-state delay		25
T51	D(0:31) read to BCLK rising setup time	15	

T52	BCLK rising to D(0:31) hold time	4	
T53	BCLK falling to -MSBURST asserted delay		25
T54	BCLK falling to -MSBURST negated delay		25
T55	-SLBURST to BCLK rising setup time	15	
T56	BCLK rising to -SLBURST hold time	25	
T57	-EX32 to BCLK rising setup time	15	
T58	BCLK rising to -EX32 hold time	25	

SECTION 6 - Electrical Specifications & Max Ratings

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0°C to+70°C	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN =2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min, VIN=VIH or VIL	IOH = -4.0mA	2.4		V
VOL	Output Low Voltage		IOL per Tables 3.1-3.4		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS <= VIN <=VDD VDD = Max		-10	+10	uA
IOZ	Tri-state Output Leakage Current	VDD= Max VSS <= VIN <=VDD		-10	+10	uA
ICC	Power Supply Current	VDD= Max (Typical = 40 mA)			80	mA

Section 7 - Package Mechanical Dimensions