

# ECN2102/2112

ECN2102 / 2112 is a single chip row driver IC for electroluminescent (EL) display panel.

## Functions

- \* Low-voltage serial to high-voltage parallel converter
- \* 34 outputs of totem pole type

## Features

- \* Output terminal voltage up to 250V
- \* Source / Sink current 500mA

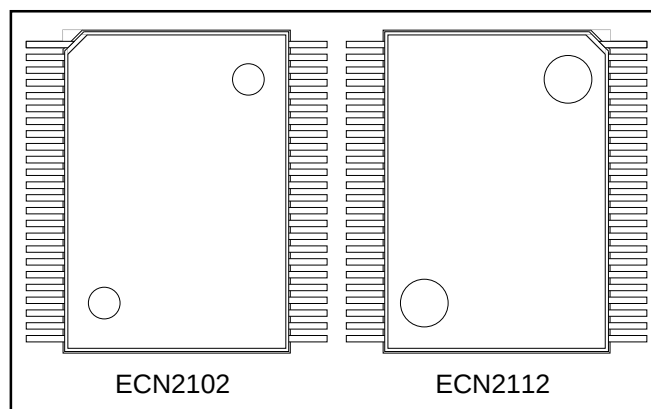
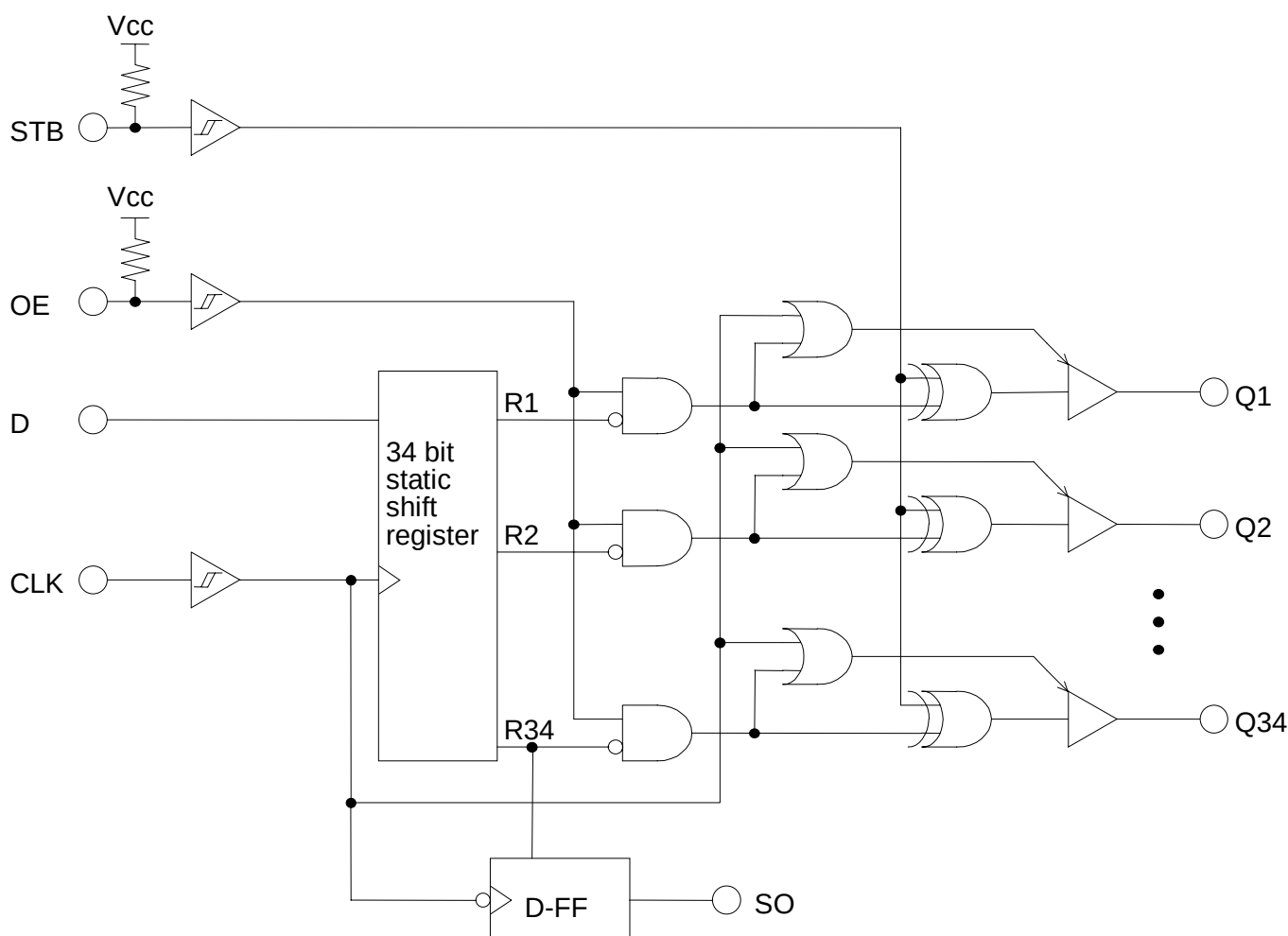


Fig. 1. OUTLINE OF FP-48 PACKAGE



Function Block Diagram (Positive Logic)

# ECN2102/2112

## 1. GENERAL

- (1) TYPE                    ECN2102/ECN2112
- (2) APPLICATION    Row line driver for Electroluminescent (EL) display panel
- (3) STRUCTURE      Monolithic IC, processed Dielectric Isolation.
- (4) PACKAGE        FP-48 (Fig.1)

## 2. MAXIMUM ALLOWABLE RATING (Ta=25°C)

| No | ITEMS                        | SYMBOLS          | RATINGS                     | UNITS | CONDITIONS                                                          |
|----|------------------------------|------------------|-----------------------------|-------|---------------------------------------------------------------------|
| 1  | Supply Voltage (logic)       | V <sub>cc</sub>  | -0.5 ~ +7.0                 | V     | to GND terminal                                                     |
| 2  | Input Voltage (logic)        | V <sub>in</sub>  | -0.5 ~ V <sub>cc</sub> +0.5 | V     | to GND terminal                                                     |
| 3  | V <sub>s</sub> - GND Voltage | V <sub>SG</sub>  | V <sub>cc</sub>             | V     | to GND terminal                                                     |
| 4  | Output Terminal Voltage      | V <sub>Q</sub>   | ±250                        | V     | Between V <sub>s</sub> ,V <sub>cc</sub> ,GND,<br>Input and Q output |
| 5  | Allowable Power Dissipation  | P <sub>T</sub>   | 800                         | mW    |                                                                     |
| 6  | Operating Temperature        | T <sub>OP</sub>  | -40 ~ +85                   | °C    |                                                                     |
| 7  | Storage Temperature          | T <sub>stg</sub> | -55 ~ +150                  | °C    |                                                                     |

## 3. RECOMMENDED OPERATING CONDITIONS

| No | ITEMS                      | SYMBOLS           | Min. | Typ. | Max. | UNITS | CONDITIONS                                          |
|----|----------------------------|-------------------|------|------|------|-------|-----------------------------------------------------|
| 1  | Supply Voltage (logic)     | V <sub>cc</sub>   | 5.0  | 5.5  | 6.0  | V     |                                                     |
| 2  | Clock Frequency            | f <sub>CLK</sub>  | —    | —    | 250  | kHz   | V <sub>cc</sub> = 5.5V<br>V <sub>in</sub> = 0V/5.5V |
| 3  | Clock Pulse Width          | tw <sub>CLK</sub> | 80   | —    | —    | ns    |                                                     |
| 4  | Data Setup Time            | t <sub>su</sub>   | 80   | —    | —    | ns    |                                                     |
| 5  | Data Hold Time             | t <sub>h</sub>    | 80   | —    | —    | ns    |                                                     |
| 6  | Output Terminal Voltage    | V <sub>Q</sub>    | —    | ±230 | —    | V     | V <sub>cc</sub> = 5.5V                              |
| 7  | Peak Output Source Current | I <sub>IOH</sub>  | —    | —    | -500 | mA    | Note 1                                              |
| 8  | Peak Output Sink Current   | I <sub>IOL</sub>  | —    | —    | +500 | mA    | Note 1                                              |

Note1 : Conduction period ≤ 5 μs per 1 IC

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## 4. ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta= 25°C, Vcc= 5.5V, HVCC=230V)

| No | ITEMS                       | SYMBOLS | Min. | Typ. | Max. | UNITS      | C O N D I T I O N S                         |           |
|----|-----------------------------|---------|------|------|------|------------|---------------------------------------------|-----------|
| 1  | Output Voltage (logic)      | VOL     | —    | —    | 0.1  | V          | IOL= 20 $\mu$ A                             |           |
|    |                             | VOH     | 5.4  | —    | —    | V          | IOH=-20 $\mu$ A                             |           |
| 2  | Output Current (logic)      | IOL     | 1.0  | —    | —    | mA         | VOL= 0.8V                                   |           |
|    |                             | IOH     | -1.0 | —    | —    | mA         | VOLH 4.7V                                   |           |
| 3  | Input Voltage (logic)       | VIL     | —    | —    | 1.0  | V          | D input                                     |           |
|    |                             | VIH     | 3.5  | —    | —    | V          |                                             |           |
|    |                             | VTHL    | —    | —    | 0.4  | V          | CLK,STB input                               |           |
|    |                             | VTLH    | 4.5  | —    | —    | V          |                                             |           |
| 4  | Input Current (logic)       | IiH     | —    | —    | 10   | $\mu$ A    | Vin=5.5V all input/1 input                  |           |
|    |                             | IiL     | —    | —    | -10  | $\mu$ A    | Vin=0V D,CLK/1 input                        |           |
|    |                             |         | —    | —    | -100 | $\mu$ A    | Vin=0V STB/1 input                          |           |
| 5  | Dissipation Current(logic)  | Istb    | —    | —    | 10   | $\mu$ A    | No signal all input 5.5V,<br>all output Off |           |
|    |                             | —       | —    | —    | 25   | mA         | No signal, 1ch source output On             |           |
|    |                             | —       | —    | —    | 5    | mA         | No signal, 1ch sink output On               |           |
| 6  | Output Voltage              | HVOL    | —    | —    | 3.0  | V          | HIOL=1mA                                    | Q out-GND |
|    |                             |         | —    | —    | 6.0  | V          | HIOL=200mA                                  | Q out-GND |
|    |                             | HVOH    | —    | —    | 4.0  | V          | HI OH=-1mA                                  | Vs-Q out  |
|    |                             |         | —    | —    | 8.0  | V          | HI OH=-200mA                                | Vs-Q out  |
| 7  | Output SCR dv/dt capability | dv/dt1  | 200  | —    | —    | V/ $\mu$ s | Vs~Q out,+dv/dt apply.Fig.6                 |           |
|    |                             | dv/dt2  | 200  | —    | —    | V/ $\mu$ s | Q out-GND,-dv/dt apply.Fig.7                |           |
| 8  | Output SCR Off Period       | toff    | —    | —    | 6.0  | $\mu$ s    | Source side                                 | Fig.8     |
|    |                             |         | —    | —    | 7.0  | $\mu$ s    | Sink side                                   |           |

## 5. SWITCHING CHARACTERISTICS (Unless otherwise specified, Ta= 25°C, Vcc= 5.5V, Fig.5)

| No | ITEMS                     | SYMBOLS | Min. | Typ. | Max. | UNITS   | C O N D I T I O N S |  |
|----|---------------------------|---------|------|------|------|---------|---------------------|--|
| 1  | Output Delay Time (logic) | tPLH    | —    | —    | 300  | ns      | CL=15pF             |  |
|    |                           | tPHL    | —    | —    | 300  | ns      |                     |  |
| 2  | Output Delay Time         | tQLH    | —    | —    | 3    | $\mu$ s | RLQ=1k $\Omega$     |  |
|    |                           | tQHL    | —    | —    | 3    | $\mu$ s | CLQ=2000pF          |  |

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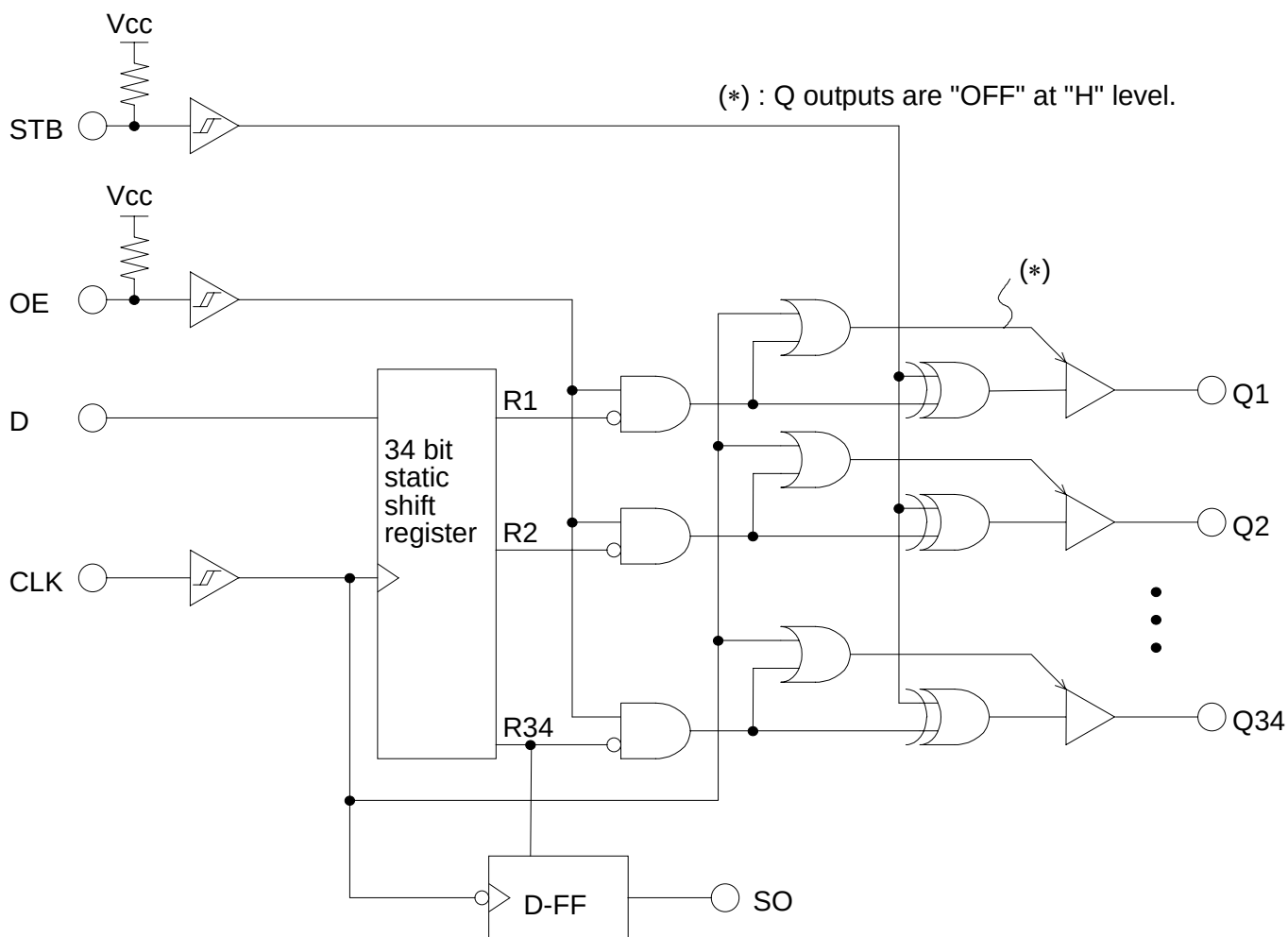


Fig. 2. Function Block Diagram (Positive Logic)

## 6. FUNCTION TABLE

|                  | CONTROL INPUT |   |        |     | SHIFT REGISTER | OUTPUT |         |
|------------------|---------------|---|--------|-----|----------------|--------|---------|
|                  | CLK           | D | OE(*4) | STB | Rn             | SO(*1) | Q       |
| SHIFT OPERATION  | ↑             | * | H      | *   | shift          | R34    |         |
|                  | no↑           | * | H      | *   | keep           |        |         |
| OUTPUT OPERATION | L             | * | H      | H   | H              |        | H (*2)  |
|                  |               |   |        | L   | L              |        | OFF     |
|                  |               |   |        |     | H              |        | L (*3)  |
|                  |               |   |        |     | L              |        | OFF     |
|                  | H             | * | H      | *   | *              |        | ALL OFF |

(\*1) 34th data is pushed out as output at the state of down edge↓ of clock signal.

(\*2) When shift register is "H", source SCR of Q output is driven to ON.

(\*3) When shift register is "H", sink SCR of Q output is driven to ON.

(\*4) OE must be kept "H".

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## 7. INPUT / OUTPUT CIRCUIT

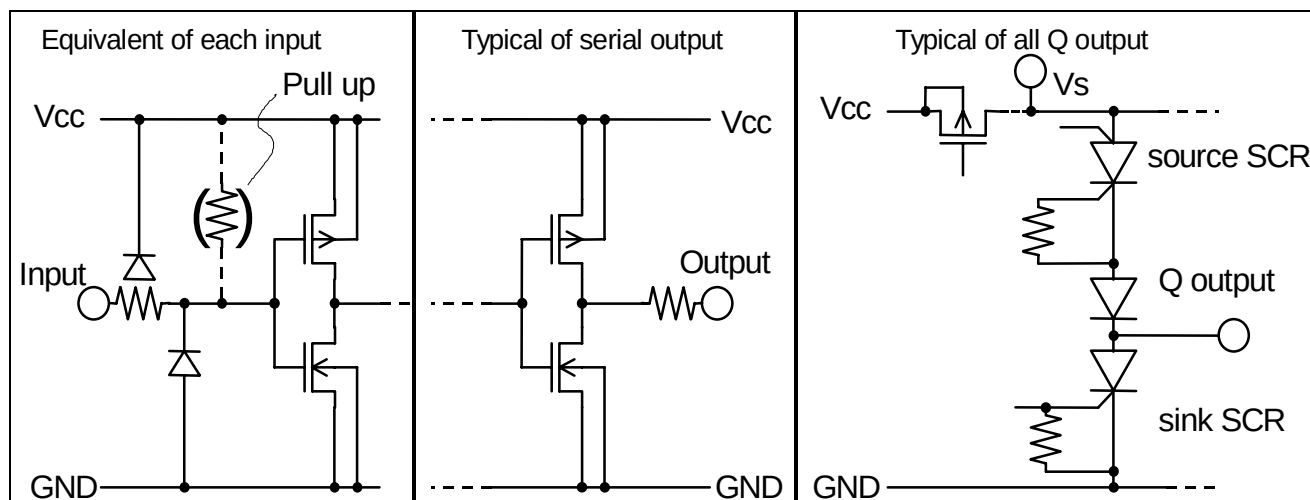


Fig. 3. Input / Output Circuit

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## 8. EXAMPLE OF OPERATING TIMING CHART

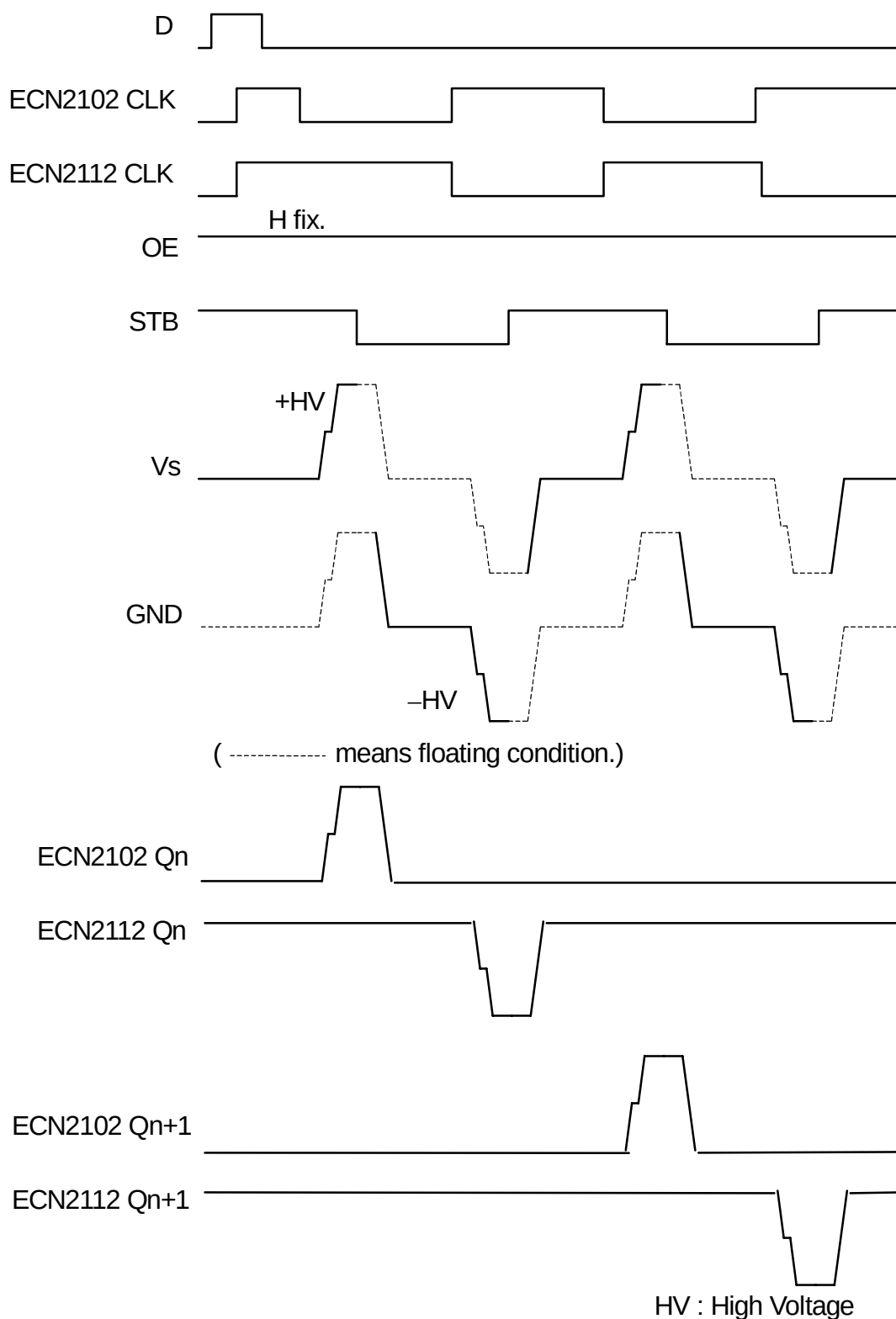
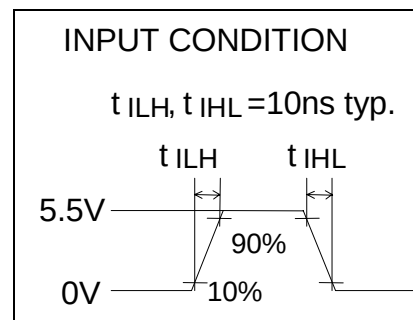
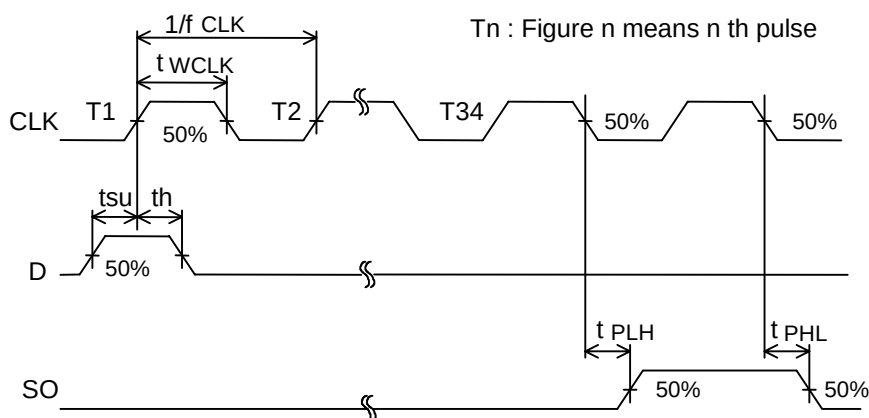


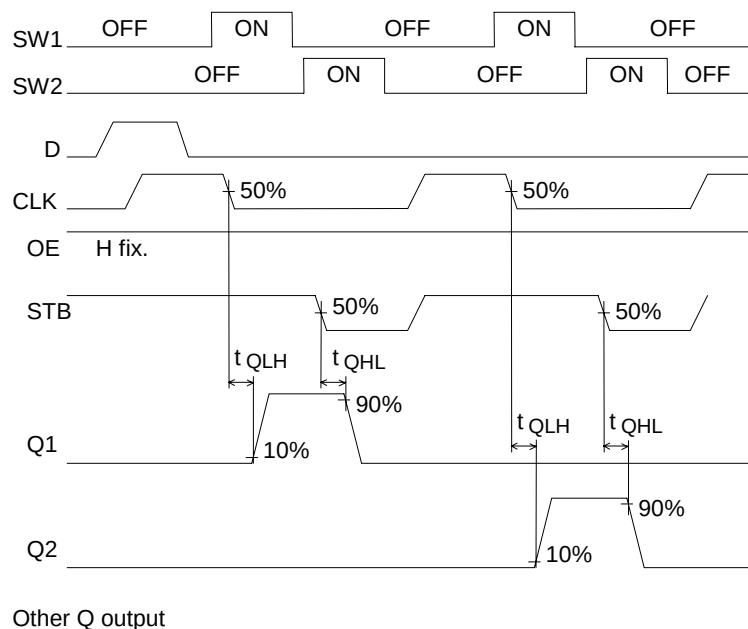
Fig. 4. Example of Operating Timing Chart

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## 9. MEASUREMENT AND MEASUREMENT CIRCUIT



(a) Shift function (SW1→OFF, SW2,3→ON)



(b) Output Function (SW3→OFF)

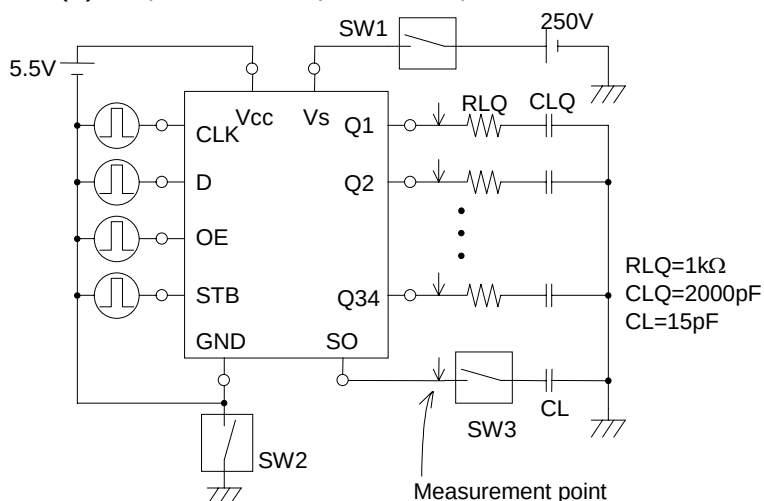


Fig. 5. Switching Characteristics Measurement Circuit

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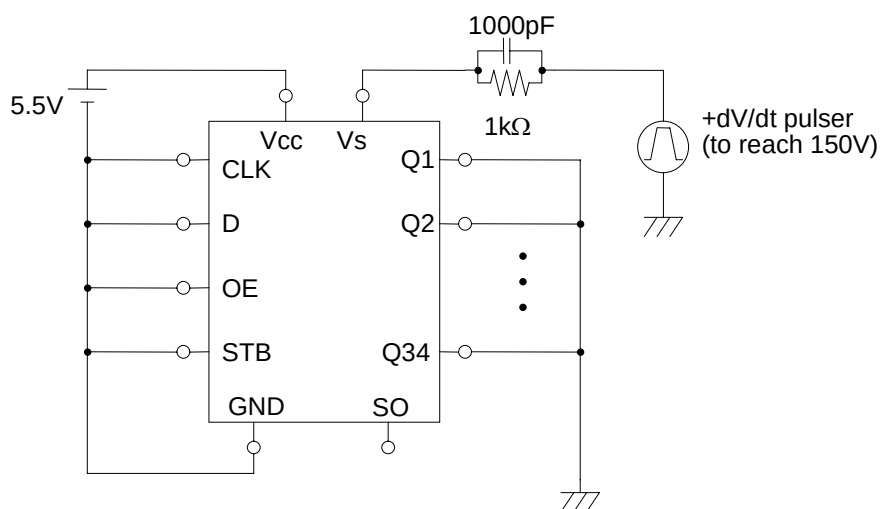


Fig. 6. Output SCR dV/dt capability (dV/dt1) Measurement Circuit

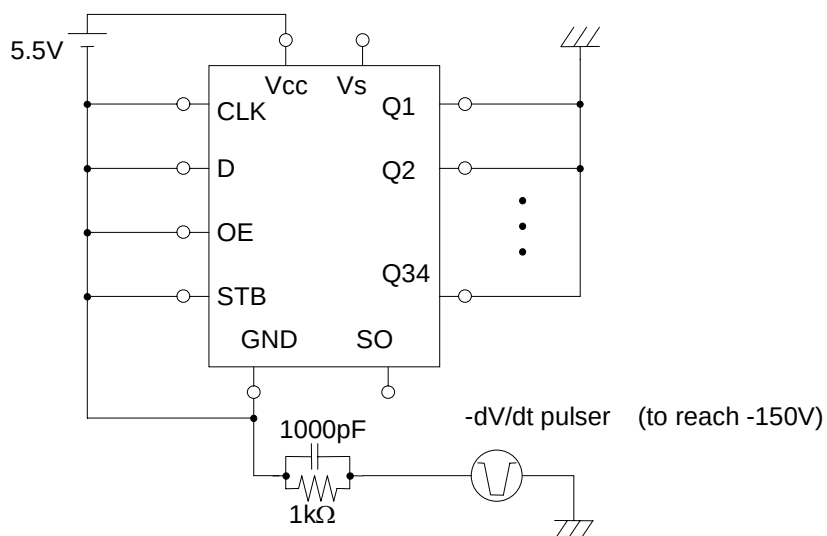
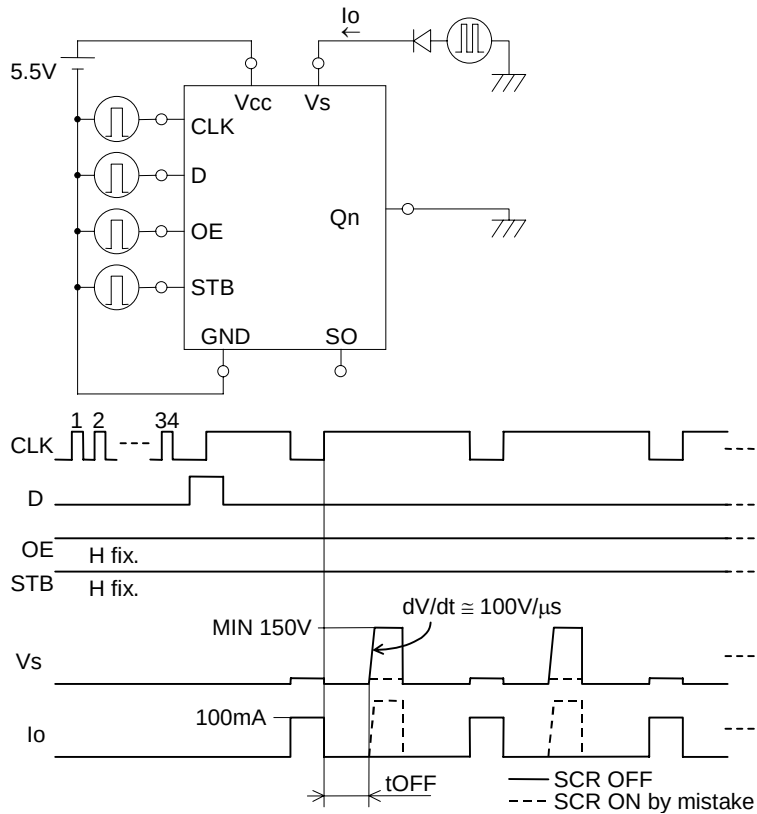


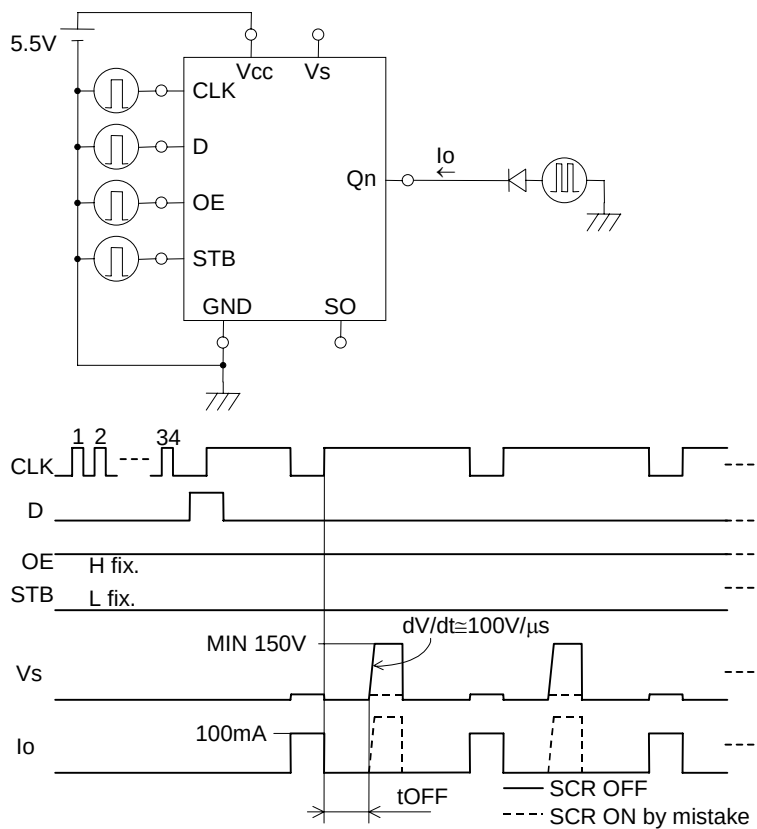
Fig. 7. Output SCR dV/dt capability (dV/dt2) Measurement Circuit



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(a) Source SCR

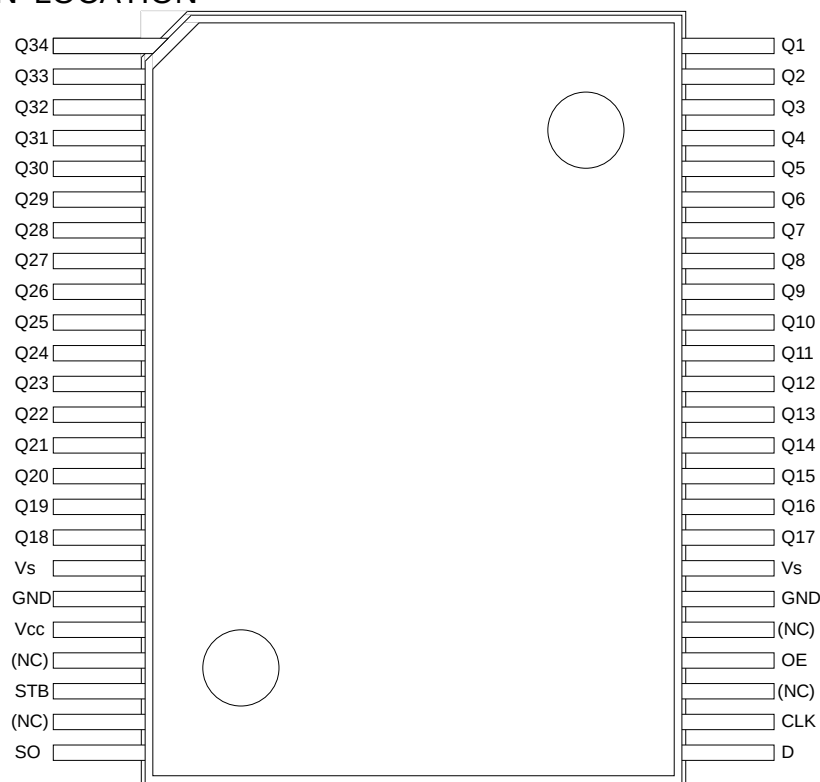


(b) Sink SCR

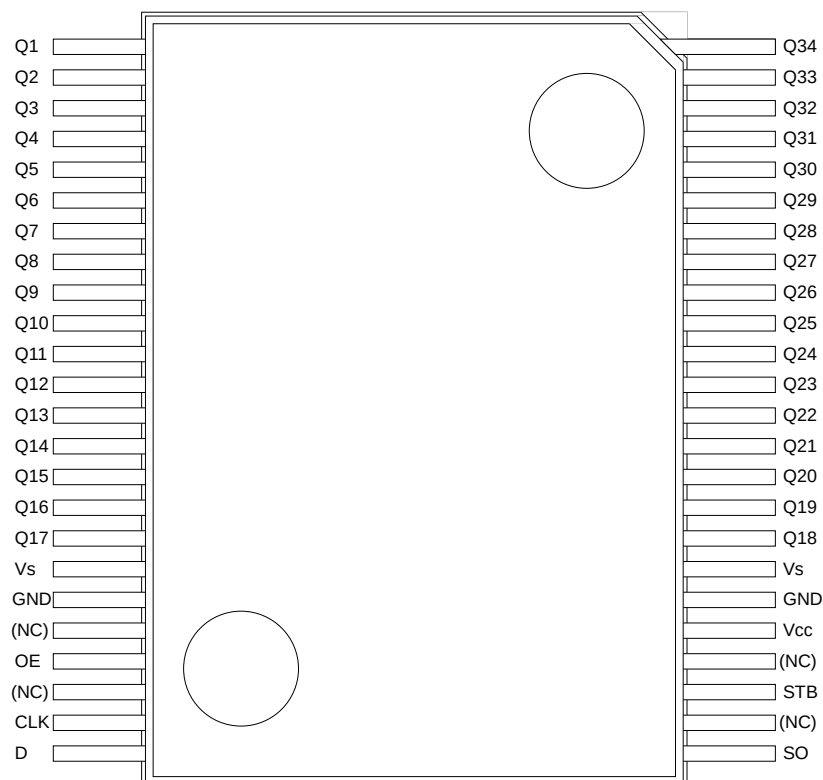
Fig. 8. Output SCR tOFF Measurement

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## 10. PIN LOCATION



(a) ECN2102



(b) ECN2112

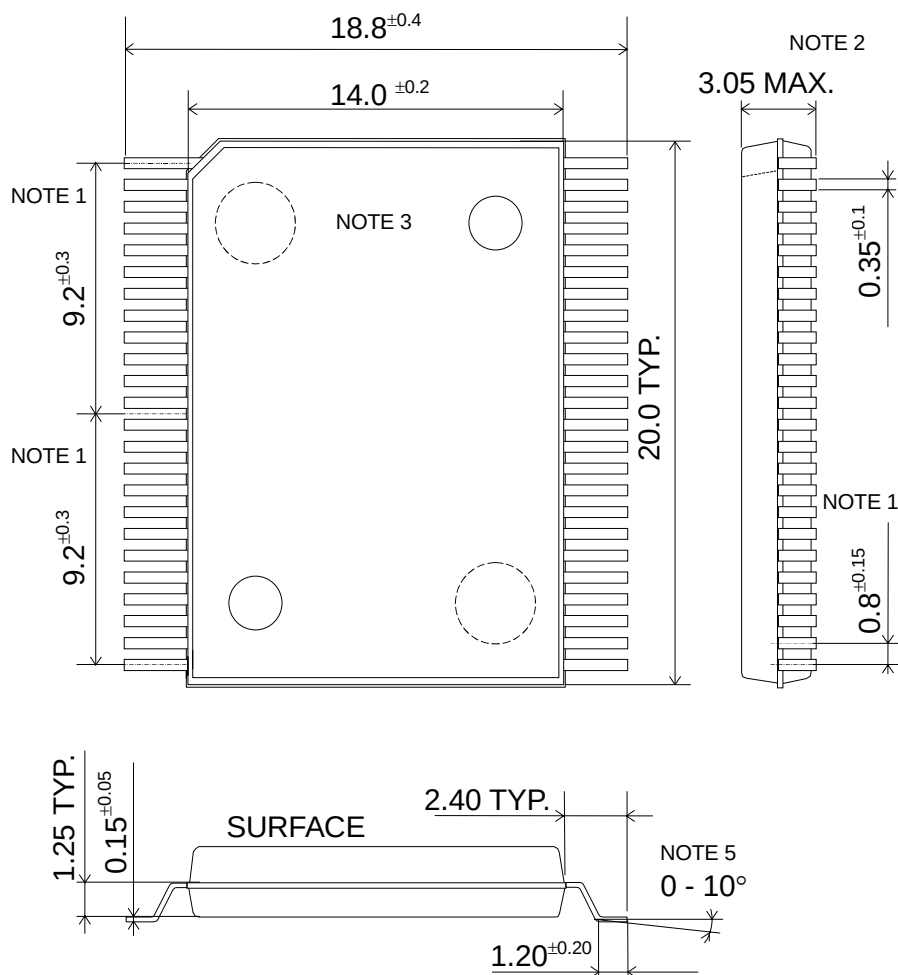
Fig. 9. Pin Location (Top view)

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## 11. PACKAGE OUTLINE

(Unit : mm)

### (1) ECN2102



#### Notes.

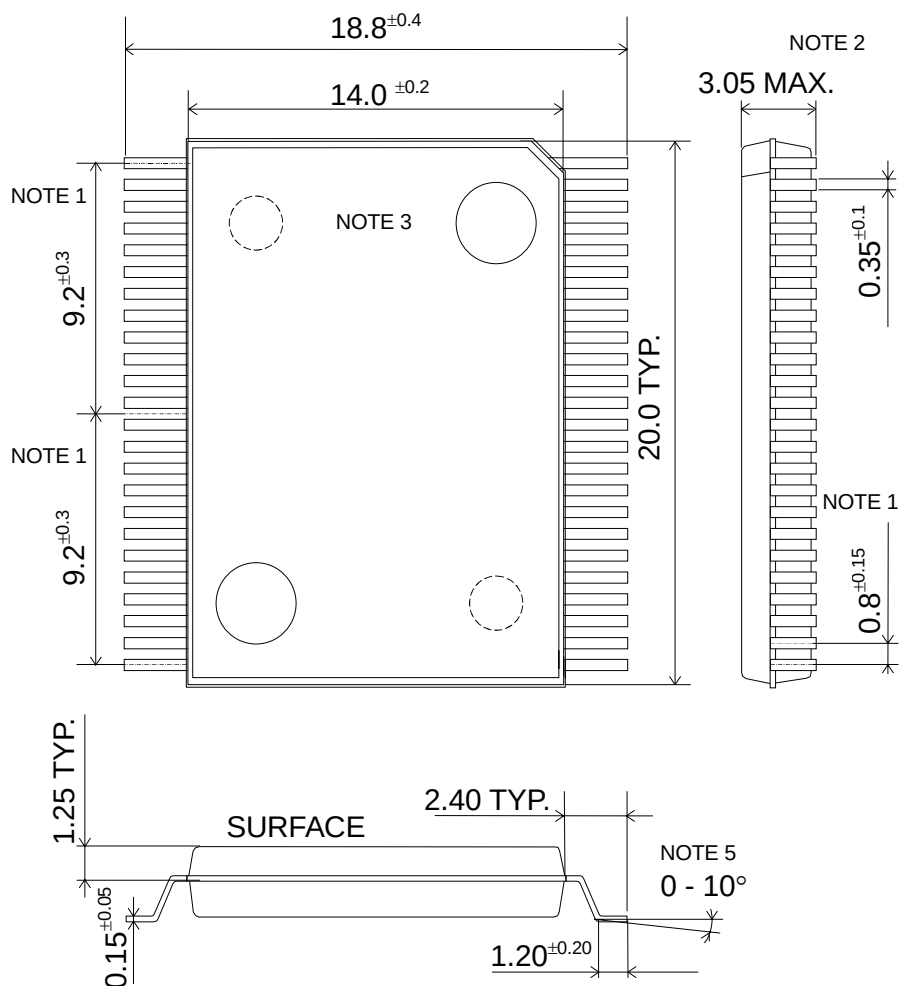
1. THIS DIMENSION IS MEASURED AT ROOT OF LEAD. SPACING AT TIP OF LEAD IS MIN 0.2.
2. THIS DIMENSION INCLUDES A WARPAGE OF PACKAGE.
3. MARKING IS ON THE SURFACE OF PACKAGE, INCLUDING HITACHI MARK, TYPE NAME, LOT NUMBER, AND JAPAN MARK.
4. LEADS ARE SOLDER PLATED.
5. THIS IS THE BENDING ANGLE WITH HORIZONTAL PLANE.

Fig. 10. Package outline (ECN2102)

# ECN2102/2112

(Unit : mm)

(2) ECN2112



Notes.

1. THIS DIMENSION IS MEASURED AT ROOT OF LEAD. SPACING AT TIP OF LEAD IS MIN 0.2.
2. THIS DIMENSION INCLUDES A WARPAGE OF PACKAGE.
3. MARKING IS ON THE SURFACE OF PACKAGE, INCLUDING HITACHI MARK, TYPE NAME, LOT NUMBER, AND JAPAN MARK.
4. LEADS ARE SOLDER PLATED.
5. THIS IS THE BENDING ANGLE WITH HORIZONTAL PLANE.

Fig. 11. Package outline (ECN2112)

# HITACHI POWER SEMICONDUCTORS

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