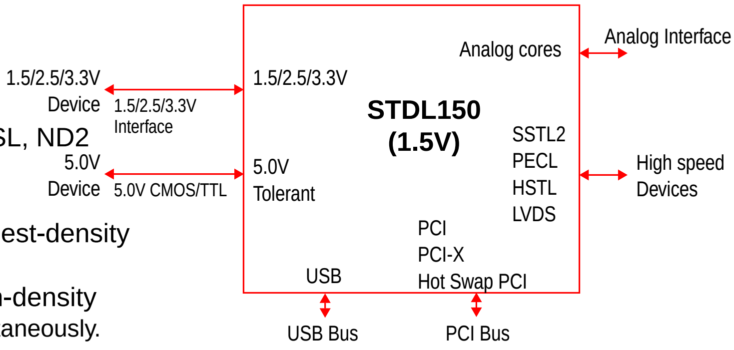
STDL150 Standard Cell
0.13um System-On-Chip ASIC

March 2002, V1.0

Features

- L_{drawn} = 0.13um
- Up to 45.8 million gates
- Power dissipation: 13nW/MHz@1.5V, 2SL, ND2
- Gate Delay: 69ps@1.5V, 2SL, ND2
- 1.5/2.5/3.3V drive and 5V tolerant I/O
- Low-power compiled SRAM/ROM with best-density
- 1.5V and 3.3V ADC,DAC and PLLs
- ARM920T/ARM940T, TeakLite/TeakHigh-density

NOTE: 2.5V and 3.3V cannot be used simultaneously.



Description

STDL150 is one of the Samsung ASIC library, which consists of standard cell products implemented in a 0.13um technology. STDL150 utilizes seven layers of interconnect metal having metal 4, 5, 6 and 7 layer options for products. STDL150 is diverse application specific digital and analog IPs for system-on-chip(SOC) application. Samsung provides a full range of products to address the challenges of producing portable devices that take advantage of SOC integration.

STDL150 which reduced power dissipation and system cost by merging the logic and IPs as a whole and connecting internally from logic to memory data bus is ideal for low-power products such as HHP, PDA and Mobile.

STDL150 supports up to 45.8 million gates counts of logic providing 85% of usable gate. Gate delay is 30%~40% slower than that of STD150, 0.13um library. Logic density is exactly same as that of STD150.

STDL150 also supports fully user-configurable compiled memory elements for low-power with minimum area loss. In STDL150, the density of compiled memory is 20% less than that of STD150. Each element is provided as a compiler. For high-capacity memory solution in SOC design, the repairable memory containing redundancy scheme is also provided as a compiler.

Variety of IPs are provided in STDL150 family including

- Processor Cores :
  ARM7T/ARM9T/ARM940T/ARM920T/ARM946E/ARM926EJ/ARM1020E/ETM7/ETM9 from ARM, TeakLite/TEAK from DSPG
- Memories
  Low-power compiled SRAM
  High-density compiled ROM/Registor file,
  Low-power repairable SRAM with redundancy
- Analog Cores :
  ADC, DAC, PLL
- IO IPs :
  USB, PCI-X, ATA-6, LVDS, SSTL2, HSTL, PECL

Samsung design methodology offers an comprehensive timing driven design flow including automated time budgeting, tight floorplan synthesis integration, powerful timing analysis and timing driven layout. Its advanced characterization flow provides accurate timing data and robust delay models for a 0.13um very deep-submicron technology. Static verification methods such as static timing analysis and formal equivalence checking provide an effective verification methodology with a variety of simulators. Samsung DFT methodology supports scan design, BIST and JTAG boundary scan. Samsung provides a full set of test-ready IPs with an efficient core test integration methodology.

Samsung ASIC Macros

Analog Cores

- Ultra low voltage analog cores: 1.5V
- High resolution analog cores: 3.3V

Analog Cores	Bit	Supply Voltage		
		3.3V± 5%	2.5V± 5%	1.5V± 5%
ADC	8	- 125MHz	-	30MHz
	10	- 500KHz	- 30MHz	-
DAC	10	- 250MHz	- 300MHz	-
	12	- 250MHz	- 80MHz	-
PLL		-	-	- 20 ~ 100MHz - 50 ~ 300MHz - 100 ~ 500MHz

Digital Cores

Application	Hard macro	Soft macro
ARM cores	- ARM7TDMI - ARM9TDMI - ARM940T - ARM920T - ARM1020E - ARM946E - ARM926EJ - ETM7 - ETM9	AMBA
DSP cores	- Teaklite - Teak	-
Interface cores	-	USB1.1, USB2.0, IrDA UART(16C450,16C550) IEEE1284, P1394a LINK
Communication cores	-	10/100 Ethernet MAC
Peripheral cores for ARM	Memory Controller, DMA Controller Timer, WDC, GPIO, SSI, Color LCD controller, Smart CARD I/F, UART_PrimeCell, Keyboard/Mouse I/F, I2C, Audio Card I/F, Real-Time Clock	

Memory Compiler

- Fully user-configurable SRAM/ROM
- Single-port(1RW, 1R), dual-port(2RW), multi-port(1R1W, 2R1W, 2R2W)
- Duty-free cycle and zero hold time in synchronous
- Bit-write feature available
- Flexible column mux
- Up to 1M-bit repairable SRAM
- Up to 4M-bit high-capacity SRAM/ROM

Name	Description
SPSRAM_LPL	- Single Port Synchronous static RAM - up to 256Kbits
SPSRAMBW_LPL	- SPSRAM with Bit-Write - up to 256Kbits
SPSRAMR_LPL	- SPSRAM with Redundancy - up to 1Mbits
DPSRAM_LPL	- Dual Port Synchronous static RAM - up to 128Kbits
DPSRAMBW_LPL	- DPSRAM with Bit-Write - up to 128Kbits
VROM_HDL	- Synchronous Via-1 programmable ROM - up to 1Mbits
SRFRAM_HDL	- Multi-port Synchronous Register File - 1R1W, 2R1W and 2R2W available - up to 16Kbits
SRFRAMBW_HDL	- SRFRAM with Bit-Write - 1R1W, 2R1W and 2R2W available - up to 16Kbits
FIFO_HDL*	- Synchronous First-In First-Out Memory - up to 64Kbits
CAM_HDL*	- Synchronous Content Addressable Memory with Binary - up to 32Kbits
HCSPSRAM_HDL*	- Single-Part Synchronous static SRAM with burst Read/Write Feature - up to 4Mbits
HCVROM_HDL*	- Synchronous Via-1 Programmable ROM - up to 4Mbits

* On demand

I/Os and I/O IPs

- 1.5V/2.5V and 3.3V drive I/Os, and 5V tolerant I/O
  - If you want 3.3V tolerant I/O, please contact SEC technical service engineer
- 3-level (high, medium, no) slew rate control
- Driving capability
  - 1,2,4,8,12mA(for drive I/Os)
  - 1,2,4,6mA(for tolerant I/Os)
- I/O IPs

Name	**Description**	**Frequency(MHz)**
PCI	2.2 compliant, 5V tolerant	33, 66Mbps
USB	2.0 compliant, High Speed/Full Speed/ Low Speed	480/12/1.5Mbps
SSTL2	Class-I and II, SDRAM Interface	Up to 200
ATA	ATA-6/UDMA100, 133 3.3/5V tolerant	25, 33
PECL	ATM interface	200(single) 500(differential)
HSTL	1.5V, SRAM interface	300
Hot Swap PCI	1V pre-charge, VIO precharge	33, 66Mbps
PCI-X	1.0 compliant, 3.3V	133Mbps
LVDS	TIA/EIA-644	300

Recommended Operating Conditions

	Parameter	**Rating**		**Unit**
V_{DD}	DC supply voltage‘	1.5V I/O	1.4 to 1.6	V
		2.5V I/O	2.3 to 2.7	
		3.3V I/O	3.0 to 3.6	
		5V tolerant I/O	3.0 to 3.6	
	Analog Core DC supply voltage	3.3V core	3.3V± 5%	
		2.5V core	2.5V± 5%	
		1.2V/1.5V core	1.2V± 5%	
T_A	Commercial temperature range		0 to 70	°C
	Industrial temperature range * If you want this range, please contact field application engineer in Samsung.		– 40 to 85	

ASIC Design Kit and EDA support

Design Flow	**Design Kits**
Logic Synthesis	Synopsys Design Compiler
Physical Synthesis	Synopsys Physical Compiler
Logic Simulation	Cadence Verilog-XL, Cadence NC-Verilog/VHDL, Mentor ModelSim-Verilog/VHDL, Synopsys VCS
Scan Insertion and ATPG	Synopsys BSDCompiler, Synopsys TetraMax, Mentor Fastscan
Static Timing Analysis	Synopsys PrimeTime
RC Analysis	Avant! Star-RCXT
Power Analysis	Synopsys DesignPower, CubicPower*, Sequence WattWatcher
Formal Verification	Synopsys Formality, Avant ! DesignVERIFYer, Verplex Tuxedo-LEC
Fault Simulation	Cadence Verifault
Delay Calculator	CubicDelay*
Floorplanner	Avant! PlanetPL, Cadence DesignPlanner, CubicPlan*
P&R	Avant! Apollo, Cadence Silicon Ensemble
DRC and LVS	Dracula, Hercules, Calibre

* In-house tools

Package Availability

Package Type	**# of Pins**
QFP	44,48,60,64,80,100,128.144,160,208,240,256,304
LQFP	32,48,64,100,128,144,160,176,208,256
TQFP	64,80,100,128,144
BGA	196,208,225,256,272,292,352,388,492
FBGA(PCB)	144,160,176,180,256
FBGA(Tape)	112,144,160,208
Multi Chip Package Availability	32,48,64,68,69,100,256

Samsung ASIC Worldwide

SSI
Samsung Semiconductor Incorporated
85 W. TASMAN DR., San Jose,
CA95134-1713, U.S.A.
TEL (1)-408-544-4545
FAX (1)-408-544-4950

SWTC
South West Technology Center
7700 Irvine Center Drive Suite 600
Irvine, CA 92618 USA
TEL (1)-949-753-7530
FAX (1)-714-236-9664

SSEG
Samsung Semiconductor Europe GMBH
ASIC Design Center, Representation Office Munich
Carl-Zeiss-Ring 9, 85737 Ismaning
TEL (49)-89-9697-7117
FAX (49)-89-9697-7126

SSEL
Samsung Semiconductor Europe Ltd.
Great West House, Great West Road
Brentford, Middlesex TW8 9DQ U. K.
TEL (44)-208-380-7115
FAX (44)-208-380-7095

SEJA
Samsung Electronics Japan Co., Ltd. ASIC Center
Hamacho Center Bldg., 16th Floor 31-1, Nihonbashi-Hamacho, 2-Chome, Chou-ku, Tokyo 103, Japan
TEL (81)-3-5641-9850(8488)
FAX (81)-3-5641-9851

CoAsia
CoAsia Microelectronics Corp.
9F, No. 69, Chou Tze St., Neihu Teipei, Taiwan
TEL (886)-2-2658-2020 Ext. 308
FAX (886)-2-2658-0101

ComSOC
ComSOC Technology Pte Ltd.,
31 International Business Park,
#04-06 Creative Resource
Singapore 609921
TEL (65)-425-2212
FAX (65)-425-2022

C&S
HaeJu bldg. 6th fl., Nonhyun-dong, Gangnam-gu, Seoul, Korea
TEL(02)-515-4468
FAX(02)-515-4469

ECT
JoonSung bldg. 4th fl., 698-30 Yeuksam-dong, Gangnam-gu, Seoul, Korea
TEL(02)-569-1960
FAX(02)-569-2388

Dawin Tech
Osuk bldg. 6th fl., 276-6 Yangje-dong, Seocho-gu, Seoul, Korea
TEL(02)-529-2826
FAX(02)-529-2827

VersaChips
Boram bldg. 6th fl., 288-2 Yangje-dong, Seocho-gu, Seoul, Korea
TEL(02)-572-0756
FAX(02)-571-3857

SAMSUNG ELECTRONICS CO., LTD.
San #24, Nongseo-Ri, Giheng-Eup,
Yongin-City, Gyeonggi-Do, KOREA
TEL : 82-31-209-6500
FAX : 82-31-209-4920
http://www.samsungelectronics.com/semiconductors/asic/asic.htm